

AMPEX

TBC-3
Service Manual

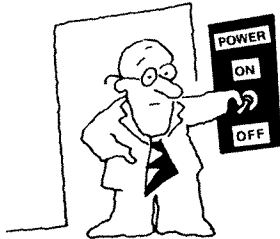


SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:

1



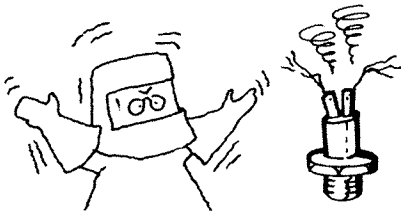
Do not attempt to adjust unprotected circuit controls or to dress leads with power on.

4



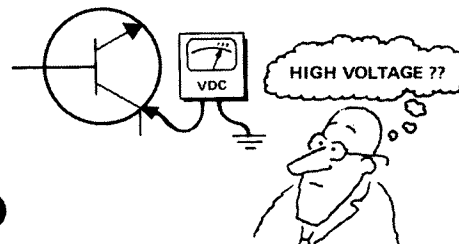
Always avoid placing parts of the body in series between ground and circuit points.

2



To avoid burns, do not touch heavily loaded or overheated components without precaution.

5



Remember that some semiconductor cases and solid-state circuits carry high voltages.

3



Do not assume that all danger of electrical shock is removed when power is off. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

6



Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS REMOVED OR YOU MAY ALSO BECOME A SHOCK VICTIM.

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

- ① When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.
 - ② When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.
 - ③ When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.
 - ④ When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.
 - ⑤ When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.
-

WARNING

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case, the user, at his own expense, will be required to take whatever measures may be necessary to correct the interference.

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TBC-3



TBC-3 Digital Time Base Corrector

PART 1

SECTION 1

INTRODUCTION AND SYSTEM HARDWARE

1-1 PURPOSE, SCOPE, AND ORGANIZATION OF MANUAL

This service manual provides theory and maintenance information for the TBC-3 Digital Time Base Corrector (NTSC 12- and 16-line memory versions), Ampex Part No. 1463500. Maintenance information includes the use of the TBC-3 with Ampex models VPR-2B and VPR-3 videotape recorders.

Part I of this manual includes descriptive and maintenance information at the system level; Part II gives descriptive and maintenance information of each printed wiring assembly (PWA).

Part I of the manual has three sections:

- Section 1, *Introduction and System Hardware*, illustrates mechanical elements and summarizes major system components and power, signal, and control elements.
- Section 2, *System Description*, presents system-level theory emphasizing the interrelationships among the PWAs.
- Section 3, *System Maintenance*, introduces a general maintenance plan for the TBC and presents a series of system level adjustments.

Part II of the manual begins with Section 4 and presents each PWA in a separate section which includes theory, maintenance procedures, and reference data. This reference material consists of block diagrams, simplified schematics, and timing waveforms.

1-2 RELATED PUBLICATIONS

This manual is the service volume of the TBC-3 manual complement made up of:

- *TBC-3 Digital Time Base Corrector, Installation and Operation*, Catalog No. 1809605
- *TBC-3 Digital Time Base Corrector, Parts Lists and Schematics*, Catalog No. 1809607

1-3 TBC-3 APPLICATION

The TBC-3 is a color television digital time-base corrector (DTBC) designed for use with one-inch Type C helical-scan videotape recorders (VTRs). Ampex VTRs in this category include the VPR-2B and VPR-3. The TBC-3 may also be used with

TBC-3

capstan-servoed 3/4-in. U-standard cassettes and 1/2-in. standard format VTRs. The unit has a correction range of greater than 10 horizontal lines on a 12-line memory system (14 horizontal lines on a 16-line system) and provides an output color signal stabilized to ± 2.5 ns. The output signal can be used (when genlocked) for fades, lap dissolves, special effects, transfer-to-film, and dubs to quadruplex or other types of recorders. The high stability of the signal permits multiple-generation dubbing.

The TBC-3 is supplied in two versions: 12-line memory and 16-line memory. The 16-line version is used with the Ampex VPR-3. The 12-line version is used with the Ampex VPR-2B and other one-inch Type C videotape recorders.

A standard element of the TBC-3 system is a sync generator which supplies sync signals when external sync is not available; it also can be genlocked to a station sync generator.

The TBC-3 has a slow-motion capability that can produce a broadcast-quality color picture at tape speeds from -1x reverse slow motion through freeze frame to +3x forward slow motion when used with the VPR-3 (-0.25x to +1.25x with the VPR-2B).

The TBC-3 is capable of producing monochrome pictures suitable for monitoring at helical recorder search speeds in either direction up to 300 ips on the VPR-2B and up to 500 ips on the VPR-3.

1-4 TBC-3 SYSTEM HARDWARE

1-5 Physical Description

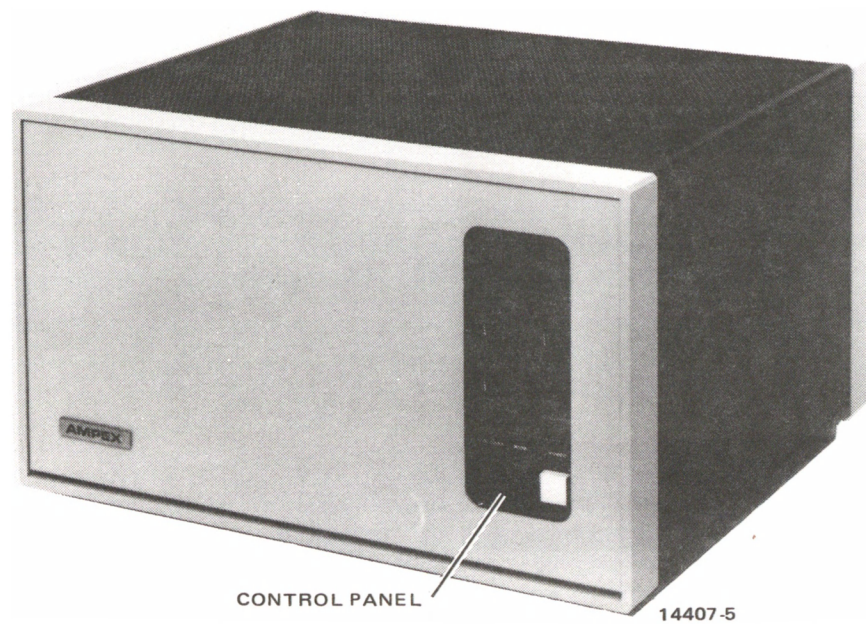
The TBC-3 is a self-contained unit that includes a power supply. Digital and analog processing circuits are contained in up to 15 individual PWAs that plug into a single card rack chassis. The unit can be mounted in a standard 19-in. rack, or mounted in a VPR-2B or VPR-3 console. The unit is also available in a standalone cabinet. Three views of the system are shown in Figure 1-1, along with lists of the major subassemblies and options.

1-6 Options and Accessories

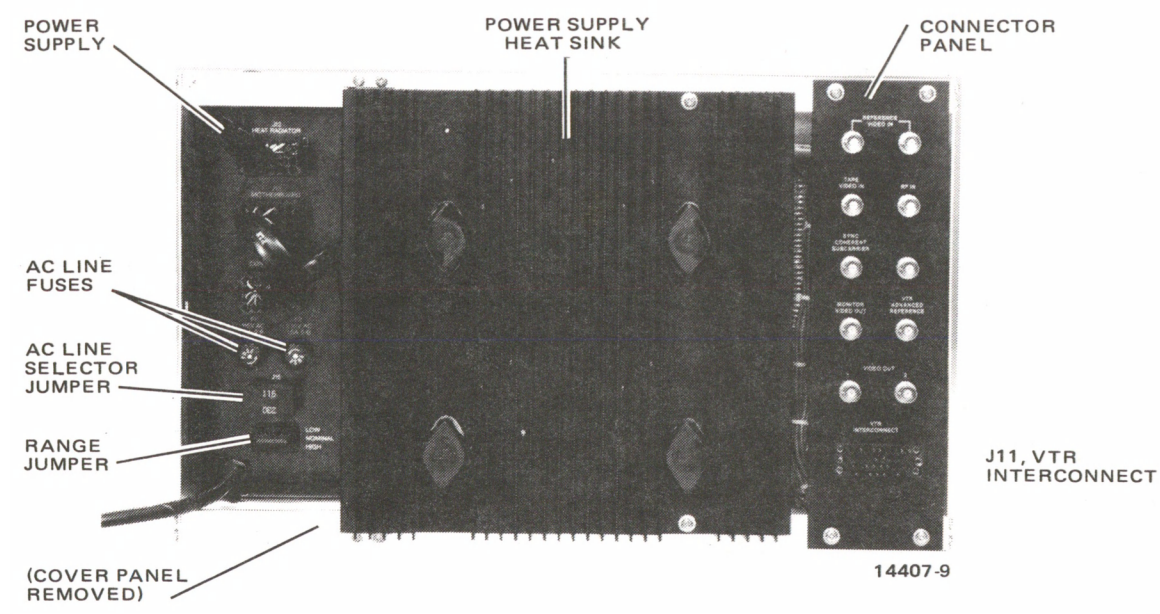
Refer to the options list in Figure 1-1. Options referred to in this manual are:

- 12-line memory option, used with the Ampex VPR-2B/VPR-80
- 16-line memory option, used with Ampex VPR-3
- Mounting options that include remote control panels

An extender board necessary for maintenance is included with the furnished miscellaneous parts kit. This manual assumes all options are integrated into the system and the system is described and tested in those terms.



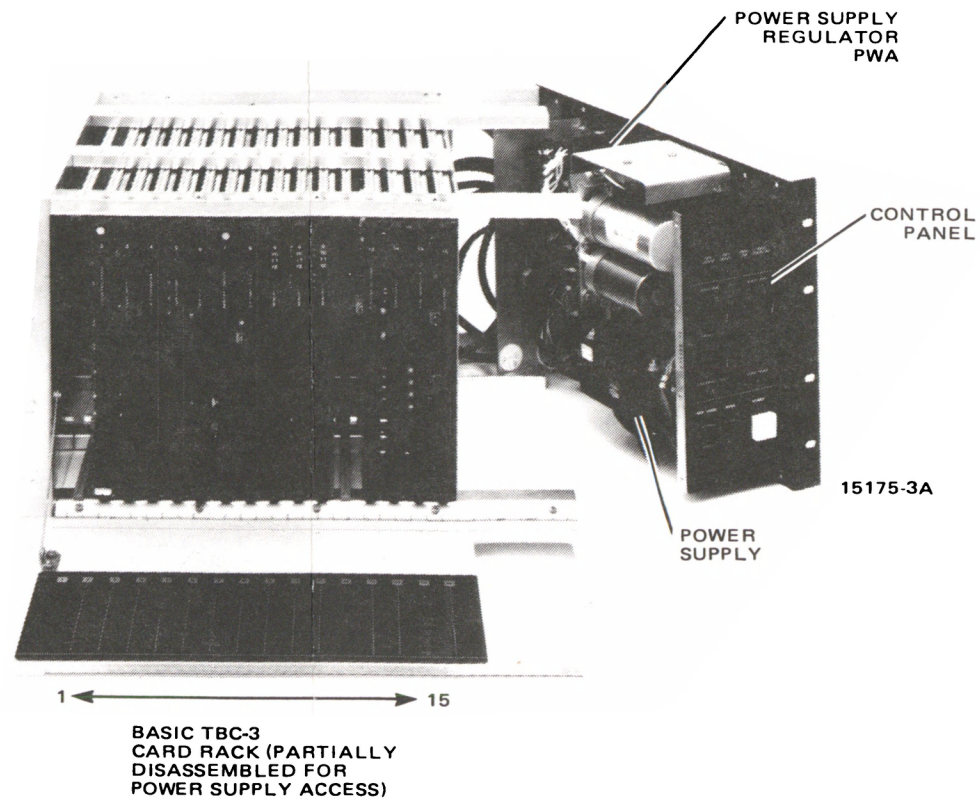
OPTIONAL STAND ALONE CABINET



REAR VIEW

NTSC Kit Printed Wiring Assemblies (PWA)

PWA	Assembly No.	Description
1	1463589	Color Processor
2	1463650	Video Input
3	1463553	Analog-to-Digital Converter
4	1463568	Tape H Comparator
5	1463528	Tape VCO
6	1463556	Memory Control (12-line)
6	1463537	Memory Control (16-line)
7	1463601	Serial-to-Parallel Converter with One-Line DOC
8	1463574	Memory
9	1463574	Memory
10	1463574	Memory
11	1463574	Memory for 16-line use)
12	1463531	Parallel-to-Serial Converter w/Vel Comp
13	1405189	Video Output
14	1405186	Sync Generator (12-line)
15	1463659	Sync Generator (16-line)



TBC-3 Basic Assembly	1463501
Card Rack Assembly	1463506
Miscellaneous Parts Kit	1463518
Power Supply	1409155

TBC Accessories and Options

Kit	Kit No.
Console Mounting Kit for VPR-3	1463513
Console Mounting Kit for VPR-2B	1409130
Rack Mounting Kit	1463514
Cabinet Mounting	1409135
60-inch Interconnect Cable	1463674-AA
180-inch Interconnect Cable	1463674-AB
NTSC Kit, 12-line	1463505
NTSC Kit, 16-Line	1463508

Figure 1-1. System Hardware

TBC-3

1-7 Fuse, Power, and Signal Connections

Fuse, power, and signal data is tabulated with illustrations for quick reference in Figure 1-2. All connections are made at the rear panels as shown. Consult the installation and operation manual for detailed installation instructions. Panel markings for fuse size and use are self-explanatory but note that the +5-Vdc supply circuit breaker is mounted on the heat sink. The 115/230-power jumper range chart is also printed on the chassis.

1-8 SYSTEM CONTROLS AND INDICATORS

For standard operation, no routine adjustments need be made beyond initial setup of the unity trim controls at the top of the control panel for video level, black level, and chroma phase. However, a wider range of tape and facility conditions may be accommodated with control panel and PWA edge controls.

Standard operation in this manual is defined with reference to EIA standard RS170A recommendations for video signal definitions (presented in Section 2, *System Description*) with special emphasis on burst/sync phase on color field I for reliable color framing. If tape and reference video conform to standard video, adjustments to the TBC during recording sessions are minimal.

1-9 Control Panel Controls and Indicators

The control panel operator controls described in Table 1-1 are used to compensate for minor variations from standard tape and facility reference.

1-10 PWA Edge Controls and Indicators

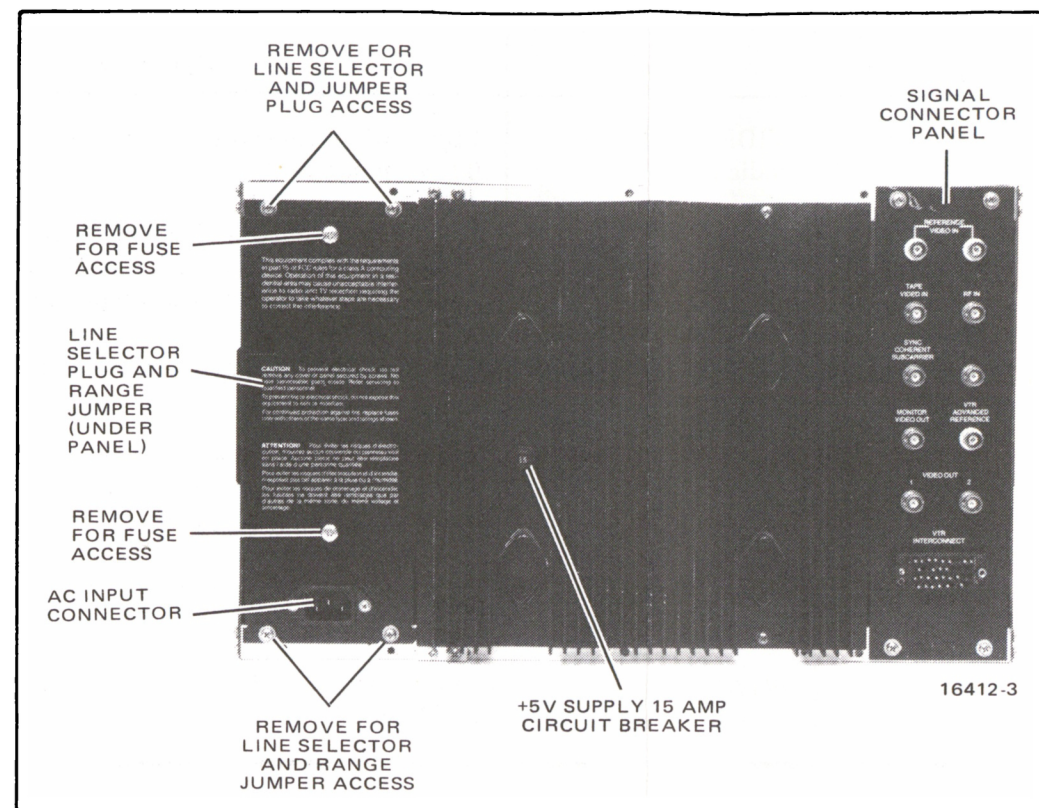
Some of the PWA edge controls summarized in Table 1-2 give the TBC flexibility to maintain correction under nonstandard conditions. Other edge controls are factory-set for basic TBC alignment.

Note

Unless instructed otherwise, do not use the extender when adjusting any edge controls.

A more detailed PWA edge control and indicator description is given in Figure 1-3. The descriptions are in terms of the conditions for adjustment, with references to the appropriate context for adjustment at the system or PWA maintenance level.

Rear Panel Power and Signal Connectors



AC Power/Range Jumper Positions

Line Voltage	Line Selector Jumper	Range Jumper Position
95-110	115	Low
104-126	115	Nominal
114-140	115	High
190-220	230	Low
208-252	230	Nominal
229-279	230	High

TBC-3 Fuse and Circuit Breaker Complement

Fuse Type	Function	Location
1.5A, slow blow	Prevents unit from drawing excessive line current. This fuse is in circuit only when line selector jumper is set for 230-Vac operation.	Mounted inside rear unit above line selector jumper.
3A, slow blow	Prevents unit from drawing excessive line current. This fuse is in circuit only when line selector jumper is set for 115-Vac operation.	Mounted inside rear of unit above line selector jumper.
15A circuit breaker	Prevents over current in the +5-Vdc regulator section of unit's power supply.	Mounted on rear heat sink. See Figure above.

Signal Interconnection Panel

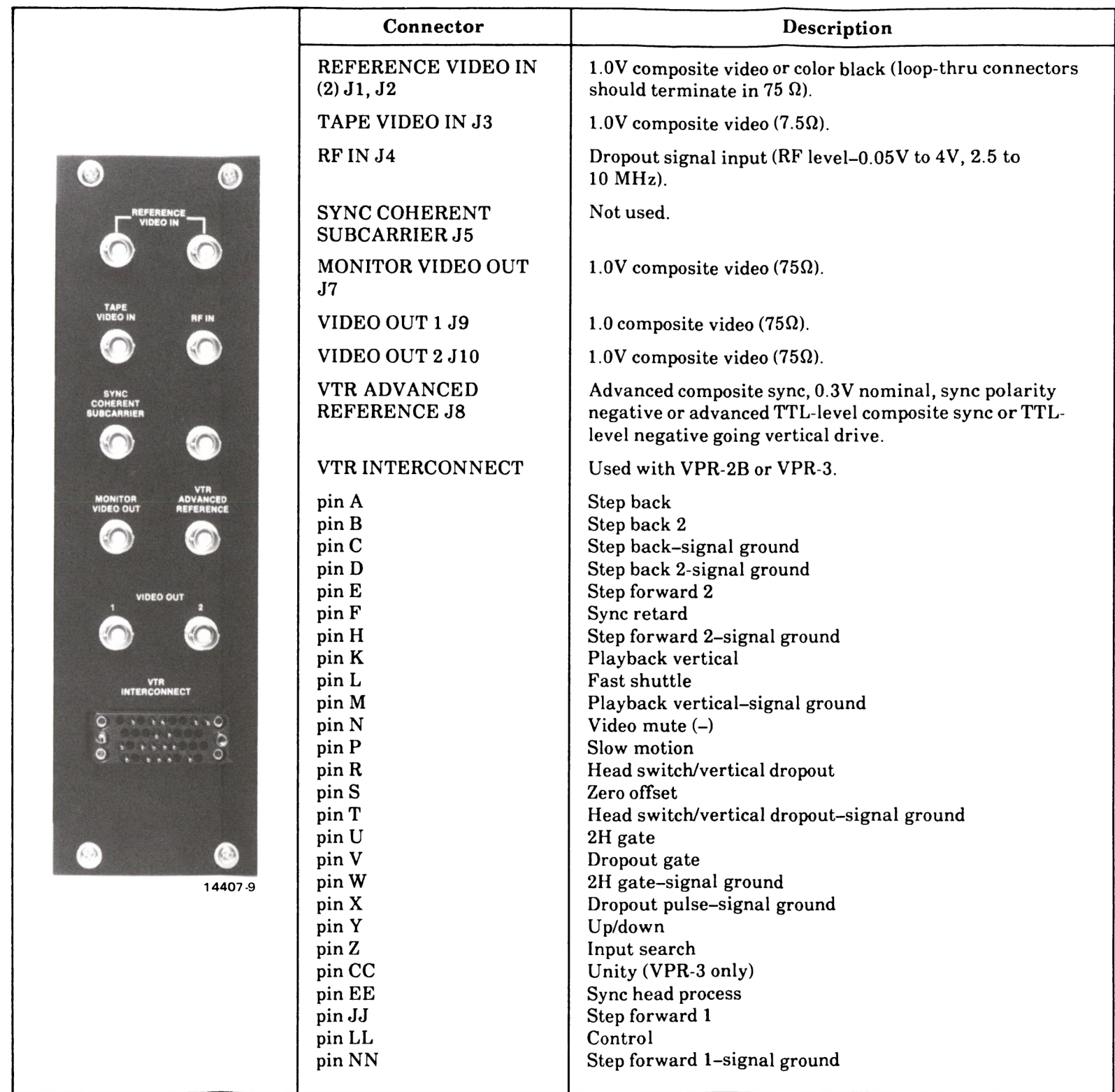
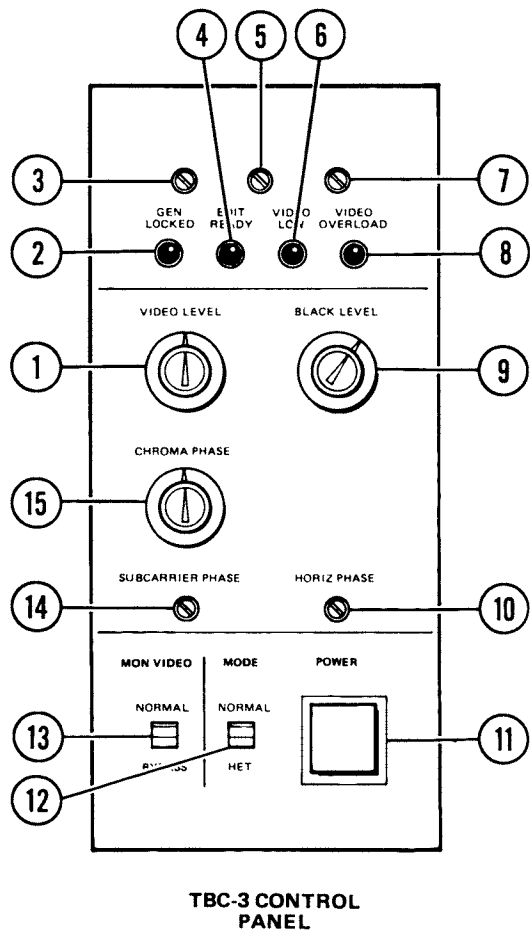


Table 1-1. Operating Controls and Indicators, Front Panel Assembly

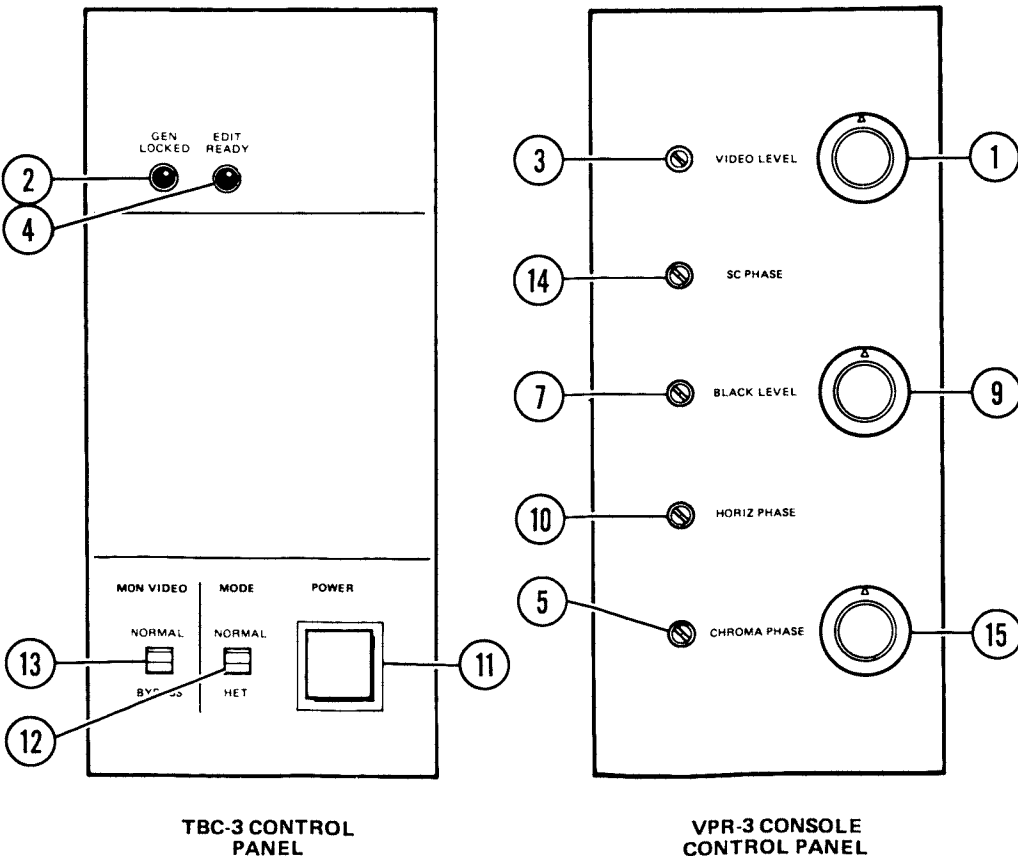
TBC-3

Index No.	Name	Function	Index No.	Name	Function	Index No.	Name	Function
1	VIDEO LEVEL potentiometer	Adjusts level of video output signal. Rotate control to center detent position for unity gain.	6	VIDEO LOW indicator	Lights when video input signal level is less than 0.8 Vp-p nominal.	12	MODE switch	Selects processing of heterodyne video signal when switch is in HET position.
2	GEN LOCKED indicator	12-line system. Indicator lights when TBC-3 is gen-locked to reference signal applied to REFERENCE VIDEO IN connector.	7	Unity black level trim potentiometer	Adjusts difference between black and blanking level of video output signal with BLACK LEVEL potentiometer in center unity position.	13	MON VIDEO switch	Selects monitor video output signal. In NORMAL position, processed TBC video is selected. In BYPASS position, video input signal from VTR is selected.
		16-line system. Indicator lights when TBC-3 is gen-locked to reference signal applied to REFERENCE VIDEO IN connector and the reference signal is RS170A (NTSC) standard.	8	VIDEO OVERLOAD indicator	Lights when video input signal level is greater than 1.25 Vp-p nominal.	14	SUBCARRIER PHASE potentiometer	Sets color subcarrier phase of VIDEO OUTPUT signal with respect to an external subcarrier. Used during fully synchronous operation to match color subcarrier phase to external signal sources.
3	Unity video level trim potentiometer	Adjusts level of video output signal with VIDEO LEVEL potentiometer set to unity gain position.	9	BLACK LEVEL potentiometer	Adjusts difference between black and blanking levels of video output signal. Rotate control to center detent position for unity black level.	15	CHROMA PHASE potentiometer	Adjusts phase of picture chrominance information with respect to color burst during playback. Rotate control to center detent position for unity chroma phase.
4	EDIT READY indicator	Lights when burst-to-sync relationship is within $\pm 40^\circ$ of that required.	10	HORIZ PHASE trim potentiometer	Adjusts output video position relative to reference sync.			
5	Unity chroma phase trim potentiometer	Adjusts the phase of picture chrominance information with respect to color burst during playback with CHROMA PHASE potentiometer set to center unity gain position.	11	POWER switch/indicator	Turns power to TBC on and off. Lights when switch is ON position.			

a. STANDALONE CONFIGURATION



b. VPR-3 CONSOLE CONFIGURATION



c. VPR-2B CONSOLE CONFIGURATION

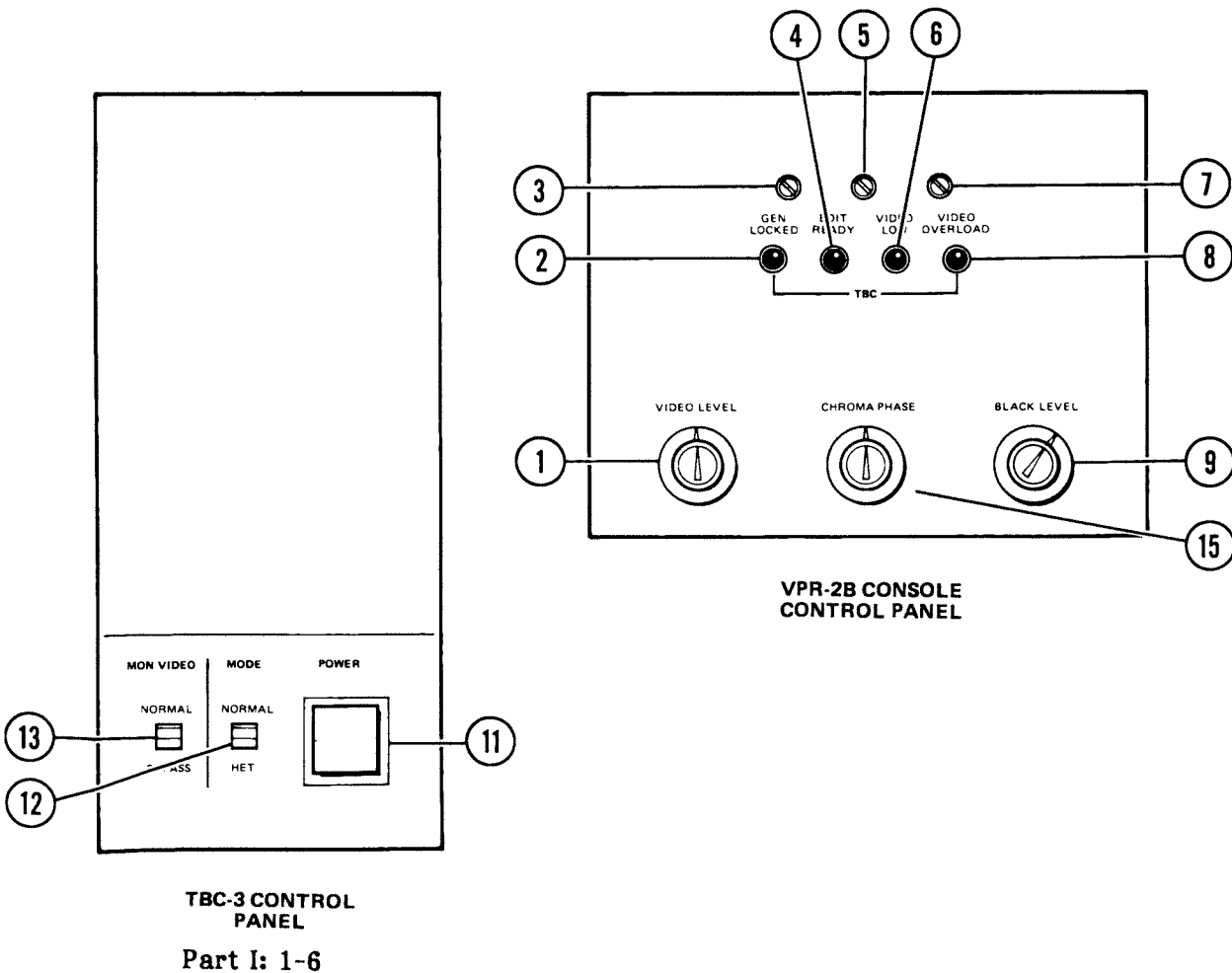
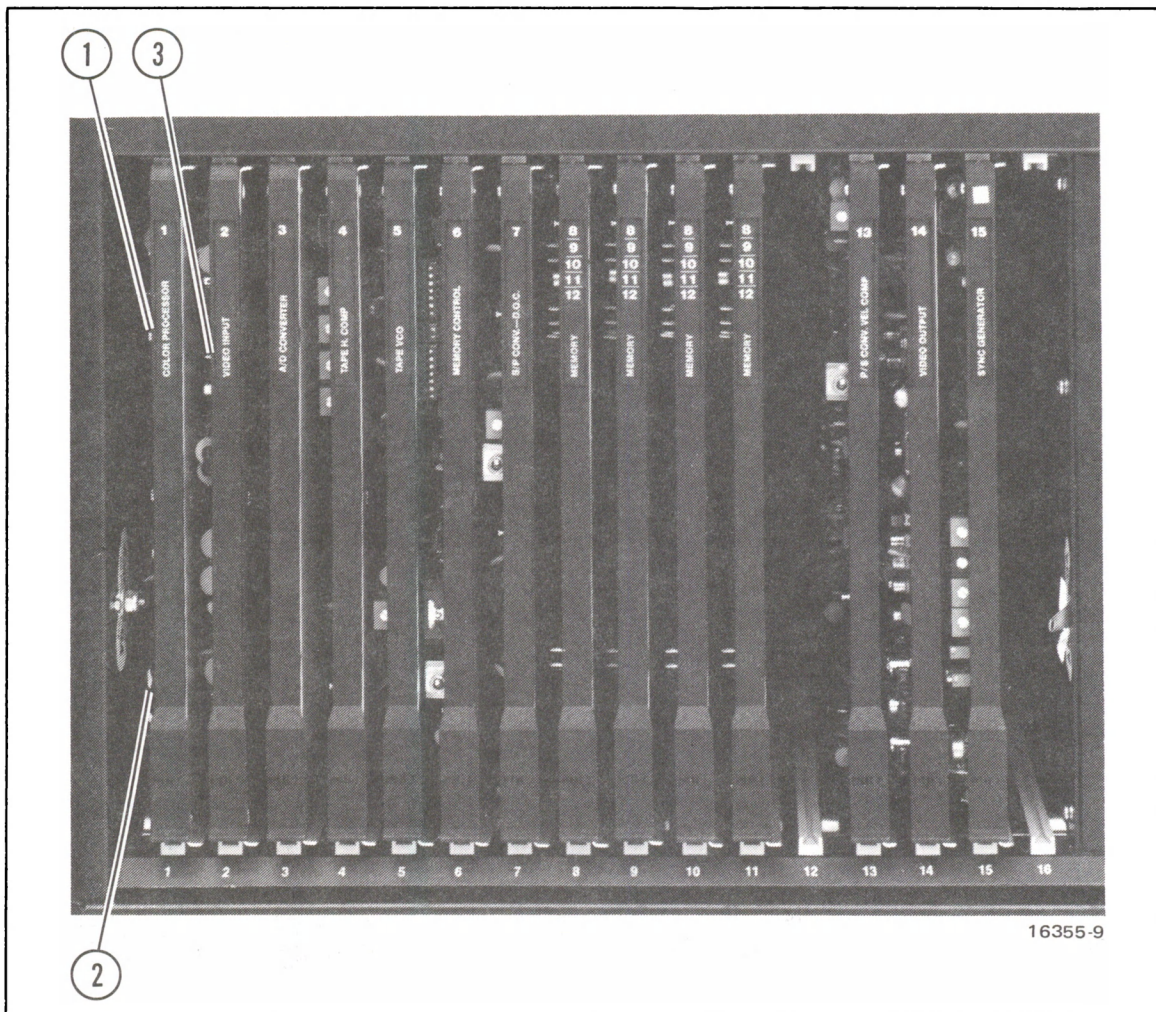


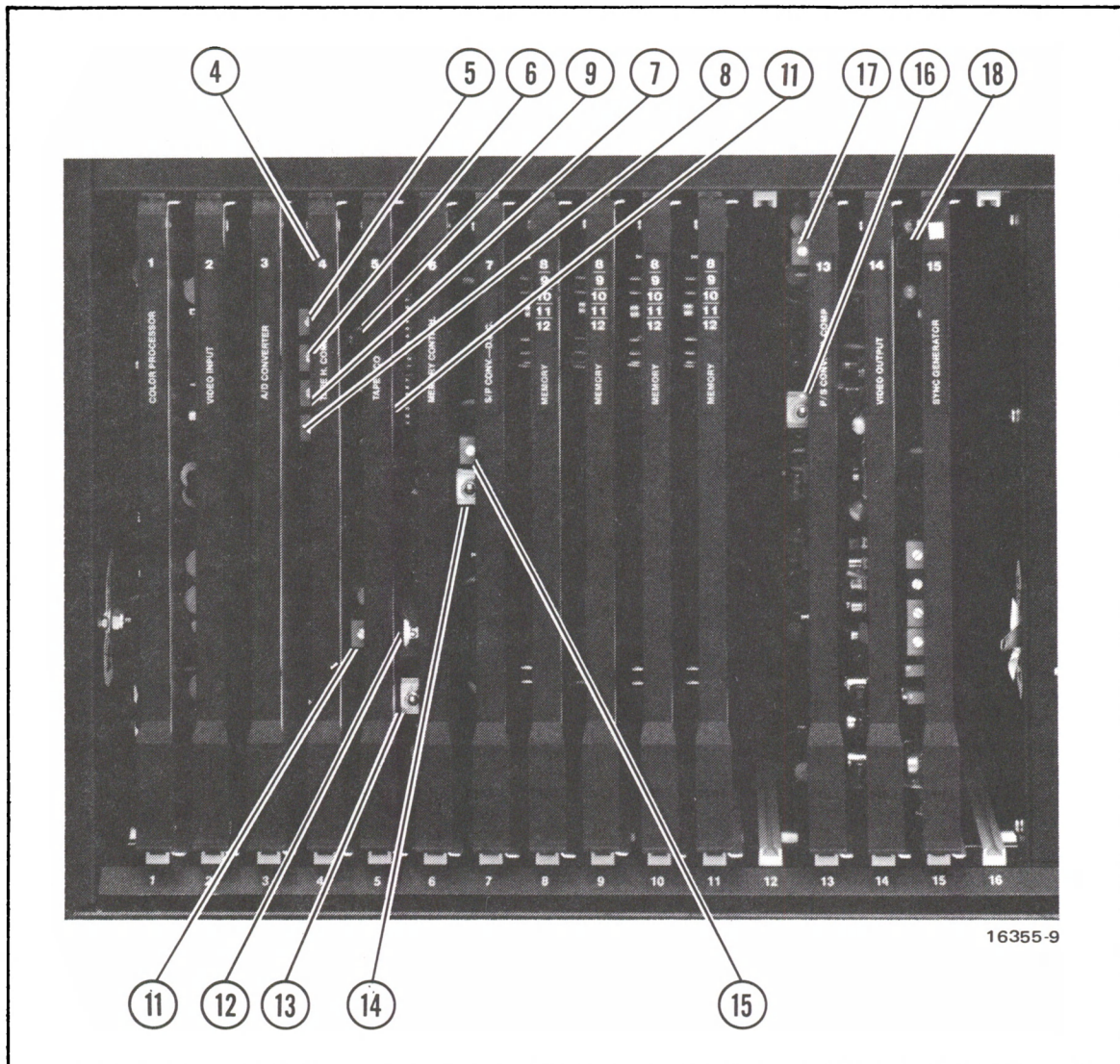
Table 1-2. Operating Controls and Indicators, Card Rack Assembly



Index No.	Name	Function
1	CHROMA LEVEL R22 PWA 1	Adjusts signal level in chroma channel of color processor.
2	LUMIN LEVEL R193 PWA 1	Adjusts signal level in luminance channel of color processor.
3	GAIN R13 PWA 2	Provides ± 2 -dB input video gain adjustment. Adjust control only if VIDEO LOW or VIDEO OVERLOAD indicators are lit. Use control only if input video level cannot be adjusted to correct level by VIDEO LEVEL control.

(Continued next page)

Table 1-2. Operating Controls and Indicators, Card Rack Assembly (Continued)



Index No.	Name	Function
4	BURST/SYNC ϕ R1 PWA 4	Sets a $\pm 40^\circ$ burst/sync phase discriminator window within which instantaneous tape error is corrected.
5	SLO-MO ϕ R170 PWA 4	Sets burst/sync phase in slow motion operation.
6	ϕ COMP CENTER R2 PWA 4	Sets phase comparator centering.

(Continued next page)

Table 1-2. Operating Controls and Indicators, Card Rack Assembly (Continued)

Index No.	Name	Function
7	ϕ MOD GAIN R3 PWA 4	These three controls (index 7, 8, 17) are set at the factory. Do not adjust unless line error circuits on PWA 5 are misadjusted or components are replaced.
8	VEL BAL R4 PWA 4	
(17)	VEL COMP GAIN R1 PWA 13	
9	Shuttle indicator DS1 PWA 5	Indicates Tape VCO is operating in shuttle mode.
10	VERT DELAY R88 PWA 5	Adjusts vertical interval timing when TBC-3 is used with a heterodyne VTR.
11	Centering Indicators PWA 6	Show memory read/write condition. When any of the upper red indicators are lighted, there is a read overload condition. When any of the lower red are lighted there is a write overload condition. The upper green indicator is lighted during normal operation.
12	Horizontal Position S2 PWA	Establishes picture position with respect to sync generator horizontal sync. Each position of switch moves picture an increment of one subcarrier cycle.
13	VERT CTRG/ MEMORY CTRG S1 PWA 6	Selects vertical centering mode for VPR-2B and VPR-3 or memory centering mode for VTRs without capstan servos.
14	ON/OFF (DOC) S1 PWA 7	Enables dropout compensator which replaces all or part of a missing line with video from previous lines.
15	AGC LEVEL R24 PWA 7	Adjusts dropout compensator sensitivity.
16	ON/OFF S1 PWA 13	Enables velocity compensator for line-by-line time-base correction.
17	VEL COMP GAIN R1 PWA 13	See index 7.
18	OUTPUT SYNC/BURST R240 PWA 15	Matches normal RS-170-A output sync/burst phasing to nonstandard video source.

(Continued next page)

TBC-3

Table 1-2. Operating Controls and Indicators, Card Rack Assembly (Continued)

Index No.	Name	Function
19	REF SYNC/BURST DS1 PWA 15 (12-line only)	Indicates proper sync/burst phasing.
20	H-TRAIL R245 PWA 15	Adjusts horizontal blanking pulse trailing edge timing.
21	H-LEAD R46 PWA 115	Adjusts horizontal blanking pulse leading edge timing.
22	NORMAL R64 PWA 15	Adjusts vertical blanking timing for normal operation.

(Continued next page)

Table 1-2. Operating Controls and Indicators, Card Rack Assembly (Continued)

Index No.	Name	Function
23	SLO-MO R65 PWA 15	Adjusts vertical blanking timing for slow-motion operation.
24	CRMA ϕ R146 PWA 15	Adjusts chroma phase for non-standard video sources.
25	SUBC ϕ R208 PWA 15	Adjusts output burst phase with respect to horizontal sync.
26	REF SYNC/BURST (16-line only) DS1 PWA 15	Lights when sync generator has proper color framing.
27	COLOR LOCK (16-line only) DS2 PWA 15	Lights when TBC is genlocked to a color reference source.
28	REF SYNC/BURST R223 PWA 15	Adjusts sync/burst phase discriminator centering.
29	AUTO/OFF/ON (16-line only) S1 PWA 15	In ON position, burst is always present in output signal. In AUTO position, burst is present if burst is present at TAPE VIDEO IN connector. In OFF position, burst is not present in output signal.

Figure 1-3. Detailed PWA Edge-Control and Indicator Description (Sheet 1 of 5)**1 LUMIN LEVEL R193, PWA 1**

Used only in heterodyne or slow motion modes and can be adjusted differently for each mode. See PWA 1 adjustment section.

2 CHROMA LEVEL R22, PWA 1

Used only in heterodyne or slow motion and still modes. Normal mode chroma level is a function of the accuracy of the digital quantization and response characteristics of video signal processing circuits throughout the TBC. It may be adjusted for separate and different level requirements of slow motion and heterodyne circuitry on the color processor. See PWA 1 adjustment procedure.

3 GAIN R13, and Video Low/Overload Indicators, PWA 2

While this video level control provides a ± 2 -dB range of adjustment for special cases in normal applications, it is considered the calibration control for the video low/video overload indicators. The calibration point is given in the PWA 2 adjustment procedure.

4 BURST/SYNC ϕ R1, PWA 4, and Edit Ready Indicator

Control R1 sets a $\pm 40^\circ$ burst/sync phase discriminator window within which instantaneous tape error is corrected. Calibration of this window is indicated by control panel EDIT READY lamp and is calibrated at the factory to an RS170A burst/sync phase on the odd color field. However, any off-tape burst/sync phase can be accommodated by the correction circuitry if R1 is used to turn EDIT READY on for a particular tape or section of tape. On a line-by-line basis, correction may continue even outside the $\pm 40^\circ$ window and within a subcarrier cycle because of the compliance of the circuitry. However, step function errors, which can occur on interchange tapes with noncolor-framed edits or nonstandard burst/sync phase, will cause a step function correction, i.e., a one-subcarrier-cycle shift of H phase. Such a correction is of consequence chiefly on matched cut edits. Any necessity for adjustment of R1 is alleviated in a facility which makes RS170A tapes and uses RS170A reference throughout. Use of R1 is further discussed in paragraph 8-8. Standard RS170A burst/sync phase calibration may be reset through use of an RS170A standard tape or (more accurately) by the adjustment in the PWA 4 procedure for standard window centering.

5 SLO-MO ϕ (Burst/Sync Phase) R170-PWA 4

The same burst/sync phase to which R1 BURST/SYNC ϕ is set can also be tracked in slow motion. Any special circumstances for which R1 is adjusted to non-RS170A standard for normal speed may also force adjustment of R170 as well as R157 and R155 on PWA 4. Adjustment of R170, R157, and R155 should be made as outlined in PWA 4 adjustment section. Note that this is not a recommended practice and should be reserved for the more unusual editing problems. Need for adjustment of R170 is apparent if, in normal play with TAPE/EE set to TAPE and the VTR properly color framed, EDIT READY is on but goes off in the transition to, or during operation in the slow or still modes.

TBC-3

Figure 1-3. Detailed PWA Edge-Control and Indicator Description (Sheet 2 of 5)

6 Φ COMP CENTER R2—PWA 4

The standard setting for R2 is given in the PWA 4 adjustment procedure, and under normal conditions it should not be readjusted. However, some Type C format tapes from VTRs with tape guide height inaccuracy, cause a larger error than the tape H qualification window on PWA 5 (Tape VCO) can tolerate as the head starts onto the tape. The result is that the TBC may select the wrong burst timing for the first three to four lines, creating a horizontal shift of one Fsc cycle. The irregularity is adjusted by shifting the qualified delay (comparator timing) pulse with R2 (PWA 5 TP13—window pulse is TP12) so the pulse is adjusted for the error of the tape rather than centered in the window. Be sure to return to the standard setting for R2 as outlined in PWA 4 adjustment procedures.

7 Φ MOD GAIN R3—PWA 4

See Index No. 13.

8 VEL BAL R4—PWA 4

See Index No. 13.

9 Shuttle VCO DS1 Indicator—PWA 5

Indicates that the Tape VCO and Tape H circuitry are maintaining H and V synchronization for the monochrome picture during high speed shuttle of the VPR.

10 Memory Line Centering Indicators—PWA 6

The indicators show memory read/write condition. For standard play mode operation the lower green LED indicator is on except for an occasional step function correction. The upper green indicator comes on if field sequence is altered. If any of the top red indicators are illuminated, there is a read overload condition. If any of the bottom red indicators are illuminated, there is a write overload condition.

11 Rf Dropout Level R24—PWA 7

Used only for heterodyne VTRs or those which do not supply a TTL dropout pulse (Ampex VPR-2B and VPR-3 supply the TTL dropout pulse) and operate on the received rf level. The dropout sensitivity is adjusted by R24 and is most easily adjusted using the recommended dropout test tape listed in Table 3-1. A procedure is given in the PWA 7 adjustment section for setting the dropout sensitivity when a test tape is not available.

12 DOC ON/OFF S1—PWA 7

Switch S1 enables the dropout compensator option which replaces all or part of a missing line with a luminance and chroma derived from previous line(s).

13 VEL COMP GAIN R1—PWA 13

The Φ MOD GAIN (No. 7) and VEL BAL (No. 8) and VEL COMP GAIN are optimized (the type of VTR is not a factor in the optimization) at the factory using a servo

Figure 1-3. Detailed PWA Edge-Control and Indicator Description (Sheet 3 of 5)

test instrument and should not be adjusted unless line error circuits on Tape H PWA 4 or P/S Converter PWA 13 have been misadjusted or repaired. Use the line error adjustment of paragraph 5-8, if adjustment is necessary.

14 VEL COMP ON/OFF S1—PWA 13

Switch S1 enables velocity compensator. Refer to PWA 13 adjustment section for normal velocity compensator operation.

15 OUTPUT SYNC/BURST R240—PWA 15

The sync/burst phase control is operable *only* with PWA 15 jumper J6 in the non-RS170A B-C position. Adjustment moves the output H-sync phase relative to burst over a range of one subcarrier cycle. The control is used for matching the normal RS170A TBC output sync/burst to any non-RS170A source.

16 REF SYNC/BURST DS1—PWA 15

12-line system -- Indicator lights to indicate proper sync/burst phasing.

16-line system -- Indicator lights when sync generator has proper color framing.

17 COLOR LOCK DS2—PWA 15

16-line system only. Indicator lights when TBC is genlocked to a color reference source.

18 REF SYNC/BURST R223—PWA 15

With RS170A reference input, R223 establishes a discriminator centering which locks the sync generator to burst zero-crossing on the odd field. This is an arbitrary calibration point which establishes the color frame sequence necessary for memory read timing (and by extension, it should be emphasized, successful color-framed edits). The odd field calibration with R223 turns REF SYNC/BURST indicator DS1 on. If the LED is not on (or has been improperly calibrated according to paragraph 3-11), the sync generator color frame will be ambiguous.

19 H-TRAIL R45—PWA 15

and

20 H-LEAD R46—PWA 15

Control R147 is used to adjust back porch blanking between burst and active video. R46 adjusts timing of the horizontal front porch blanking with respect to sync. The horizontal blanking leading/trailing edges are adjusted narrower than the source to prevent widening of the broadcast horizontal blanking interval. The blanking timing is seen in the video output by turning BLACK LEVEL fully clockwise and observing the pedestal. Normal settings for R46 and R45 are given in the Sync Generator PWA 15 adjustment section.

TBC-3

Figure 1-3. Detailed PWA Edge-Control and Indicator Description (Sheet 4 of 5)

21 NORMAL Vertical Blanking R64—PWA 15

and

22 SLO-MO Vertical Blanking R65—PWA 15

NORMAL may be set as far down as line 10 to unblank any V-interval test and control signals, and is usually set for blanking of the line preceding such signals. Because slow motion and still modes of operation ambiguously reproduce odd or even fields, the slow-motion blanking control R65 is set for blanking to end before start of the last line prior to picture video. This blanks the ambiguous test signals which may be displaced a half line. The blanking is seen in the video output by turning BLACK LEVEL fully clockwise and observing that the unblanked lines show a pedestal; blanked lines do not. See the Sync Generator PWA 15 adjustment section.

23 Burst AUTO/ON/OFF S1—PWA 15

Switch S1 controls presence or absence of burst in the output signal. In ON position, burst is always present in output signal. In AUTO, burst is present if it is present at TAPE VIDEO IN connector. In OFF, burst is not present in output signal.

24 CHROMA Φ R146—PWA 15

CHROMA Φ control R146, like subcarrier phase control R208, should not be adjusted with the PWA on the extender board. It is part of the basic TBC reference setup for RS170A input and will not require adjustment in any facility which uses RS170A throughout. For facilities which use a non-RS170A reference sync/burst relationship, the sync/burst calibration routine in the Sync Generator PWA 15 adjustment section outlines the adjustments required to phase the TBC to that nonstandard reference.

25 SUBC Φ R208—PWA 15

While the control panel subcarrier phase control affects the relative phasing of both H-sync and burst, R208 SUBC Φ adjusts the output burst phase only with respect to H-sync. This control is factory-set for RS170A reference input and does not require adjustment in any facility which uses RS170A throughout. For those facilities which use a non-RS170A reference sync/burst relationship, the sync/burst calibration routine in the Sync Generator PWA 15 adjustment section outlines the adjustment of R208 as well as CHROMA Φ R146 and other controls required to phase the TBC to that nonstandard reference. R208 should not be adjusted with the PWA on the extender board.

26 Horizontal Phasing S2—PWA 6

For RS170A standard off-tape video and reference, EDIT READY and the REF SYNC/BURST indicator on PWA 15 will be on, and S2 will normally be centered at number 5. This establishes the picture position (horizontal centering) relative to the Sync Generator PWA H-sync output. Each position of the switch moves the picture an increment of one subcarrier cycle with a two- or three-increment shift

Figure 1-3. Detailed PWA Edge-Control and Indicator Description (Sheet 5 of 5)

in either direction from the number 5 before vertical white edges (invalid data in memory) appear at either side of the screen. This control is part of the H-sync phasing procedure in paragraph 3-12. This procedure should be checked if nonstandard tape or reference burst/sync phase is used.

27 VERT CTRG/MEMORY CTRG S1—PWA 6

The vertical centering position is for Type C format VPR series VTRs (or any machine with sufficiently tight servos to guarantee a nominally consistent advance that is one-half the TBC memory or 5-1/2 lines). Memory-centering is limited to nonservoed capstan heterodyne VTRs or those which do not use advanced sync. In memory centering a read/write overload (refer to the PWA 6 description) may drop a line or add two lines, making the picture move up or down—a function of the loose servos and large errors common to nonservoed capstan heterodyne VTRs—whenever accumulated time-base error demands it. In vertical centering, however, playback vertical and reference vertical are compared and the correction is made.

28 VERT DELAY R88—PWA 5

This control is only used for heterodyne VTRs or any VTR without a sync head, such as the VPR-20. Ampex VPR-1, VPR-2, and VPR-2B machines provide their own vertical blanking dropout pulse. The setting for R88 is determined by the extent of head switching noise in the vertical interval. (Head switching noise beyond line 10 of the vertical interval may cause a step-function error which may interfere with any video information in the vertical interval.) R88 is normally set so that TBC correction begins on the second H-sync pulse following the vertical. An R88 setup procedure is given in the Tape VCO PWA 5 adjustment section. If the necessary setting for R88 goes beyond the second H-sync pulse, a readjustment to the line error circuits (R3 and R4 on PWA 5 and R1 on PWA 13) may be in order.

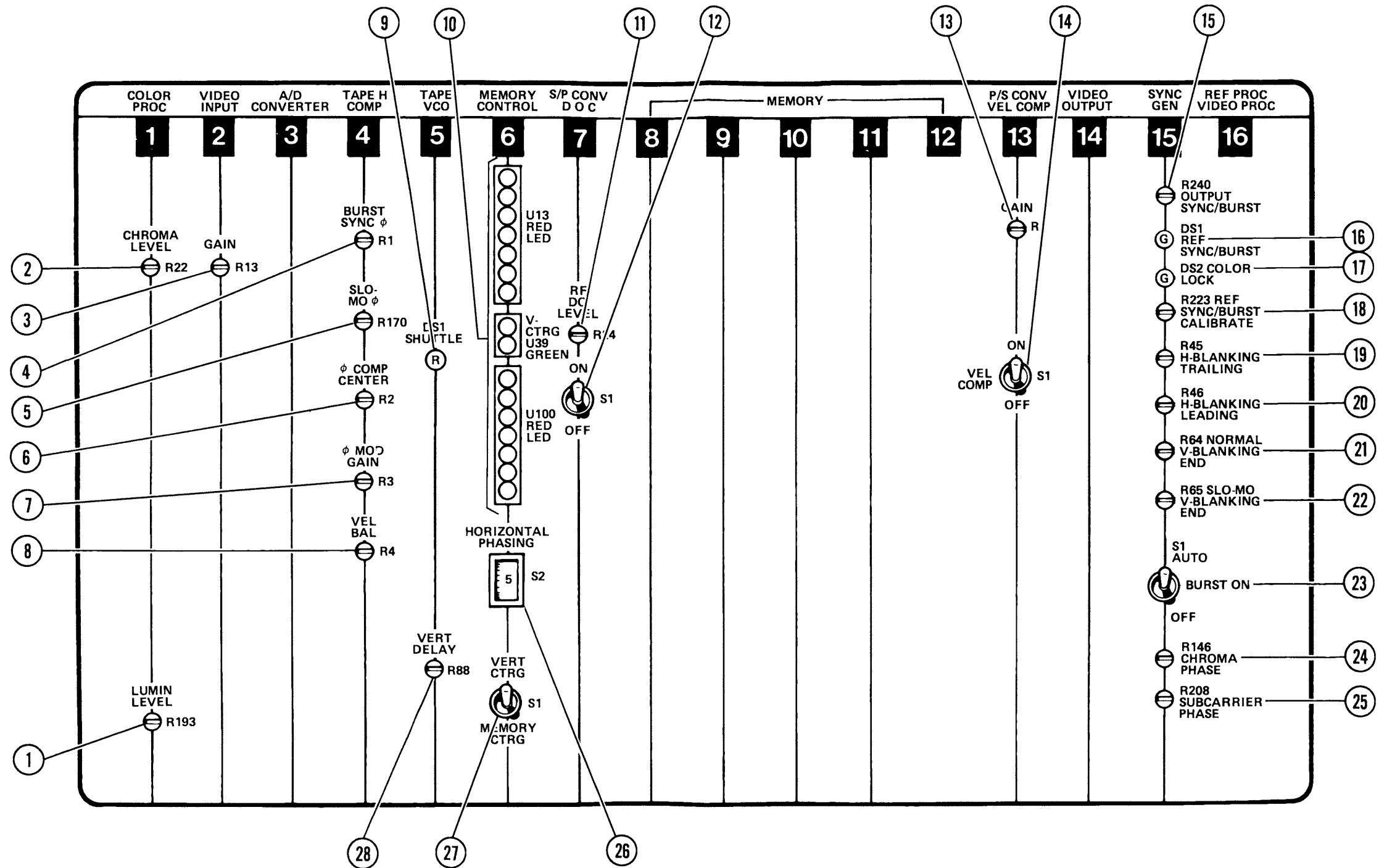


Figure 1-3.
Detailed PWA Edge-Control
and Indicator Description

TBC-3

1-11 TEST AND CONFIGURATION JUMPERS

Many PWAs used in the TBC-3 contain jumpers. A jumper is a link that plugs into the component side of the PWA and electrically connects two points of the PWA circuitry. Some jumpers can be set in two or more positions while others can only be plugged in or removed. They alter circuit operation by including or bypassing portions of PWA circuitry. Many jumpers are used to alter the circuit in order to provide convenient test or alignment configurations of the circuit. Others provide the operator with alternative modes of system operation. Table 1-3 lists all jumpers used in the the TBC-3 PWAs. Various positions in which the jumpers may be placed are given for each. Jumper placement for normal circuit operation is indicated as well as alternative positions.

Before troubleshooting a PWA, check that jumpers are in the desired position.

Table 1-3. Test and Configuration Jumpers

Jumper	Position	Function
PWA 1 Color Processor 1463589		
J1	A-B B-C	Crystal oscillator error Normal Test; fixed error voltage
J2	A-B B-C	Y-axis encoder Normal Test; disabled
J6	A-B B-C	U-axis encoder Normal Test; disables B-Y encoder
J7	A-B B-C	Filter Adjustment Normal Test
J8	A-B B-C	Filter Adjustment Normal Test
J9	A-B B-C	Filter Adjustment Normal Test
J10	A-B B-C	Filter Adjustment Normal Test

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 1 Color Processor 1463589 (Continued)		
J11	A-B B-C	Filter Adjustment Normal Test
J14	A-B B-C	Chroma Inverter Normal Inverter disable
J15	A-B B-C	Filter Adjustment Normal Test
J16	A-B B-C	Filter Adjustment Normal Test
PWA 2 Video Input 1463650		
J1	Removed A-B	Filter Adjustmnet Normal Align filter
J2	A-B Removed	Filter Adjustment Normal Test
J4	A-B Removed	Clamp Normal Defeats clamp
J5	A-B B-C	Ramp Generator Normal Test ramp
J6	A-B B-C	Standards Select NTSC PAL
J7	A-B B-C	Standards Select NTSC PAL

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 2 Video Input 1463650 (Continued)		
J8	A-B Removed	Burst Normal Force monochrome
PWA 3 No Jumpers		
PWA 4 Tape H Comparator 1463568		
J1	A-B B-C	Phase Modulation Normal Test—inserts fixed error voltage
J2	A-B B-C	Edit Ready Loop Test Normal Inserts variable error voltage
J3	B-C A-B	Edit Ready Window Normal; 40° window Approx 10° window
PWA 5 Tape VCO 1463528		
J1	A-B B-C B-D	Normal/Search Internal Search (VPR-2B) External Search (VPR-3) Forces normal oscillator (test)
J2	B-C A-B	Counter Disable Normal x2 disable
J3	A-B Removed	VCO Test Normal Removes error to oscillator
J5	A-B B-C	Factory Test Normal Test
J6	A-B B-C	Two-Wire/Single-Wire Single-wire heterodyne operation Two-wire heterodyne operation

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 5 Tape VCO 1463528 (Continued)		
J7	A-B B-C	Factory Test Normal Test—defeats H-reset
J8	A-B Removed	Factory Test Normal Test—verifies reset qualify counter
J9	A-B B-C	Sync Head Video Processing Normal Disabled
J10	A-B Removed	Factory Test Normal Disables tape vertical-to-vertical display
J11	A-B Removed	Factory Test Normal Disables VTR vertical-to-vertical delay
J12	A-B B-C	VTR Type Select Normal; vertical dropout Front porch vertical dropout
J13	A-B B-C	Down Search VCO Normal Test
J14	A-B B-C	Up Search VCO Normal Test
PWA 6 Memory Control 1463556 (12-line), 1463537 (16-line)		
J1	A-B Removed	+ 2 lines Normal Test; disables + 2 line signal
J2	A-B Removed	Dual Load Normal Disables dual load signal

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 6 Memory Control 1463556 (12-line), 1463537 (16-line) (Continued)		
J3	A-B Removed	-4 lines Normal Test: disables -4 line signal
J4	A-B B-C	Slo-Mo Normal Test: forces slow motion
J6	A-B B-C	Dropout Select Two-line DOC (PAL/SECAM) One-line DOC (NTSC)
J7	A-B Removed	Centering Normal Factory Test only
PWA 7 Serial/Parallel One Line DOC 1463601		
J1	A-B B-C	Factory Test Normal Test Data Disable
J2	A-B A-C	Dropout Select Normal. Inhibits PWA 7 onboard dropout detector. VPR-2B, VPR-3, Heterodyne use. Inhibits VTR dropout command and enables PWA 7 on-board dropout detector. VPR-20 use.
PWA 8 (9, 10, 11) Memory 1463574—no jumpers		
PWA 13 Parallel-to-Serial Converter with Vel Comp 1463531		
J1	A-B B-C	Factory Test Normal Test—forces memory overload condition.
J2	A-B Removed	Second Order Correction Normal Disconnects second-order correction
J3	A-B B-C	Standard Select NTSC PAL/SECAM

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
J4	A-B B-C	Standard Select PAL-M NTSC
J5	A-B B-C	Factory Test Normal Test-inserts fixed error voltage
J6	A-B B-C	12.5 Hz Select PAL/SECAM PAL-M/NTSC
J7 20-line 16-line 12-line	A-B A-B A-C	J7 through J11 are set as shown for each memory size.
J8 20-line 16-line 12-line	A-B A-C A-C	
J9 20-line 16-line 12-line	remove A-B remove	
J10 20-line 16-line 12-line	remove remove A-B	
J11 20-line 16-line 12-line	A-B remove remove	
PWA 14 Video Output 1405189		
J1	RF connector	Factory Test Test only – insert sweep to interpolation filter

(Continued next page)

Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 14 Video Output 1405189 (Continued)		
J2	A-B Removed	Factory Test Normal Test—removes clamp pulse
J3	A-B Removed	Factory Test Normal Test—removes phase equalizer
J4	A-B Removed	Black Clip Normal—black clip on Test— removes black clip
J5	A-B Removed	Composite/Non-Composite Normal—composite sync on VIDEO OUT 2 No composite sync on VIDEO OUT 2
J6	A-B B-C	Factory Test Normal Test—inhibits V-internal clamp
PWA 15 Sync Generator 1463659 (16-line) 1405186 (12-line)		
J1	A-B B-C	VPR/Heterodyne Select Fixed; VPR-2B/VPR-3 Dynamic; heterodyne VTR
J2	A-B B-C B-D B-E	Advanced Reference Select Composite sync (-8V) Composite sync Vertical (-8V) Sync and subcarrier (VPR-3)
J3	A-B B-C B-D B-E	Reference 3.58 MHz Select jumper position as required for correct system operation
J4	A-B B-C B-D B-E	Subcarrier Select jumper position as required for correct system operation

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Table 1-3. Test and Configuration Jumpers (Continued)

Jumper	Position	Function
PWA 15 Sync Generator 1463659 (16-line) 1405186 (12-line) (Continued)		
J5	A-B B-C	H-phase select Select jumper position as required for correct system operation
J6	A-B B-C	RS170A Standard Select RS 170A Standard Non-standard
J7 (16-line sync gen only)	A-B B-C	Mode switch lockout VPR-3 (normal only) VPR-2B (selectable)

PART I

SECTION 2

SYSTEM DESCRIPTION

2-1 INTRODUCTION

This section provides an overview of the TBC-3 Digital Time Base Corrector (NTSC), Ampex Part No. 1463500. More detail on individual printed wiring assemblies (PWAs) is given in Part II of this manual.

2-2 CAUSES OF TIME BASE ERRORS

Time base correction of off-tape video is necessary because of head-to-tape velocity errors in the VTR record and playback processes. Before examining the Ampex TBC-3, a general understanding of the cause of time-base errors and methods of time-base correction is required.

The ideal VTR would play back a video signal identical to the original input signal. To achieve this, the time intervals between any two points on the tape must be identical each time the same piece of tape is moved across the heads by the transport. Thus, playback timing would be identical to input signal timing when the tape was recorded.

This ideal VTR with perfect record and playback timing has yet to be built and such perfection is not likely to be attained in spite of the many advances of design and manufacture. During both record and playback, the video signal suffers a deviation from synchronism with respect to time, resulting in time-base distortions of horizontal sync and burst. In addition, chroma phase relative to the original subcarrier signal may be distorted. Time base errors that produce distortions obvious to the viewer have a bandpass from less than 0.1 Hz to approximately 2 kHz.

Time base errors in the record/playback process are generally caused by instantaneous head-to-tape speed errors. Errors usually originate from the rotating parts of the tape transport. Some errors and their causes are:

- Tape recorded at one temperature/humidity level and played back at another stretches and shrinks, compounding the time-base errors.
- Transfer error introduced when a tape is recorded on one VTR and played back on another VTR.
- Mechanical error caused by friction of the air film between scanner and tape. This includes nonlinear thickness of the air bearing and drag of the rough tape surface.

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- Long-term errors caused by the capstan drive and reel mechanism, and by temperature/humidity changes. Somewhat shorter-term errors occur in the scanner mechanism and the tape-to-scanner interface.
- Line-to-line errors caused by lateral motion of the tape and variations in the intimacy of head-tape contact.
- Impact errors resulting from entrance and exit of heads into the tape on the scanner. These are slope function errors from beginning to end of a horizontal line of video and are referred to as velocity errors.
- Intermittent errors caused by a combination of static and friction. An electrostatic charge can build up on the surface of the tape as it moves over metal parts of the transport. Friction of the heads on the scanner moving opposite to the direction of tape travel causes drag. These factors, as well as other sources of static and friction, can combine to cause an accumulation of forces which resulting in a temporary slowing of the rate of tape movement.

2-3 SYSTEM DESCRIPTION

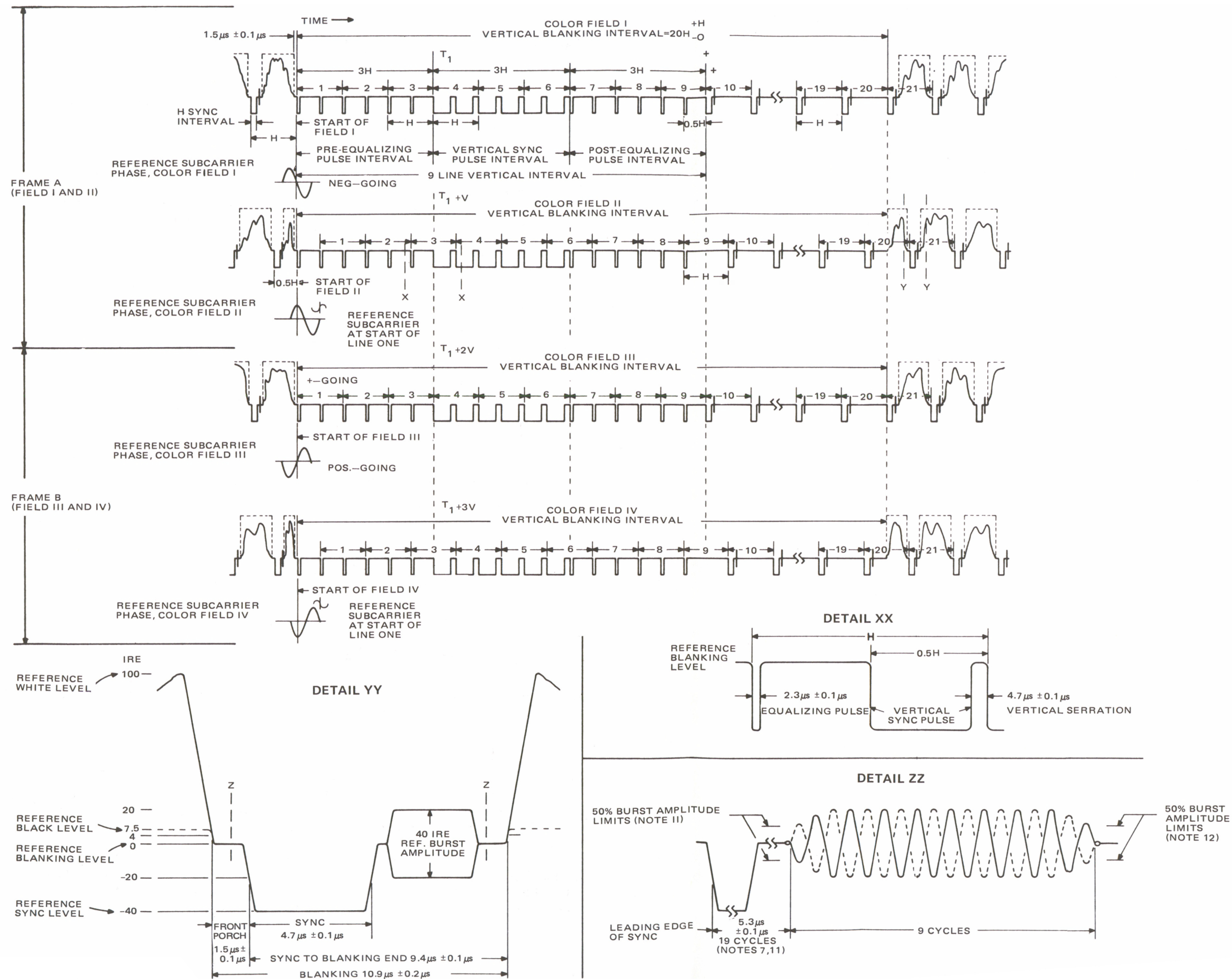
Note

The following discussion pertains first to the 12-line memory version of the TBC-3. Information pertaining to the 16-line version is immediately shown in parenthesis.

The TBC-3 provides time-base error correction for nonsegmented helical-scan videotape recorders, including VPR-2B and VPR-3. The TBC-3 corrects errors in a range up to 10 (14) horizontal lines to within 3 ns in the NTSC standard. Correction is within 20 ns in monochrome. The TBC-3 also processes still and slow-motion playback from the VPR-2B and VPR-3 videotape recorders. When used with the Ampex VPR series production recorders, the TBC-3 produces monochrome pictures at all shuttle speeds, as well as broadcast-quality color pictures from three times normal reverse slow motion, through still frame, to three times normal play speed.

Enhanced performance of video equipment using digital techniques for switching and matched-cut editing requires exact sync and video timing. EIA standard RS170A, illustrated in Figure 2-1, is the basis of performance for the TBC. The definitions in the standard for sync/burst phase and color field are particularly relevant for an understanding of TBC functions. Reference throughout the manual to standard levels, timing, or color frame, relates to the RS170A definitions of the NTSC video signal.

The TBC-3 contains input processing, storage, output processing, and timing circuits, all located on printed wiring assemblies. The input processing circuits are located on the Color Processor PWA 1, Video Input PWA 2, Analog-to-Digital Converter PWA 3, and Serial/Parallel One-Line DOC PWA 7. Storage circuits are located on the three (12-line) or four (16-line) PWAs (PWA 8, 9, 10 and 11). The output processing circuits are located on the Parallel/Serial with Vel Comp PWA 13 and the Video Output PWA 14. Timing and control circuits for time base correction are located on the Tape H Comparator PWA 4, Tape VCO PWA 5, Memory Control PWA 6, and Sync Generator PWA 15.



Notes

- Specifications apply to studio facilities. Common carrier, studio-to-transmitter, and transmitter characteristics are not included.
- All tolerances and limits shown in this drawing permissible only for long time variations.
- The burst frequency shall be 3.579545 MHz.
- The horizontal scanning frequency shall be 2/455 times the burst frequency.
- The vertical scanning frequency shall be 2/525 times the horizontal scanning frequency.
- Start of color fields I and III is defined by a whole line between the first equalizing pulse and the preceding H-sync pulse. Start of color fields II and IV is defined by a half line between the first equalizing pulse and the preceding H-sync pulse. Color field I: that field with negative-going zero-crossing of reference subcarrier nominally coincident with the 50% amplitude point of the leading edges of odd numbered horizontal sync pulses.
- It is recommended that the relationship between sync and reference subcarrier, as defined in note 6 for color field, be uniformly maintained within a tolerance of $\pm 40^\circ$ of reference subcarrier.
- All rise times and decay times, unless otherwise specified, are to $0.14 \pm 0.02 \mu$ s measured from 10% to 90% amplitude points. All pulse widths are measured at 50% amplitude points, unless otherwise specified.
- Overshoot on all pulses during sync and blanking, vertical and horizontal, shall not exceed 2 IRE. Extraneous signals during blanking intervals, including residual subcarrier, shall not exceed 2 IRE, measured over a bandwidth of 8 MHz.
- Burst envelope rise time is $0.30 \pm 0.1 \mu$ s measured between the 10% and 90% amplitude points.
- The start of burst is defined by the zero-crossing (positive or negative slope) that precedes the first half cycle of subcarrier that is 50% or greater of the burst amplitude.
- The end of burst is defined by the zero-crossing (positive or negative slope) that follows the last half cycle of subcarrier that is 50% or greater of the burst amplitude.
- Monochrome signals shall be in accordance with this drawing except that burst is omitted, and fields III and IV are identical to fields I and II respectively.
- Reference subcarrier is a continuous signal which has the same instantaneous phase as burst.

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Figure 2-2 is a simplified block diagram showing the functional relationship of the PWAs that comprise the system.

2-4 Time Base Error Correction

Time base error correction is accomplished by timing the input processing circuits synchronous with off-tape video and timing the output processing circuits synchronous with station reference video. Storage circuits (Memory PWAs) store the data to compensate for the timing disparity between the input and output processing circuits. Timing circuits generate tape and reference-synchronous timing.

In the NTSC standard, tape and reference timing is derived from subcarrier or burst. Timing circuits generate the basic clock signal at the subcarrier frequency (3.58 MHz) and the 3X clock signal at 10.7 MHz.

Time base errors can be corrected by

- digitizing off-tape video into a binary representation of the video instantaneous voltage level at 3X clock rate,
- storing quantized data in memory synchronous with tape timing,
- reading data out of memory synchronous with reference timing, and
- converting binary data back to an analog signal.

Each binary representation consists of an eight-bit data word which corresponds to the voltage level of the associated video sample. Video is sampled at a 3x clock rate. Eight-bit data words are combined in groups of three consecutive words to form a single 24-bit word. The 24-bit word is stored in memory at the basic clock rate.

2-5 Signal Interconnections and Description

For more detailed functional interrelationships among PWAs, refer to the expanded system block diagram shown in Figure 2-3. A signal glossary is given in Table 2-1. This table describes each PWA edge connector signal and gives its destination.

2-6 PWA Functions

The rate at which digital video is clocked into memory follows off-tape sync rate. Time-base nonlinearities that may have accrued during the record-play process are duplicated by the clock that stores digital video in memory (write clock). Faster off-tape video rates result in faster rates of storage of digital video. Slower rates result in slower storage rates. Digitized video is read out of storage at a constant rate, without time-base errors, by the read clock. The velocity compensator circuit on the Parallel/Serial Converter w/Vel Comp PWA 13 modulates the read clock to minimize short-term time-base errors occurring between sync pulses. The read clock is generated by a crystal oscillator in the Sync Generator PWA.

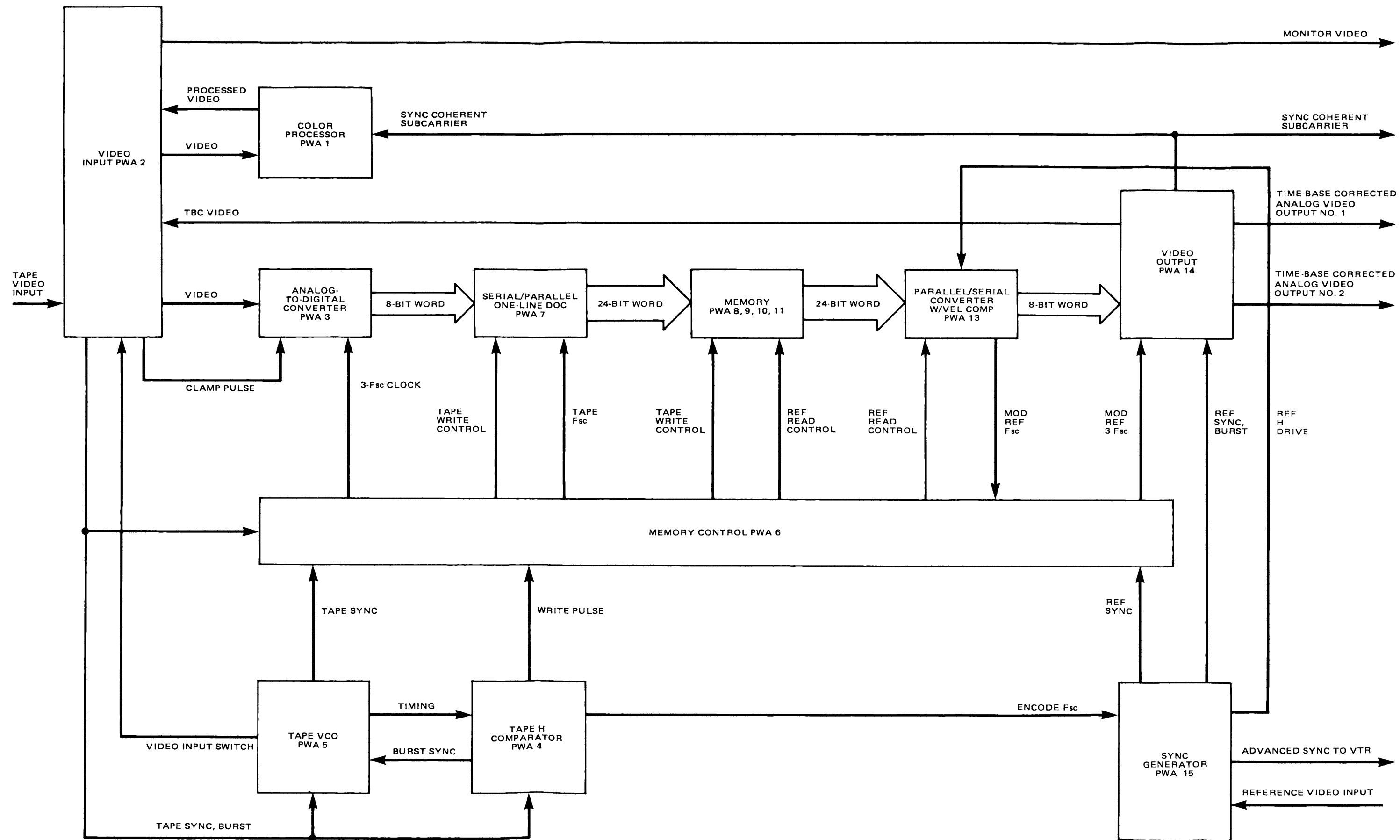


Figure 2-2.
TBC-3 System Simplified Block Diagram

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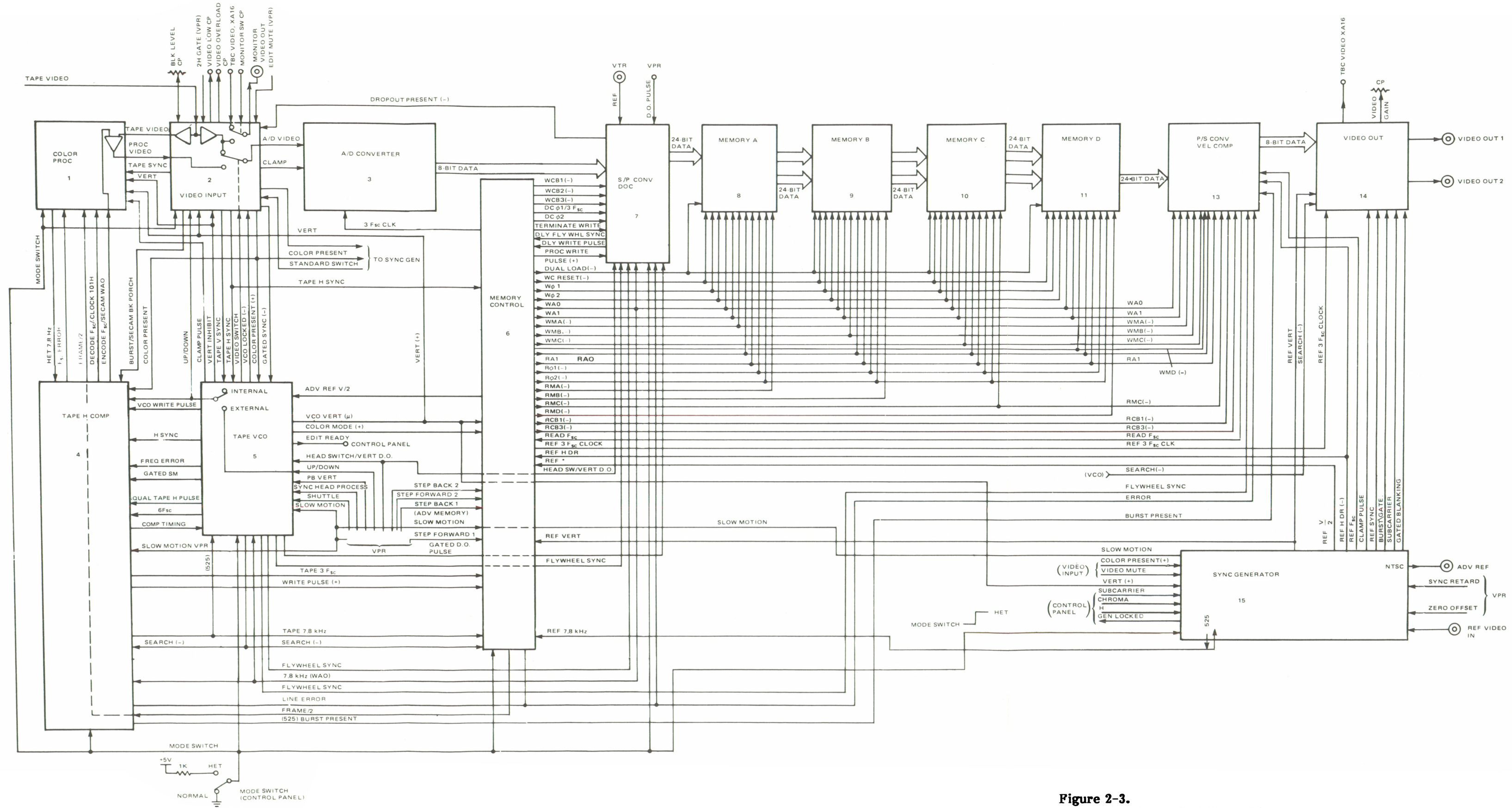


Figure 2-3.
TBC-3 NTSC Detailed Block Diagram

The Color Processor PWA 1 permits the TBC to be used with the VPR series in slow-motion mode and also allows the TBC to be used with a heterodyne-type color VTR. In single-wire heterodyne mode, tape video and sync are supplied to the Color Processor PWA 1 from the Video Input PWA 2 (see Figure 2-2). The color processor strips nonsync-coherent chroma information from video and demodulates it. Demodulation is effected by using a chroma-coherent subcarrier derived by the Color Processor PWA 1 from tape burst. Chroma information is added to luminance in the video after remodulation using a sync-coherent subcarrier developed by the Tape H PWA 4. Processed video is then routed back to the Video Input PWA 1 which supplies video to the A/D Converter PWA 3. Processed video is also supplied to the MONITOR VIDEO OUT connector on the connector panel. The Color Processor PWA 1 is also used with still and slow-motion modes of operation and provides the 180° phase alternation of chrominance information at the correct color frame phase sequence and returns the processed video to the Video Input PWA 2.

Off-tape video is received by the Video Input PWA 2, which clamps and amplifies the signal, switches the signal through the Color Processor PWA 1, switches off-tape or TBC video to the monitor video output, and strips color and sync information from the off-tape video signal for use by the timing circuits. The Video Input PWA also provides input video level monitoring with video high/low warning indicators on the VPR-2B or VPR-3 console control panel. In addition, the PWA (Assembly No. 1463650) contains a color/monochrome sensing circuit and a jumper-selected test ramp generator circuit that exercises the video path of the TBC for test and maintenance purposes.

The A/D Converter PWA 3 quantizes off-tape video into a binary representation of instantaneous video voltage level at a conversion rate of 3Fsc (three times the 3.58 MHz subcarrier or 10.7 MHz). Each binary representation consists of an 8-bit data word. Serial/Parallel One-Line DOC PWA 7 combines the 8-bit data words into groups of three consecutive words and from them produces a single 24-bit word. The 24-bit word is stored in the 12-line (16-line) memory at the basic clock rate of 3.58 MHz (one-third the A/D conversion rate). Each 24-bit word defines a single cycle (279 ns) of subcarrier.

A one-line dropout compensator is provided on the Serial/Parallel One-Line DOC PWA 7. The one-line dropout compensator manipulates 8-bit data to supply replacement video which is a composite of chroma from two lines previous and luminance from the previous line. Dropout compensation is accomplished by blanking the faulty video signal and recirculating the output of the compensator which corresponds to correctly color-phased data. This replaces the current data (dropout) from the A/D converters during the time that a dropout is detected. Dropouts are identified by a TTL dropout signal originating in the VPR or a loss of rf signal from the VTR.

The 24-bit words from PWA 7 are written into memory line-by-line synchronous with tape timing and are read out of memory line-by-line synchronous with reference timing. The 24-bit words from memory are converted back to 8-bit data words corresponding to the original video samples by the Parallel/Serial Converter with Vel Comp PWA 13.

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The velocity compensator circuitry is located on Parallel/Serial Converter w/Vel Comp PWA 13. Velocity errors, or short-term time-base errors that occur during each video line, produce an apparent hue shift during the line period. The velocity compensator corrects this effect by modulating the time-base of the memory read clock in the direction and by the amount that is counter to the velocity error.

In the Video Output PWA 14, 8-bit words are converted back to an analog signal which, together with inserted sync burst and blanking information supplied by the Sync Generator PWA 15, provides output video from the TBC.

The memory stores 12 or 16 lines of video (four lines in each of three or four Memory PWAs). When there are no time-base errors, a line of video is read out of memory six (eight) lines after it has been written into memory and memory is said to be centered. When, because of time-base errors, video is read in faster than it is read out, readout of a line may occur from 8 to 12 (10 to 16) lines after it has been read in. Continuing high rates of writing into memory cause memory capacity to be exceeded—a condition called write overload. Time base errors that cause video to be read in slower than it is read out, result in the readout of a line occurring only one to seven lines after it has been read in. Continuing slow writing rates cause the read memory selection circuits to try to access the same line of memory that is being accessed by the write memory selection circuits—a condition called read overload. Read or write overloads may result in picture breakup.

Ampex VPR series video production recorders have a preset line-advance of off-tape video with respect to the memory read function of the TBC. Logic in the Memory Control PWA 6 maintains this relationship regardless of fluctuations of tape speed. The Sync Generator PWA 15 provides an advanced sync signal to establish line-advance for VTRs that do not have an internal advance circuit.

Memory access signals are also generated by the Memory Control PWA 6. This PWA centers memory read-write timing after the occurrence of time-base disturbances to ensure that memory buffering capability is optimized. Accessing signals for the memory write process, which are generated by the Memory Control PWA, are initiated by the Tape H and Tape VCO PWAs. Access signals for the memory read process are initiated by the Sync Generator PWA 15.

Operating together, Tape H Comparator PWA 4 and Tape VCO PWA 5, produce the clock and clocking signals required by the Memory Control PWA to generate memory write signals. Off-tape sync and burst signals, provided by the Video Input PWA 2, phase-lock an oscillator that develops the $3F_{sc}$ clock signal used by the A/D Converter and Memory Control PWAs. In this way, the rate of conversion of video into digital, and loading of data into memory, are functions of tape speed. In addition, the Tape H PWA 4 produces a line-by-line velocity error measurement signal which it sends to velocity compensator circuits on the Parallel/Serial Converter PWA 13. The velocity compensator stores the error signal and uses it to produce the modulated read F_{sc} signal that reduces velocity error.

Table 2-1. PWA Edge Connector Signal Description

Signal	From	To	Purpose
1/2 line (gated slow motion)	Tape VCO PWA 5, pin 27	Tape H Comparator PWA 4, pin 28	Sets registers at half-line time to prepare for action on next line. Equivalent to tape sync delayed 32 #s.
2H gate	VPR J11-U	Video Input PWA 2, pin 87	Inhibits half-line pulses in vertical interval.
3Fsc	Memory Control PWA 6, pin 65	A/D Converter PWA 3, pin 63, 64	Derived from Tape H Comparator PWA. 10.74-MHz clock for A/D converter integrated circuit.
6Fsc	Tape VCO PWA 5, pin 13, 14	Tape H Comparator PWA 4, pin 13, 14	VCO clock rate used to reclock timing signals to maintain precision.
A/D clamp (-)	Video Input PWA 2, pin 51, 52	A/D Converter PWA 3, pin 33, 34	Triggers sync clamp in A/D input amplifier. Clamp level is negative 2V.
Advanced reference	Sync Generator PWA 15, pin 37	Rear panel J8	Advanced reference to external VTR. Jumper selectable—vertical drive, composite sync, or composite video.
Advanced reference V/2	Memory Control PWA 6, pin 55	Tape VCO PWA 5, pin 58	Derived from reference V/2 (sync generator). Establishes odd field of studio reference video. Programs encode divider.
Black level control	Control panel P14-1	Video Input PWA 2, pin 64	Permits operator control of black level in blanking interval.
Burst	Video Input PWA 2, pin 67, 68	Tape H Comparator PWA 4, pin 69	Provides sync-coherent burst crossing to 6Fsc VCO oscillator via burst present detector, burst crossing detector.
Burst 3.58 MHz	Sync Generator PWA 15, pin 75, 76	Video Output PWA 14, pin 75, 76	Burst signal inserted in output video signal of TBC.
Burst flag	Sync generator PWA 15, pin 45	Video Output PWA 14, pin 45, 46	Keys burst in composite video out.
Chroma phase	Control panel P14-8	Sync Generator PWA 15, pin 29, 30	Operator control of reference 3.58-MHz phase.
Clamp	Tape VCO PWA 5, pin 56	Color Processor PWA 1, pin 47, 48	Clamp pulse to output video amplifier of Color Processor PWA.
Clamp pulse (-)	Sync Generator PWA 15, pin 41	Video Output PWA 14, pin 43, 44	Sample pulses for dc restorations after D/A converter.
Color present	Video Input PWA 4, pin 83	Tape H Comparator PWA 2, pin 88	Inhibits edit ready lamp in monochrome, operates sync select in phase error detector, replaces error voltage with fixed value.
COMP blank (-)	Sync Generator PWA 15, pin 71, 72	Tape VCO PWA 5, pin 83	Input to video in switch circuit, input to selected tape VCO sync selector.
		Sync Generator PWA 15, pin 81	Inhibits burst flag to Video Output PWA when color not present.
		Video Output PWA 14, pin 72	Puts fixed binary number to filter/amplifier during horizontal and vertical blanking.

(Continued next page)

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Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
COMP sync (-)	Sync Generator PWA 15, pin 49	Video Output PWA 14, pin 49, 50	Composite sync added to TBC output video signal.
COMP timing	Tape H Comparator PWA 4, pin 26	Tape VCO PWA 5, pin 25	Modified burst crossing used to lock 6Fsc VCO.
Data out (bits 1-8)	A/D Converter PWA 3, pin 37 to 52	S/P Converter PWA 7, pin 38, 40, 42, 44, 46, 48, 50, 52	Digitized sample of video coded as an 8-binary word.
Data out (bits 1-24)	S/P Converter PWA 7, pins 59-82 (bit 1 is pin 82)	Memory PWAs 8, 9, 10, 11, 12 pins 59-82 (bit 1 is pin 81)	24 parallel bits representing three 8-bit video words data input bus.
Data out (bits 1-24)	Memory PWAs 8, 9, 10, 11, 12, pins 33-56 (bit 1 is pin 33)	P/S Converter PWA 13, pin 33-56 (bit 1 is pin 34)	24 parallel bits representing three 8-bit video words. Data output bus.
Data out (bits 1-8)	P/S Converter PWA 13, pin 16, 18, 20, 22, 24, 26, 28, 30	Video output PWA 14, pins 15-30	8-bit parallel video word.
DC ϕ 1, DC ϕ 2	Memory Control PWA 6, pin 57, 58	S/P Converter PWA 7 pin 57, 58	Two-phase memory shift clock.
Delayed flywheel sync	S/P Converter PWA 7, pin 45	Memory Control PWA 6, pin 46	Wired straight through the S/P Converter PWA. (See flywheel sync.)
Delayed sync	Tape VCO PWA 5, pin 31	Tape H Comparator PWA 4, pin 32	H-rate clock for Fsc error signal ramp generator.
Delayed write Pulse (+)	S/P Converter PWA 7, pin 43	Memory control PWA 6, pin 44	Starts write function in main memory.
Dropout present	S/P Converter PWA 7, pin 55	Video Input PWA 2, pin 33	Inhibits one-shots during dropout.
Dual load (-)	Memory Control PWA 6, pin 14	Memory PWA 8, 9, 10, 11, 12, pin 13, 14	Accesses two lines of memory to be simultaneously loaded during memory overload correction.
Edit mute	VPR J11-N	Video Input PWA 2, pin 63	VPR edit accessory blanks video at Video Output PWA during edit.
Edit ready	Tape H Comparator PWA 4, pin 29	Control panel P14-11	Indicates TBC is locked to burst crossing within acceptable limits.
Encode Fsc	Tape H Com- parator PWA 4, pin 75, 76	Color Processor PWA 1, pin 71, 72	Sync coherent subcarrier used to re-encode the chroma signal in slow motion operation.
Fast shuttle	VPR J11-L	Tape VCO, PWA 5, pin 74	VPR control of search.
Flywheel sync	Tape VCO PWA 5, pin 49, 50	S/P Converter PWA 8, pin 49	VCO derived H-sync. Wired straight through S/P Converter PWA. (See delayed flywheel sync.)

(Continued next page)

Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
Flywheel sync	Tape VCO, PWA 5 pin 84	P/S converter PWA 13, pin 84	Initiates line-by-line velocity error digital storage in vel-comp.
Frame/2	Memory Control PWA 7, pin 16	Color Processor PWA 1, pin 27, 28	Controls phase reversal of chroma field-to-field in slow motion operation.
Frequency error	Tape VCO PWA 6, pin 79, 80	Tape H Comparator PWA 5, pin 80	Modulates encode Fsc (Color Processor PWA) with VCO component of tape time-base error.
Gated DO pulse	Tape VCO PWA 5, pin 75	Serial-to-Parallel PWA 7, pin 56	TTL level dropout pulse from VPR. Inhibited during format dropout.
Gated sync	Video Input PWA 2, pin 35, 36	Tape VCO PWA 5, pin 30	Operates sample pulse former, search 6Fsc oscillator, phase comparator.
Genlocked	Sync Generator PWA 15, pin 33, 34	Control panel; P14-10	Lamp indication that TBC is locked to reference sync.
H-sync	Tape VCO PWA 5, pin 26	Tape H Comparator PWA 4, pin 25	Enables burst present and burst crossing detectors.
Head switch/-vertical dropout	VPR J11-R	S/P Converter PWA 8, pin 53, 54 Tape VCO PWA 6, pin 69, 70	VPR dropout signal during vertical blanking interval, activates dropout present generator. If sync head installed, time sync head video being processed.
HET/normal (mode switch)	Control panel P14-6	Video Input PWA 3, pin 47 Color Processor PWA 1, pin 17, 18 Tape H Comparator PWA 4, pin 22 Tape VCO PWA 5, pin 21, 22 Memory Control PWA 6, pin 41 S/P Converter PWA 7, pin 31, 32 Sync Generator PWA 15, pin 32	Changes circuits to conform to requirements of operation with a heterodyne VTR.
Heterodyne video	Video Input PWA 2, pin 21, 22	Color Processor PWA 1, pin 21, 22	Off-tape video to Color Processor PWA in heterodyne or slow motion operation.
Horizontal phase (coarse) subcarrier phase (fine)	Control panel P14-5	Sync Generator PWA 15, pin 21	Operator control of sync-to-burst crossing phase adjustment.
Line error	Tape H Comparator PWA 4, pin 79	P/S Converter PWA 13	Velocity error signal to velocity compensation option circuits.
Mode switch	Control panel P14-6	Tape VCO, PWA 5, pin 21, 22	Controls heterodyne or normal operation of TBC. (See HET/normal.)

(Continued next page)

Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
Monitor switch	Control panel P14-7	Video Input PWA 2, pin 34	Selects tape video or TBC output video for monitor output.
Monitor video out	Video input PWA 2, pin 37	Rear panel, J7	Processed or tape video to color monitor.
Processed video	Color Processor PWA 1, pin 81, 82	Video Input PWA 2, pin 81, 82	Processed video in heterodyne operation.
Processed write pulse (+)	Memory Control PWA 6, pin 51, 52	Serial-to-Parallel Converter PWA 7, pin 51	Starts write function in DOC memory.
Qualified tape H pulse	Tape VCO PWA 5, pin 59	Tape H Comparator PWA 4 pin 60	Senses whether VCO is locked to off-tape burst crossing.
RF in	Rear panel, J4	S/P Converter, PWA 7, pin 33, 34	Off-tape RF to dropout detector. Used when TTL dropout not available.
R ϕ 1, R ϕ 2 (-)	Memory Control PWA 7, pin 26, 29	Memory PWAs 9, 10, 11, 12, pin 26, 27	Memory read clock.
RA0, RA1	Memory Control PWA 7, pin 30, 32	Memory PWAs 9, 10, 11, 12, pin 30, 29 P/S Converter, PWA 13, pins 25, 23	Memory line select, part of read address.
RCB1, RCB3	Memory Control PWA 7, pin 34, 36	P/S Converter, PWA 13, pin 27, 29	Latch and multiplexer clock for 24-bit to 8-bit conversion.
Read Fsc	P/S Converter, PWA 13, pin 75, 76	Memory Control PWA 6, pin 82	Velocity compensation modulated reference Fsc from Sync Generator PWA. Drives read 3Fsc clock.
Reference 3Fsc Clock	Memory Control PWA 7, pin 75, 76	Video Output PWA 14, pin 33, 34	Reclocking of read time to ensure precision.
Reference 3.58 MHz	Sync Generator PWA pin 79, 80	P/S Converter PWA 13, pin 79, 80	Velocity compensation clock.
Reference H-drive	Sync Generator PWA 15, pin 50	Memory Control PWA 6, pin 72 P/S Converter PWA 13, pin 63, 64	H-sync phase locked to studio reference video. Starts memory read cycle, generates read addresses.
Ref vertical	Sync Generator PWA 15, pin 69, 70	Memory Control PWA 6, pin 68	Enables delete 2 (or 3) lines circuit in slow operation.
RMA, RMB, RMC	Memory Control PWA 6, pin 25, 27, and 28	Memory PWA 8, 9, 10, 11 and 12, pin 25, 27 and 28	Board select, part of read memory address.
Search (-)	Tape VCO PWA 5, pin 72	Tape H Comparator PWA 4, pin 72 Memory Control PWA 6, pin 67 Video Output PWA 14, pin 69, 70	Changes circuits to conform to requirements of shuttle operation.

(Continued next page)

Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
Slow motion	VPR J11-P	Tape H Comparator PWA 4, pin 35 Tape VCO, PWA 5, pin 36 Memory Control PWA 6, pin 39 Sync Generator PWA 15, pin 22	Changes circuits to conform to requirements of slow motion operation.
Slow motion pulse	Memory Control PWA 7, pin 13	Tape VCO PWA 6, pin 18	
Step back 1	VPR, J11-A	Memory Control PWA 6, pin 69	Moves write pointer on memory control 2 or 3 lines back.
Step back 2	VPR J11-B	Memory Control PWA 6, pin 87	Moves write pointer on memory control 4 or 5 lines back.
Step forward 1	VPR, J11-JJ	Memory Control PWA 6, pin 88	Moves write pointer on memory control 2 or 3 lines forward.
Step forward 2	VPR, J11-E	Memory Control PWA 6, pin 81	Moves write pointer on memory control 4 or 5 lines forward.
Sync coherent subcarrier out	Color Processor PWA 1, pin 59, 60	Rear panel, J5	Used in 2-wire heterodyne VTR operation.
Sync head process	VPR, J11-EE	Tape VCO PWA 5, pin 73	Permits Tape VCO PWA to process sync head signals if sync head is installed.
Sync retard	VPR, J11-F	Sync Generator PWA 15, pin 63, 64	VPR control to compensate for VPR video timing. Shifts output vertical timing 1/3 of a field.
Sync terminate	Video Input PWA 2, pin 32	Tape VCO PWA 5, pin 29	Prevent half-frequency lockup of search VCOs
Tape 3Fsc	Tape H Comparator PWA 4, pin 64	Memory Control PWA 6, pin 63	Clock for write functions, A/D memories.
Tape 7.8 kHz	Tape H Comparator PWA 4, pin 33	Memory Control PWA 6, pin 35	Clocked by gated half-line, reset by 7.8 kHz reset-clocks WA0, WA1.
Tape video input	VPR J3 via motherboard jumper J1	Video Input PWA 2, pin 15, 16	Signal to be time-base corrected.
Tape sync	Video Input PWA 2, pin 5, 54	Color Processor PWA 1, pin 49, 50	Triggers sampling gates.
Tape V sync	Video Input PWA 2, pin 58	Tape VCO PWA 6, pin 57	Vertical reference from tape.
TBC video	Video Output PWA 14 via pin 53, 54 and J1 to slot-16 via pin 59, 60	Video Input PWA 2 IN pin 25, 26 OUT pin 43, 44 to J7	Provides video for studio monitor.
TTL dropout	VPR, J11-V	Tape VCO PWA 8, pin 76	Input to dropout present generator.
VCO write pulse	Tape VCO PWA 5, pin 23	Tape H Comparator PWA 4, pin 24	Start with write function to be line-by-line corrected.

(Continued next page)

Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
Vel-comp process	Tape H Comparator PWA 4, pin 18	Tape VCO PWA 5, pin 19 P/S Converter PWA 13, pin 59, 60	Enables previous line velocity error to be used when burst missing because of Bruch blanking.
Vertical inhibit	Tape VCO PWA 5, pin 24	Tape H Comparator PWA 5, pin 23	Inhibits 7.8 kHz reset and burst/sync ϕ detector in vertical interval.
Vertical inhibit	Tape VCO PWA 5, pin 55	Video Input PWA 2, pin 55, 56 Color Processor PWA 2, pin 53, 54	Inhibit pulse formers of blanking and sync level sample-and-hold.
Vertical out (VCO vertical)	Tape VCO PWA 5, pin 32	Video Input PWA 2, pin 57 Memory Control PWA 6, pin 33 Sync Generator PWA 15, pin 82 Reference Processor PWA 16, pin 74	Inhibits clamp. Derived from playback vertical. Clock for odd/even field circuit. Tie point. Input to vertical phase detector in nonservoed capstan operation.
V/2(+)	Sync Generator PWA 15, pin 38	Memory Control PWA 7, pin 71	Defines odd number fields of color frame.
Video	Video Input PWA 2, pin 78	A/D Converter PWA 3, pin 77, 78	Off-tape video to A/D Converter PWA.
Video gain	Control panel P14-2	Video Output PWA 14, pin 39, 40	Operator control of gain of digital-to-analog converter output.
Video in	Rear panel J1, J2	Sync Generator PWA 15, pin 15, 16 Video Processor PWA 16, pin 15, 16	Composite video master reference sync in.
Video low	Video Input PWA 2, pin 49	Control panel P14-3	Indicates below standard input video sync level.
Video mute	Video Input PWA 2, pin 31	Video Processor PWA 16, pin 27 Sync Processor PWA 15, pin 25	Tie point. Locks blanking signal to kill video output if no video input.
Video out	Color Processor PWA 1, pin 81, 82	Video Input PWA 3, pin 81, 82	Processed color video returned to the Video Input PWA.
Video out no. 1	Video Output PWA 14, pin 59, 60	J9 rear panel	TBC video output.
Video out no. 2	Video output PWA 14, pin 65, 66	J10 rear panel	TBC video output. Jumper selectable noncomposite or composite.
Video overload	Video Input PWA 2, pin 50	Control panel P14-4	Drives indicator lamp—indicates abnormal video amplitude condition.
VPR up/down	J11-Y	Tape VCO PWA 5, pin 20	VPR control selection of search up/down VCO in normal operation. Selected by PWA 7, J5.

(Continued next page)

Table 2-1. PWA Edge Connector Signal Description (Continued)

Signal	From	To	Purpose
Video switch	Tape VCO PWA 5, pin 47	Video Input PWA 2, pin 48	Select processed video from color processor in heterodyne mode or VPR slow-motion.
$W_{\phi 1}$, $W_{\phi 2}$	Memory Control PWA 6, pin 18, 17	Memory PWA 8, 9, 10, 11 and 12, pin 17 and 18	A two-phase clock to enter data into main memory.
WA0, WA1	Memory Control PWA 6, pin 23, 24	Tape H Comparator PWA 4, pin 21 (WA0) S/P Converter PWA 7, pin 24 (WA0) Memory PWAs 8, 9, 10, 11, 12, pin 24, 23 P/S Converter PWA 13, pin 17, 19	Memory line select—part of memory write address.
WCB1, WCB2, WCB3	Memory Control PWA 6, pin 38, 40 and 42	Serial-to-Parallel Converter PWA 8, pin 37, 39, 41	Data latch clock used in 8 bit/3Fsc to 24-bit/Fsc conversion.
WMA, WMB, WMC	Memory Control PWA 6, pin 22, 21 and 20	Memory PWAs 9, 10, 11, 12, pin 22	Memory board selects part of memory write address.
Wide (-)	Video Input PWA 2, pin 72	Tape VCO PWA 5, pin 71	Used to selectively steer (clear) search oscillators.
Write clock reset	Memory Control PWA 6, pin 15	Memory PWAs 8, 9, 10, 11, 12, pin 16	Terminates shift pulses to memory register.
Write pulse	Tape H Comparator PWA 4, pin 53, 54	Memory Control PWA 7, pin 53, 54 Tape VCO, PWA 6, pin 53, 54	Starts write function of memory.
Zero offset	VPR, J11-S	Sync Generator PWA 15, pin 28 Video Input PWA 2, pin 40	Tie point. VPR in E-E mode (direct transfer of signals). Shifts output vertical timing six lines.

PART I

SECTION 3

SYSTEM MAINTENANCE

3-1 GENERAL

This section introduces general maintenance practices for field testing the TBC-3. Most adjustments should be carried out with alignment procedures contained in the individual PWA sections of Part II of this manual. The arrangement of those sections presents concentrated information pertinent to each PWA as a subsystem.

This system-level introduction to testing summarizes and extends system adjustments given in the installation and operation manual to provide a framework for adjusting or troubleshooting a particular PWA. Summaries, checks, and adjustments in this manual guide the user in adapting the TBC-3 to various facility requirements or returning the unit to normal operating status in the course of repair.

3-2 PREVENTIVE/PERIODIC MAINTENANCE

Apart from keeping the unit free of dust, which contributes to heat buildup, the TBC-3 does not require preventive maintenance.

3-3 TEST EQUIPMENT REQUIREMENTS

Test equipment suggested for testing and alignment of the TBC is listed in Table 3-1. Test equipment with equivalent-or-better specifications can be substituted for equipment suggested in the table.

Table 3-1. Test Equipment and Tools

Equipment	Type/Function
Digital Voltmeter	Dc voltage accuracy ± 0.1 . Voltage range 100 mV to 20V. Hewlett Packard 3435B.
Oscilloscope	Dual-channel, 50-MHz bandwidth, 5 ns/div, 5 mV/div, A + B display mode, delayed sweep. Tektronix 465B.
Waveform monitor	Dual channel, V and H sweep modes, 1 V/4V full-scale vertical sensitivity. Tektronix 528A.

(Continued next page)

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Table 3-1. Test Equipment and Tools (Continued)

Equipment	Type/Function
Vectorscope	Composite video and vector displays, differential gain and phase measurement, external and internal phase reference. Tektronix 520A.
Signal Sources	Color bars, color black (switchable R-Y, B-Y components) variable setup level, 0-50% APL flat field, locked/unlocked subcarrier, modulated/unmodulated ramp, unmodulated staircase. Tektronix 1410 Series.
Color Video Monitor	Standard monitor for viewing stable color bars. Tektronix 650 HR.
Dropout Test Tape	Ampex VPR-2B/VPR-3, Type C, Ampex P/N 1498625.
Extender Card	Ampex P/N 1402453 (supplied with TBC-3).

3-4 SYSTEM ALIGNMENT AND TESTING

Field testing of the TBC cannot provide complete of isolation of each PWA from system interactivity that is possible in factory testing. The technician must be constantly aware of the functional relationship among PWAs when making adjustments. There is a necessary order in which certain adjustments are made. At the system level, the alignment sequence given in Table 3-2 should be observed to prevent misadjustment. The sequence is even more exacting at the PWA level of adjustment. Adjustment (or verification of circuit parameters by checking through the procedure without actually adjusting the controls) should always progress from the start of the procedure to the area of interest.

Do not consider alignment procedures in this manual routine maintenance. These procedures are rather a means of returning the TBC to normal operation following repair, or a means of adapting the TBC to other VTRs or nonstandard facility requirements. Results indicated in the procedures define normal operating parameters of the TBC. To isolate faults, make checks at points described in the various procedures and check the waveforms given for each PWA. During such checks, avoid unnecessary adjustments. Many of the controls are used merely to trim circuit tolerances during factory alignment and should be considered fixed components.

A complete alignment is not a necessary (nor recommended) practice. Only that PWA in which a malfunction has occurred would likely require adjustment. The alignment sequence of Table 3-2 is that of a complete alignment and must be used as a guide to PWA interactivity during any testing adjustments. If difficulty arises in an adjustment done outside the order given, look for a fault or misadjustment in a preceding section. The sequence given here is only general, and additional notes on interactivity are provided within the various test procedures.

Table 3-2. System Alignment Guide

PWA No.	Alignment Sequence	Alignment Procedure	Paragraph No.
System	1	Power Supply	4-5
15	2	Sync Generator	15-10
14	3	Video Output	14-8
2	4	Video Input	6-15
5	5	Tape VCO	9-10
4	6	Tape-H Comparator	8-6
6	7	Memory Control	10-14
1	8	Color Processor	5-5
3	9	A/D Converter	7-3
System	10	Unity Gain and Controls Range	3-13
15	11	Output Subcarrier and Chroma Phasing	15-23
4	12	Slow/Still Reverse Motion	8-9
5	13	Shuttle	9-13
System	14	Color Framing with VPR	3-17
7	15	Dropout Compensator	11-14
7	16	RF Detector	11-17
13	17	Velocity Compensator	13-16

3-5 MAINTENANCE ACCESS

Figure 3-1 is a maintenance access diagram which provides a step-by-step procedure for the disassembly of the TBC-3 to the major component level. Each step corresponds to the hardware or component being handled and is also the callout number on the related illustration. If complete disassembly is not required, use the steps mentioned in the table at the upper right of Figure 3-1 to gain access to a particular component.

There are slight differences in the rear support brackets between the cabinet version and the rack-mount version of the TBC-3. The console versions do not have the rear support brackets. Except for steps 5 and 6, the disassembly is the same for that shown in the maintenance access diagram, Figure 3-1.

3-6 TAPE/REFERENCE TEST LOOP

Field testing presented in this manual uses a composite video test source for reference video and simulated tape video as illustrated in Figure 3-2. The VTR interconnect must be used to maintain configuration integrity of the TBC as well as provide mode switching from the VTR. This method isolates the TBC from possible VTR video signal inaccuracy. VTR tape video output is required for some tests; the alternate setup is shown with broken lines.

Care must be taken to observe the proper use of loop-throughs, equal cable lengths, and terminations as illustrated.

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The full instrumentation shown is not always used. Use of particular instruments is called out where required in the procedure.

This test setup replicates VPR/TBC console systems with a monitor bridge, and use of that instrumentation will be apparent throughout the procedures. It must be noted, however, that the MONITOR VIDEO OUT does not have the same accuracy as VIDEO OUT 1 and 2 for critical level measurements.

3-7 WAVEFORMS AND MEASUREMENTS

Several key waveforms are provided in the reference data for each PWA. These waveforms are referenced to the simplified schematics.

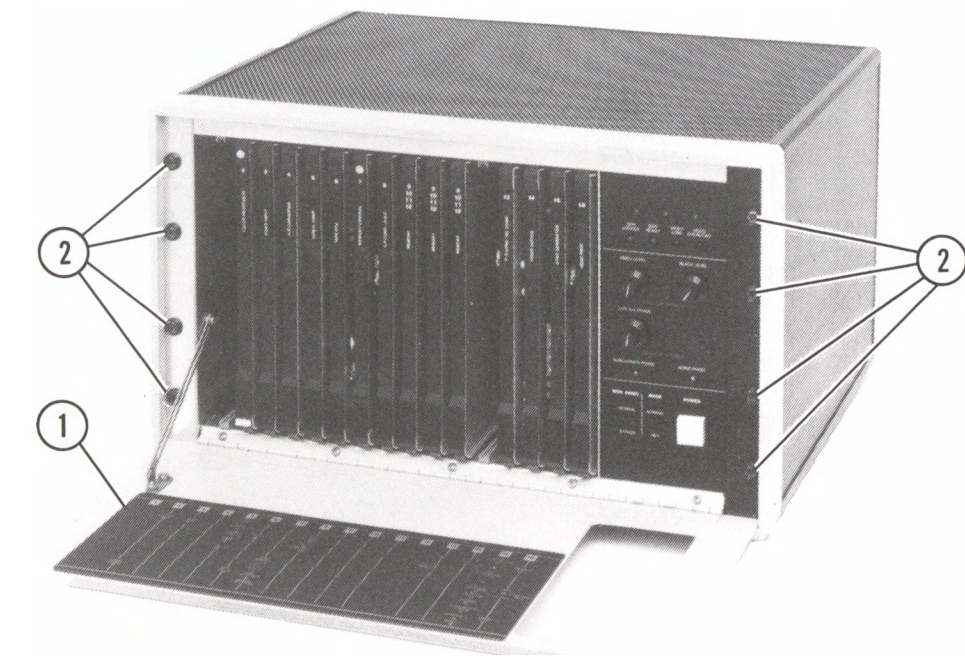
When performing adjustments given in this manual, or undertaking fault analysis with the aid of waveform photos, the following should be observed:

- All pulse width measurements are made at the 50% amplitude level.
- All rise and fall times are measured from the 10% to 90% level.
- Oscilloscope probes with 10:1 attenuation are used for all waveforms unless otherwise indicated.
- All input and output video signal measurements are taken with signals terminated by precision 75 Ω terminations.
- When taking waveforms for comparison, ensure that oscilloscope settings and triggering are as specified in the procedure or the data accompanying the waveform photo. Take special care to trigger on the odd or even field as required when using delayed sweep. The following abbreviations are used with those waveform photos which do not have vertical sensitivity and sweep time displayed on the CRT.
 - V for oscilloscope vertical sensitivity/division
 - H for horizontal time-base
 - UNCAL for an uncalibrated V or H setting
 - TRIG for oscilloscope triggering
 - .INT for internal triggering (any external trigger source is given)
 - DEL for delayed sweep

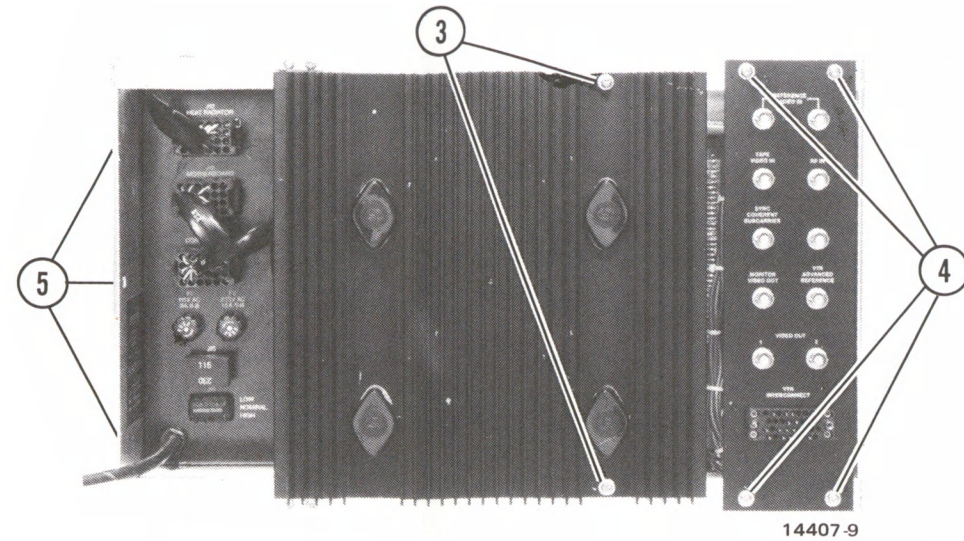
3-8 GENERAL NOTES AND PRECAUTIONS

CAUTION

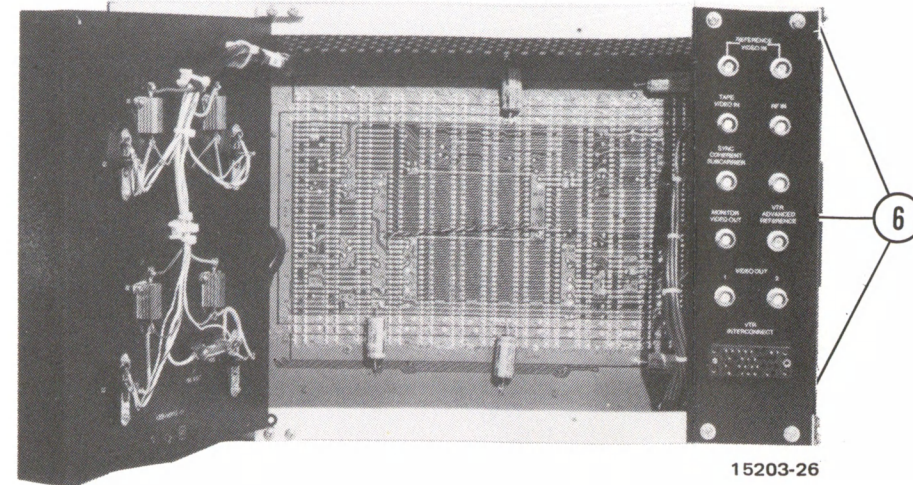
ALWAYS TURN POWER OFF WHEN REMOVING OR REINSERTING PRINTED WIRING ASSEMBLIES (PWAs). FAILURE TO DO SO MAY RESULT IN DAMAGE TO COMPONENTS ON THE PWA.



- 1 OPEN MAGNETICALLY LATCHED FRONT PANEL.
- 2 REMOVE FOUR RACK SCREWS EACH SIDE. CONSOLE VERSION ONLY: PULL CARD RACK FROM CONSOLE, PROCEED TO 7.

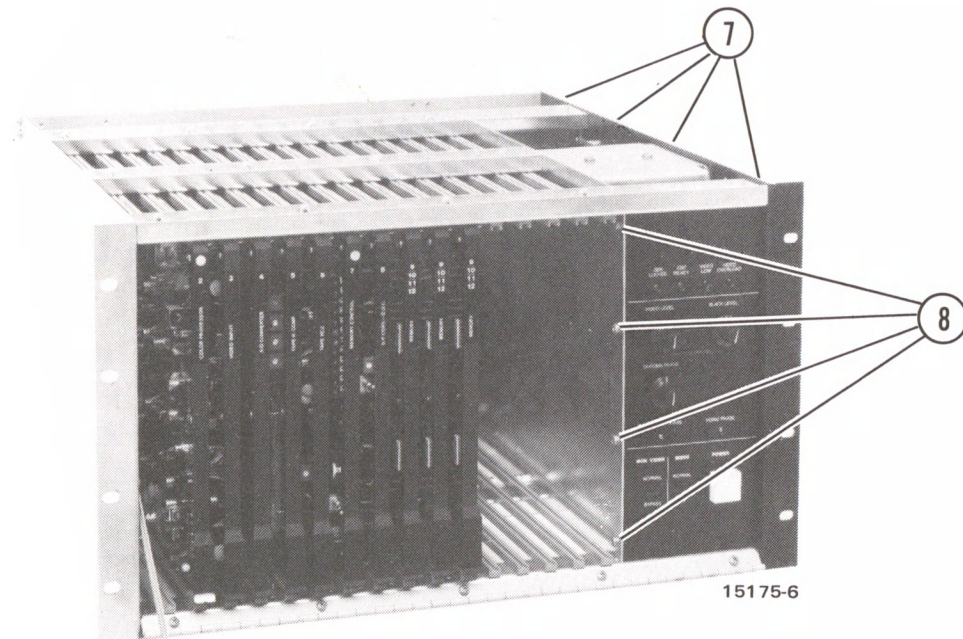


- 3 LOOSEN TWO CAPTIVE SCREWS TO OPEN HINGED HEATSINK FOR ACCESS TO MOTHERBOARD.
- 4 REMOVE FOUR SCREWS TO REMOVE CONNECTOR PANEL TO RELEASE SIDE OF CARD RACK.
- 5 REMOVE THREE SCREWS TO RELEASE LEFT SIDE OF CARD RACK.

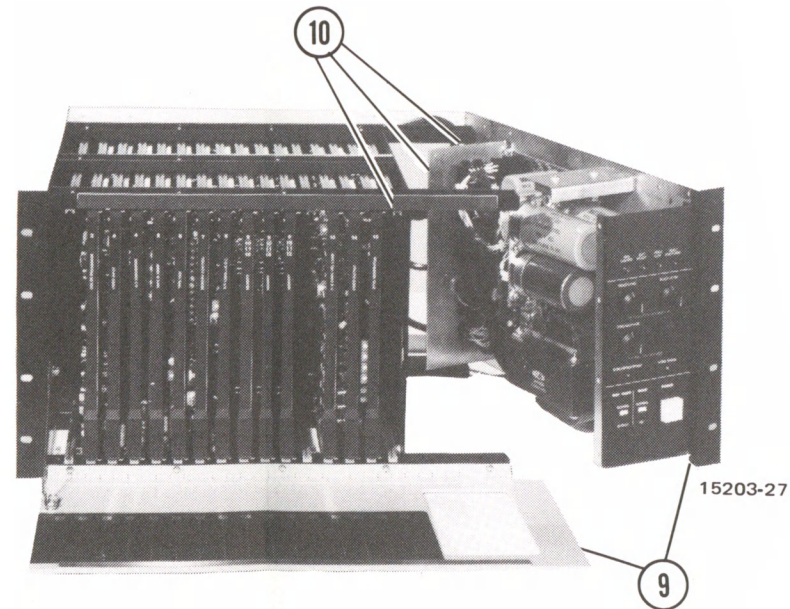


- 6 REMOVE THREE SCREWS (NOT VISIBLE) TO RELEASE RIGHT SIDE OF CARD RACK. CARD RACK MAY NOW BE PULLED FROM FRONT OF CABINET.

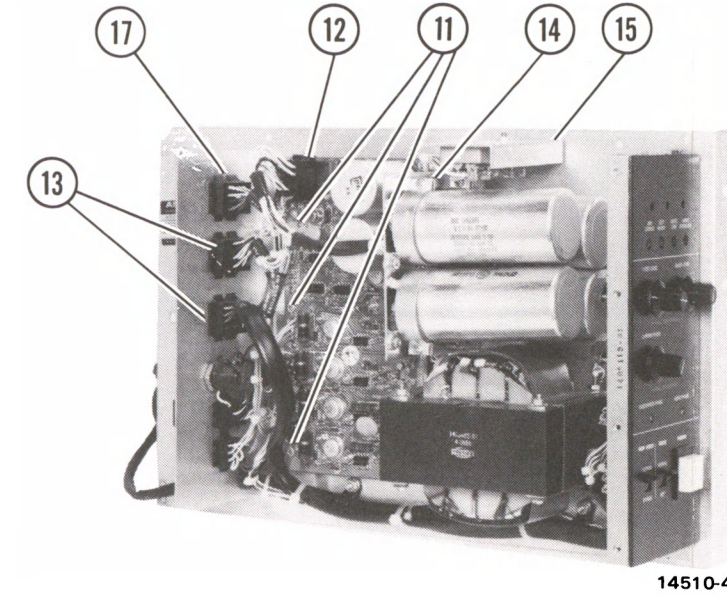
Selected Component Disassembly	
Component	Maintenance Access Disassembly Steps
Card Rack—Console and Rack Mount	1 and 2
Card Rack	1 through 6
Power Supply	1 through 10
Connector Panel	4 only
Control Panel	1 through 6 plus 16 and 17
Power Supply Transistors	3 only
Power Supply Regulator	1 through 12
Power supply Capacitors	1 through 10 plus 14
Power Supply Rectifiers	1 through 10 plus 15
+5V Supply Fuse	3 only



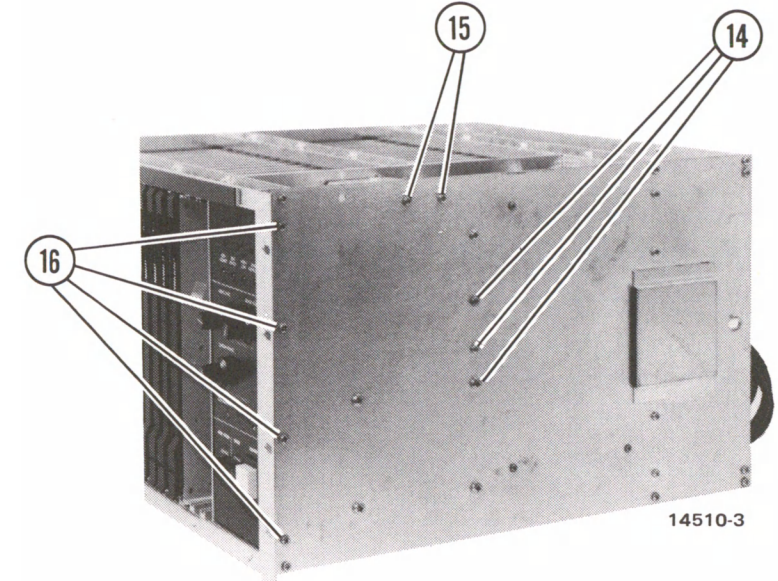
- 7 REMOVE EIGHT SCREWS, FOUR ON TOP AND FOUR BOTTOM, (NOT VISIBLE) ON RIGHT SIDE OF CARD RACK, AND
- 8 REMOVE FOUR SCREWS AT CONTROL PANEL LEFT FRONT



- 9 SEPARATE CONTROL PANEL/POWER SUPPLY SECTION FOR COMPONENT ACCESS.
- 10 DISCONNECT THREE PLUGS (J12/J13/J14—HIDDEN) TO COMPLETELY SEPARATE ASSEMBLY FROM CARD RACK.



- 11 REMOVE FOUR CORNER AND TWO SIDE SCREWS TO LIFT REGULATOR PWA.
- 12 DISCONNECT PLUG J1, AND
- 13 RELEASE J12/J13 MOUNTING LATCHES TO REMOVE REGULATOR PWA AND HARNESS.
- 14 REMOVE THREE SCREWS ON RIGHT SIDE PANEL TO FREE CAPACITOR MOUNTING BRACKET FOR ACCESS TO CAPACITORS.
- 15 REMOVE TWO SCREWS ON RIGHT SIDE PANEL TO LIFT POWER SUPPLY RECTIFIER ASSEMBLY.



- 16 REMOVE FOUR SCREWS ON RIGHT SIDE PANEL, AND
- 17 RELEASE J14 MOUNTING LATCHES TO REMOVE CONTROL PANEL AND HARNESS.

Figure 3-1.
Maintenance Access Diagram

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CAUTION

SOME ADJUSTABLE COMPONENTS HAVE BEEN SEALED WITH A LOCKING COMPOUND FOLLOWING FACTORY ADJUSTMENT. TO AVOID DAMAGE TO SUCH COMPONENTS, BREAK THE SEAL BEFORE ATTEMPTING ANY ADJUSTMENT.

- Do not allow continuous overvoltage operation when adjusting the power supply. This will shorten solid-state component life.
- Use care when handling insulated gate (MOS/CMOS) field-effect semiconductor devices in order to avoid destruction or degradation of performance as a result of static charge buildup. Persons handling such devices must be grounded using a conductive wrist strap that is connected

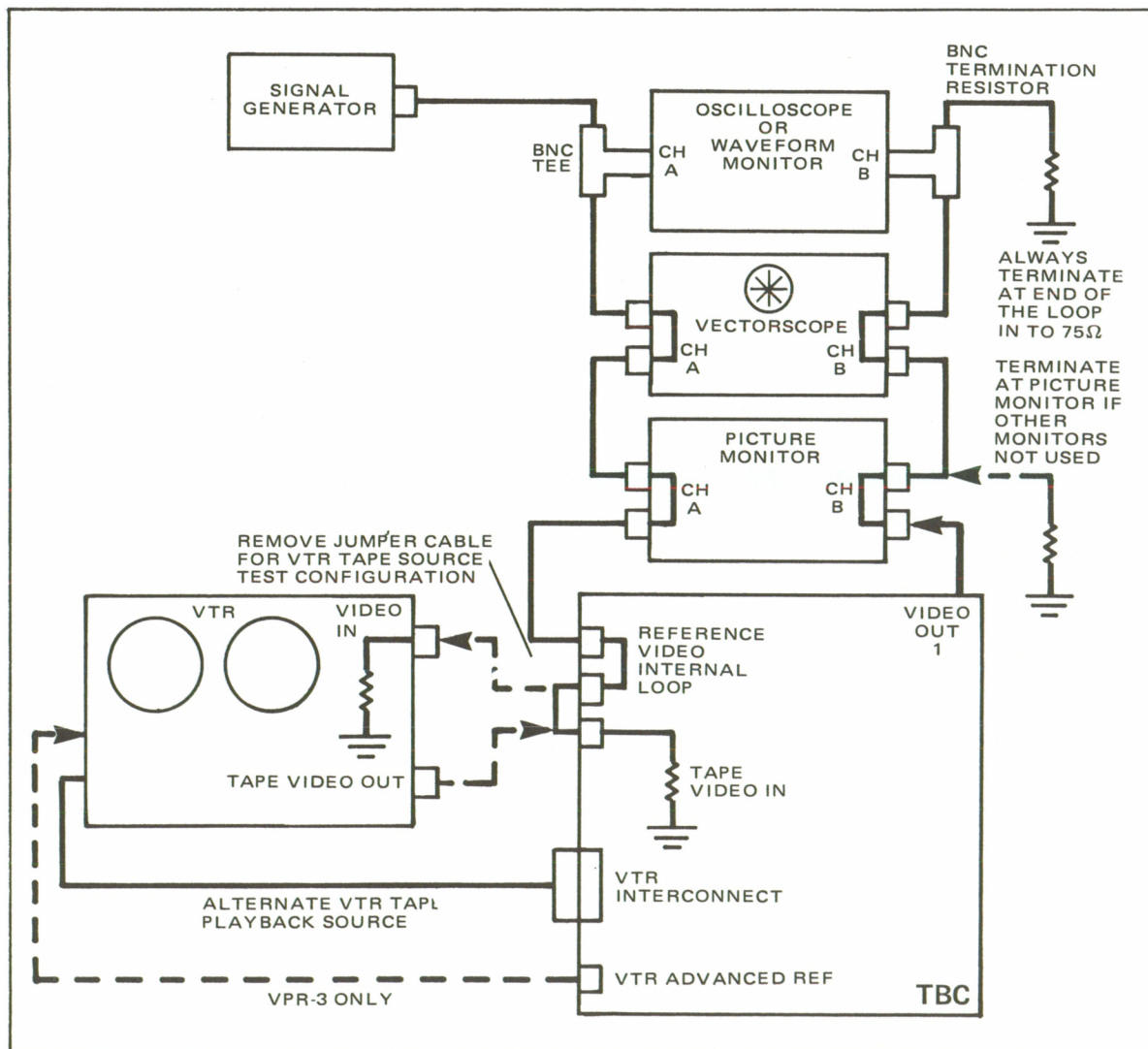


Figure 3-2. Tape and Reference Test Loop

through a 1-M Ω series resistor to ground. Use great care when the humidity is 30% or less, and make sure all leads of the device are shorted together (usually by the conductive material in which the devices are packed), until installed into the PWA.

- Adjustments and test points that are accessible at the PWA edge should be made with the PWA inserted in the card rack.
- Ensure that jumpers are returned to their original positions following tests. Refer to the complete jumper list in Section 1, Table 1-1, or the PWA jumper table in the PWA level reference data.
- Each procedure assumes that test equipment connections are removed at the completion of the procedure.
- When making adjustments or checks which do not directly involve the dropout compensator or the velocity compensator, turn them both off to reduce the variables in the checks being made.

3-9 PWA EDGE CONTROLS AND INDICATORS SUMMARY

The PWA edge controls fall into two groups:

- Those which, for reasons of stability and noise interference, must not be adjusted with the PWA on the extender.
- Those which extend the use of the TBC over a wide range of VTR, facility, and tape interchange conditions.

The summary given in Section 1, Figure 1-3, describes the appropriate condition for adjustment and references the relevant adjustment procedures.

3-10 SYSTEM LEVEL ADJUSTMENT AND OPERATION

These procedures complete the alignment of the individual PWAs at the system level and at the same time set up the TBC for normal operation in the facility. The adjustments here assume that the PWAs are aligned to the values indicated in the PWA level adjustments. If any difficulties arise with these system adjustments consult the appropriate PWA-level procedures.

Note

All procedures pertain to the 12- and 16-line versions of the TBC-3 except where noted in the text.

3-11 System Reference Phasing Routine

The factory setting for reference sync/burst calibration control R223 on Sync Generator PWA 15 lights calibration indicator DS1 on PWA 15 edge for RS170A standard reference. If DS1 is not on for a known RS170A reference input, the technique given in steps 1 through 4 recalibrates DS1 while illustrating aspects of color framing with which the user should be familiar. If the facility reference is RS170A and DS1 is on, go to the system-phasing routine, step 5. An alternate R223 calibration procedure in the Sync Generator PWA 15 adjustment section is part of

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the PWA-level adjustment and furnishes a guide to adjusting sync/burst phasing to a non-RS170A facility reference where color-framed editing is not a requirement.

Setup:

- Sync Generator PWA 15 Jumper J6 to A-B position (RS 170 A standard)
- Normal VPR/TBC interconnection
- 75% color bar, inputs to VPR and TBC reference with Standard RS170A burst/sync phase
- Scope (observe 75 Ω termination requirements):
 - CH1: Reference video
 - CH2: TBC Video Out 1
 - Trigger: VPR-2B PWA 14 TP7, 15-Hz frame pulse
VPR-20 Video PWA—TP28, field I pulse
VPR-3 Color Framer P 1A 5 pin 87, field I identification
 - Vectorscope: Parallel connections with oscilloscope channels 1 and 2.
Trigger channel 1 external subcarrier phase.

The procedure for reference sync/burst phase calibration (R223) is as follows:

- STEP 1** With the setup above, play back an RS170A-recorded tape and display four vertical intervals as shown in WF1, Figure 3-3. Note that control panel EDIT READY indicator should be on for the RS170A-recorded tape.
- STEP 2** The object is to identify line 10 of field III. Using the scope-delayed sweep, display a single vertical interval as shown in WF2. Note that the 1/2-line relationship between the last post-equalizing pulse and the first horizontal line with burst indicates line 10 of field I or III. To further identify field III, examine the sync/burst interval to find the same phase of burst between the reference and TBC output.
- STEP 3** Expand delayed sweep again to display single sync/burst interval shown in WF3. Examine first cycle of burst. If bursts are of opposite phase, sync generator is producing line 10 field I when the reference is line 10 field III. Field III is identified here with reference also to the RS170A data sheet where first cycle of burst on field III, line 10 is negative-going and is furthermore at a nominal 5.3 μ s from H sync leading edge.
- STEP 4** Turn R223 so TBC output and reference burst phase are the same phase as shown in WF3 and DS1 is on. Center control within range of DS1 illumination. Note that there are two positions of R223 which will turn DS1 on, but only one which turns DS1 on and produces correct burst phase.

Horizontal phase adjustment: Control panel HORIZ PHASE moves the leading edge of the sync/burst interval in steps of one subcarrier cycle while control panel

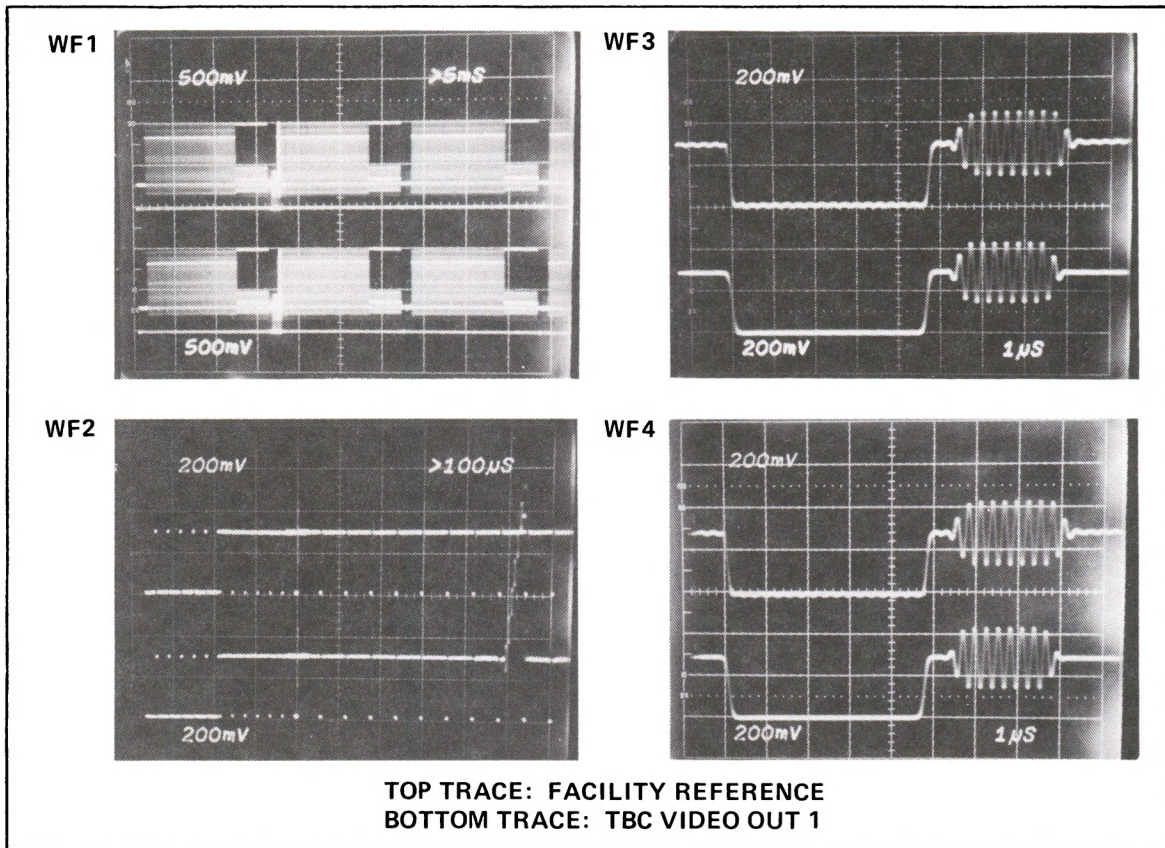


Figure 3-3. System Phasing Waveforms

SUBCARRIER PHASE is a fine adjustment of burst phase within that subcarrier cycle (279 ns). Adjust **HORIZ PHASE** to line up leading edges within a subcarrier cycle.

Subcarrier phase adjustment: Using oscilloscope display for coarse phasing and the vectorscope for fine phasing, adjust control panel **SUBCARRIER PHASE** for the same burst phase. Since reference and TBC outputs are now both RS170A, the remaining H sync phase error will be removed.

Chroma phase adjustment: Using vectorscope, superimpose reference and output chroma vectors, using either variable **CHROMA PHASE** control or unity **CHROMA PHASE** trim (control panel--top center) as required.

This sync/burst calibration with R223 returns the TBC to standard RS170A setting and ensures consistent color frame. If control panel controls are not appropriately centered for the operation, or more subcarrier or chroma phase range is needed, use the procedures given in the Sync Generator PWA 15 section to return the system to the standard factory settings. That procedure may also be used to align the TBC to a non-RS170A reference so that any reference sync/burst can be matched by using R208 (subcarrier phase) and R146 (chroma phase) as described in Figure 1-3.

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3-12 Non-RS170A H-Sync Phasing

Output sync/burst control R240 is used to phase the output H-sync pulse to any non-RS170A equipment without affecting subcarrier phase. Reference sync/burst (R223) remains calibrated to RS170A standard reference of the facility. Color frame is maintained for RS170A standard tapes but inserted H-sync from the sync generator is displayed.

- STEP 1 Move Sync Generator PWA 15 jumper J6 to the B-C (non-standard) position and center control R240, output sync/burst.
- STEP 2 Using a delayed sweep oscilloscope and vectorscope as described in paragraph 3-11, RS170A system phasing routine, compare reference and TBC outputs.
- STEP 3 Adjust control panel HORIZ PHASE for coincidence of the sync leading edge within a subcarrier cycle.
- STEP 4 Adjust control panel SUBCARRIER PHASE to superimpose burst vectors of reference and TBC output.
- STEP 5 Sync leading edge will shift as SUBCARRIER PHASE is adjusted. Adjust R240 to realign sync leading edges.

3-13 Unity Gain and Adjustable Controls Range

This procedure is the final TBC unity gain input/output adjustment. It ensures that with a standard VTR tape input and accurate system reference phasing, the TBC will be virtually "transparent". Adjustment of the front panel unity trim controls for video and black levels and chroma phase can be a one-time setup adjustment for normal TBC use in the facility. These trim controls parallel the adjustable control function and are set for the output level/phase to be the same as that of standard input. When the VTR is operating normally under standard conditions, is properly color framed, and tapes are recorded with standard sync/burst phase, the TBC does not require adjustment. The following procedure uses the tape reference test loop of Figure 3-1 to illustrate unity settings in a maintenance context. The routine with a normal VTR configuration would be similar.

Setup procedure:

Note

Make certain that all inputs used during this procedure are standard 1.0-Vp-p levels. When comparing video input signals use cables of equal length and use 1/4% tolerance 75 Ω termination resistors into a properly calibrated oscilloscope.

- STEP 1 Use tape/reference test loop with a 100% color bar signal at 0% setup level and a 100% white calibration pulse.
- STEP 2 Connect waveform monitor and vectorscope.

- STEP 3** Verify normal system reference phasing (paragraph 3-11).
- STEP 4** Place the following controls to center (detent) unity position: VIDEO LEVEL, BLACK LEVEL, and CHROMA PHASE.
- STEP 5** Switch TBC-3 MODE to NORMAL.
- Verify indicator conditions for normal operation. All green indicators on:
- a. GEN LOCK, EDIT READY (control panel)
 - b. REF SYNC/BURST (Sync Generator PWA 15)
 - c. Memory centering indicators (Memory Control PWA 6)
 - (1) 12-line system (EE mode); Top green LED—blinking, bottom green LED—steady
 - (2) 16-line system (EE mode); Second red LED up from top green LED—steady, bottom green LED—blinking

Note

In play mode, bottom green LED is on steady (12- and 16-line systems). If upper green LED comes on, this indicates field sequence has been altered.

Red indicators off:

- a. Shuttle indicator (Tape VCO PWA 5) memory overload (Memory Control PWA 6). An occasional lighting sequence here indicates a step function error correction or memory recentering due to accumulated error.
- b. VIDEO LOW/VIDEO OVERLOAD (control panel). There may be an occasional flash in shuttle due to unclamped video.

Video level procedure: The output level sets the gain of the final amplifier stage on Video Output PWA 14. Front panel VIDEO LOW/VIDEO OVERLOAD indications are a function of video input level to Video Input PWA 2. If a nonstandard tape is being played and either level indicator comes on, the video level control R13 (PWA 2) can be used to effectively extend the range of the control panel VIDEO LEVEL. However, since R13 is the calibration control for the low/overload indicators, the PWA 2 adjustment section should be consulted for recalibration.

- STEP 1** Adjust unity video level trim control (front panel top left) so that peak white calibration pulse of the color bar is at 100% (100-IRE units) on waveform monitor (or a difference of less than 10 mV between input and output).
- STEP 2** Adjust front panel VIDEO LEVEL control fully counterclockwise. Level should be reduced to 70 (± 10) IRE units.
- STEP 3** Adjust control fully clockwise and verify a 120 (± 10) IRE unit level.

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Sync level procedure: Adjust sync and burst at Video Output PWA 14 if required (paragraph 14-10).

STEP 1 H-sync—286 mV (40 IRE)

STEP 2 Burst—286 mV (40 IRE) and symmetrical with the blanking level.

Black level adjustment: Black level control sets up an arbitrary interval reference at the sync tip level on the A/D video on the Video Input PWA 2. This sets the range of the video to be quantized.

STEP 1 Adjust unity black level trim control for same level between input and output.

STEP 2 With power off remove Video Output PWA 14 and remove jumper J4 (removes black clip). Reinstall PWA 14 into cage.

STEP 3 Observe black reference on output color bar signal. The variable BLACK LEVEL range should be 30 (± 10) IRE units.

STEP 4 With power off reinstall jumper J4 to position A-B.

Chroma phase adjustment: Unity CHROMA PHASE trim (control panel top-center) is set during the system reference phasing routine (paragraph 3-11). Range and centering adjustments are found in paragraph 15-22 (Sync Generator PWA 15).

3-14 Tape-H/Sync to Video Timing

These adjustments complete alignment of the write timing circuits of the Tape-H Comparator, Tape VCO, and Memory Control PWAs. Timing is set at the factory for standard RS170A burst/sync phase and will not require adjustment unless a nonstandard burst/sync phase is used or adjustments have been made to the write timing at the PWA level.

STEP 1 Use tape/reference test loop setup (paragraph 3-5) with a 75% split field color bar signal at standard level and sync/burst phase (or the nonstandard facility reference) connected to TAPE VIDEO IN on connector panel.

STEP 2 Switch TBC MODE to NORMAL.

STEP 3 With power off extend Tape VCO PWA.

STEP 4 Switch power on and verify that front panel EDIT READY and Sync Generator PWA 15 REF SYNC/BURST calibration indicators are on. Refer to Tape H Comparator PWA 4 and Sync Generator PWA 15 alignment procedures if indicators are not on.

STEP 5 Connect oscilloscope to VIDEO OUT 1 and using delayed sweep, line up leading edge of white bar on center graticule. Use sufficient sensitivity

to see any horizontal shift within a subcarrier cycle. This will be the reference point for the next steps.

- STEP 6** Remove burst signal from video input signal source.
- STEP 7** Adjust Tape VCO PWA 5 R53 (H-sync phasing) to reposition white bar edge on center graticule.
- STEP 8** Alternately switch burst on and off while adjusting R53 for minimum horizontal shift.
- STEP 9** Switch TBC between NORMAL and BYPASS. Note any shift in picture position.
- STEP 10** If there is a shift in picture position, turn thumbwheel horizontal phasing switch S2 on Memory Control PWA 6 to a position which minimizes horizontal shift. Each position of switch moves the picture an increment of one subcarrier cycle with respect to sync generator horizontal sync.

Note

As S2 is set to its extremes, a vertical line will appear at edge of screen. This is an indication that invalid data is being read out of memory, i.e., the valid data for each line of video is read out early or late as memory locations without video data are being accessed.

- STEP 11** Switch TBC power on and off several times and verify that picture position remains the same.

3-15 VPR Slow-Motion Operation

The VPR may be sequentially switched between normal and all slow/still/reverse speeds without picture breakup or loss of color frame. EDIT READY indicator should remain on throughout these modes. If EDIT READY is on and properly calibrated for normal playback, but goes out in slow motion, a readjustment of SLO-MO burst/sync phase control R170 on Tape H Comparator PWA 4 (front edge) may be in order. See paragraph 8-9 in Tape H Comparator PWA 4 adjustment section.

3-16 Shuttle Mode with the VPR

The normal picture during shuttle is monochrome with black streaks. The SHUTTLE VCO indicator (PWA 5) will be on. The memory line indicators on PWA 6 will sequence randomly, and the occasional flash of the VIDEO LOW/VIDEO OVERLOAD indicators on the control panel (due to unclamped video) is normal.

3-17 Color Framing with the VPR

This color framing test demonstrates adjustments which affect input/output phasing and coordination with the VPR controls. This in turn verifies the transparency of the TBC in terms of unity gain, system phasing, and memory write/read timing necessary for matched cut editing.

TBC-3

This test uses the normal VPR/TBC console monitor system or the VTR tape source test configuration illustrated with the tape/reference test loop described in paragraph 3-5. Complete setup as follows:

- STEP 1 Loop signal generator composite video output through picture monitor channel A input, then TBC REFERENCE VIDEO IN loop-through to the VPR VIDEO INPUT.
- STEP 2 Connect VPR output to TBC TAPE VIDEO IN.
- STEP 3 Connect TBC VIDEO OUT 1 to picture monitor channel B input (terminate).
- STEP 4 On monitor set picture SCAN switch monitor to PULSE CROSS.
- STEP 5 On monitor set INPUT MODE switch to A-B.
- STEP 6 Make sure that reference composite video conforms to RS170A standard (or the facility standard) for level and sync/burst phase. Use a split field 75% color bar signal.
- STEP 7 Prepare for playback a known good recording of split field 75% color bars.

Set up TBC as follows:

- STEP 1 Set MODE to NORMAL
- STEP 2 Set MON VIDEO to NORMAL.
- STEP 3 Set VERT CTRG/MEMORY CTRG (Memory Control PWA 6 edge) to VERT/CTRГ.
- STEP 4 Use center unity positions for VIDEO LEVEL, BLACK LEVEL, AND CHROMA PHASE (this assumes that unity settings conform to RS170A standard video).

Prepare VPR as follows:

- STEP 1 On the VPR turn color frame on and set color frame phase to normal. (Refer to appropriate operators manual as required).
- STEP 2 Switch sync head ON (if present on VPR).
- STEP 3 Play back RS170A recording at normal speed and note that after a few seconds the VPR SERVO light will go out indicating VPR has color framed.

Verify transparency of TBC-3 concerning sync-to-video timing relationship as follows:

Note

Vertical and horizontal sync of the input and output signals must be coherent, and sync-to-video timing of input and output signals must be coherent.

- STEP 1** Verify that the following indicators are illuminated:
- a. Upper green LED on Memory Control PWA 6.
 - b. Reference sync burst indicator DS1 (and color lock indicator DS2, 16-line system only) on Sync Generator PWA 15.
 - c. EDIT READY indicator on control panel.
 - d. GEN LOCKED indicator on control panel.
- STEP 2** Verify that display on picture monitor is completely cancelled (gray screen) and that there are no bright horizontal or vertical lines on I and Q signals.
- STEP 3** If cancellation is not complete go to next step. If cancellation is complete, move to step 7.
- STEP 4** Adjust SUBCARRIER PHASE CONTROL on TBC-3 panel for complete color cancellation.
- STEP 5** On Memory Control PWA 6, adjust thumbwheel horizontal phasing switch S2 for no bright vertical lines on I and Q edges.

Note

If step 5 cannot be accomplished, perform step 6.

- STEP 6**
- a. VPR-2B: On Color Framer PWA 13, switch SELECT P/B phase switch to the opposite position and repeat step 5.
 - b. VPR-80: Press CLR FMR INVERT switch and repeat step 5.
 - c. VPR-3: Set VPR-3 color framer to opposite phase and repeat step 5.
- STEP 7** Stop and start tape. The VPR should color frame (SERVO on), EDIT READY should come on, and the screen should cancel to gray. If I and Q sections do not cancel and EDIT READY does not come on, select the other position for color frame phase. Switch VPR from NORMAL play to SLOW and back to NORMAL to force VPR to recolor-frame. EDIT READY should now be on and cancellation should be complete.
- STEP 8** If necessary, readjust Memory Control PWA 6 horizontal position switch to cancel any bright vertical lines on I and Q section edges.
- STEP 9** Switch VPR from NORMAL to SLOW MOTION.

TBC 3

- STEP 10** Verify that EDIT READY stays on. If it does not, adjust R170 (SLO-MOΦ, Tape H Comparator PWA 4) for EDIT READY to be on for slow, still, and reverse motion. If R170 is adjusted, recolor-frame the VPR by switching between NORMAL and SLOW motion.
- STEP 11** Observe picture cancellation and note that on I and Q sections a white line switches back and forth between the top and bottom of the I and Q sections. This is the normal effect of the ambiguous burst/sync phase of the repeated frame in the slow/still motion modes of the VPR.

3-18 Heterodyne Operation

Heterodyne and nonservoed capstan VTR operations require specific jumper configurations to meet particular VTR requirements as well as a possible adjustment of advanced vertical reference, vertical blanking, and the chroma and luminance levels. This procedure reviews operation with the heterodyne and nonservoed capstan VTRs. For reference, the configuration variations for the several possible VTRs are presented with a setup and summary procedure, only part of which will be applicable to a particular VTR.

Setup:

1. Jumper options:

- PWA 15 J1** A-B 12-line systems: Fixed 5.5—6.5-line advance to compensate for one-half the TBC memory delay of the video.
- A-B 16-line systems: Adjustable line advance. Connect scope and adjust R262 (line advance) on PWA 15 as follows:
- a. Connect channel 1 scope probe to pin 15 (REF VIDEO).
- b. Connect channel 2 scope probe to pin 37 (advanced reference).
- c. Adjust R262 so signal at pin 37 is 10 lines in advance of the signal at pin 15.
- B-C Dynamic advance adjusted by R67—advance reference vertical delay (see below).
- PWA 15 J2** Advanced reference signal output options (measured at rear panel VTR ADVANCED REFERENCE connector J8, terminated).
- B-D Vertical Sync: $-4V \pm 0.4V$
- B-A Composite Sync: $-4V \pm 0.4V$
- B-E Composite Sync/Burst: sync level $0.33 V_{p-p} \pm 0.03 V_{p-p}$,
burst level $0.4 V_{p-p} \pm 0.04 V_{p-p}$
- B-C Composite Sync: $0.33V \pm 0.03V$ (with VTR switched to INTERNAL SUBCARRIER)
- PWA 5 J6** A-B Sets up internal TBC sync delay processing to accommodate single-wire heterodyne.

B-C Enables tape Fsc processing for two-wire heterodyne subcarrier input. Prevents video signal being routed through Color Processor PWA 1. Stabilization of sync-to-burst relationship is accomplished in remodulation circuits of the VTR in a two-wire operation.

PWA 7 J2 A-B Allows onboard dropout detector to be used in heterodyne.

2. Switches:

- a. TBC MODE switch TO HET.
- b. Memory Control PWA 6 edge: Set VERT CTRG/MEMORY CTRG switch to MEMORY/CTRG.
- c. On two-wire heterodyne VTR, switch subcarrier to external.

With a normal TBC/VTR hookup play a standard 75% color bar recording and make any necessary adjustments as follows:

STEP 1 Advanced reference:

- a. With power off extend Sync Generator PWA 15.
- b. Connect oscilloscope as follows:
CH1—Video Input PWA 2 TP1 (tape video in—TP1 is at PWA edge just above video level control).
CH2—Sync Generator PWA 15 pin 15 (reference video). Trigger on PWA 15 pin 82 (tape vertical—use delayed sweep).
- c. Observe tape and reference vertical intervals and adjust R67 (advance reference vertical delay) so that tape vertical sync leads reference by 5.5 lines.
- d. With power off return Sync Generator PWA 15 to the cage.

STEP 2 Chroma and luminance levels:

No adjustment should be required for a standard level tape. If adjustment is necessary, follow procedure outlined in Color Processor PWA 1 adjustments, paragraph 5-7, using a normal tape input. Note that levels should be reset for VPR slow-motion operation.

STEP 3 Vertical delay:

Some VTRs may require readjustment of the vertical delay circuit on the Tape VCO PWA 5 to eliminate head switching transients in vertical interval. Consult paragraph 9-12 in the tape VCO adjustment section.

STEP 4 Dropout compensator rf detector:

Consult the adjustment procedure in the S/P Converter PWA 7 maintenance section to adjust the dropout level with or without a dropout test tape.

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3-19 VPR-20 Operation

The Type C format VPR-20 operation uses the same tape VCO jumper configurations as the VPR-2B with sync head, but unlike the VPR-2B, an advanced reference must be used because the VPR-20 does not have internal circuitry to compensate for the TBC memory delay (one-half the 12-line (16-line) memory).

Setup:

1. Jumper positions:

- | | | | |
|--------|-----|-----|---|
| PWA 5 | J6 | A-B | Sets up normal internal TBC sync delay. |
| | J9 | A-B | For sync head video processing. |
| | J12 | A-B | For back porch format dropout operation. |
| | J1 | A-B | For internal control of the VCO search oscillators. |
| PWA 7 | J2 | A-C | Enables rf dropout detector circuit. |
| PWA 15 | J1 | A-B | Fixed, 5.5-line (10-line) advance to compensate for one-half the TBC memory delay of the video. |
| | J2 | B-E | Selects composite sync with burst advanced reference signal out for VPR-20 servo. |

2. Switch: Memory Control PWA 6 edge: Set VERT CTRG/MEMORY/CTRG switch to MEMORY/CTRG.

There are no adjustments to be made separately for VPR-20 operation that are not common to the basic TBC adjustments given in this manual for normal VPR-2B operation except for the VPR-20 interface kit mentioned above.

The VPR-20 playback gives the same control panel and PWA Edge Control indications outlined in paragraph 3-13.

3-20 FAULT ISOLATION

The first step in fault isolation is to reduce variables by setting up the tape/reference test loop and turning off the dropout and velocity compensators. Then, making certain the input tape and reference video are standard, begin checking for normal conditions following the pattern of system alignment order (paragraph 3-4).

3-21 Reference Data

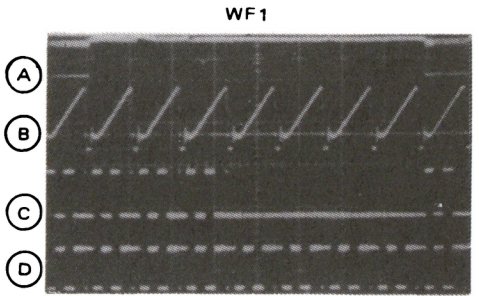
In order to simplify testing, theory and maintenance information for each PWA is presented in a separate section of this manual. Reference data sheets at the end of each section support both the descriptive and maintenance information. These data sheets contain key waveforms as well as summaries of test points, controls, and jumpers. Simplified schematics give one-shot times, counter preloads, and interconnect data. See Section 4 of Part II to become familiar with the arrangement and use of the reference data.

3-22 Digital Path Faults

Interestingly, digital path faults are easier to recognize than some of the analog and timing subtleties of the TBC. The test ramp bit finder diagram, Figure 3-4, reveals some typical faults. The diagram is entirely self-explanatory and assumes that the dropout compensator is switched off. Sample comparison waveforms of specific missing bits and the accompanying notes provide a method of identifying faulty devices at various points in the digital path. The test ramp is generated on Video Input PWA 2 (Assembly No. 1463650) when jumper J5 is placed in the B-C position.

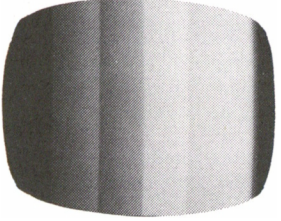
SETUP CONDITIONS

- COLOR BARS TO TAPE VIDEO IN AND REFERENCE VIDEO IN
- JUMPER J5 (PWA 2) TO B-C (TEST RAMP)
- SWITCH PWA 7, S1 TO DROPOUT COMP (DOC) OFF
- SWITCH PWA 13-S1 TO VEL COMP OFF
- OSCILLOSCOPE CH A TO PWA 8, U14-4
- OSCILLOSCOPE CH B TO VIDEO OUT 1
- TRIGGER OSCILLOSCOPE ON Wφ1: PWA 6, PIN 18
- SETUP SHOWS EIGHT LINES AS IN WAVEFORM 1. CHANNEL C AND D SHOW THE MEMORY LINE AND BIT OF INTEREST.



- (A) PWA 8, U14-4 (R1φ1 READ CLOCK). LINE 1 REFERENCE
- (B) VIDEO OUT 1 SHOWING EIGHT LINES
- (C) PWA 8, U15-8 BIT 10 (BIT 2 OF 10.7 MHz BYTE 2 SHOWING MEMORY OUTPUT OF BIT 10 FOR LINES 1 THROUGH 4. NOTE THAT THERE IS NO OUTPUT FROM U15-8 DURING LINES 5-8
- (D) PWA 8, PIN 42, BIT 10 SHOWN FOR LINES 1-8 ON THE COMMON MEMORY BUS

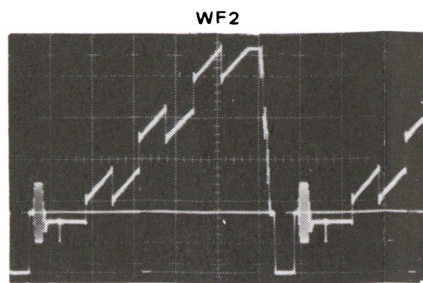
DIGITAL PATH FAULT SYMPTOM



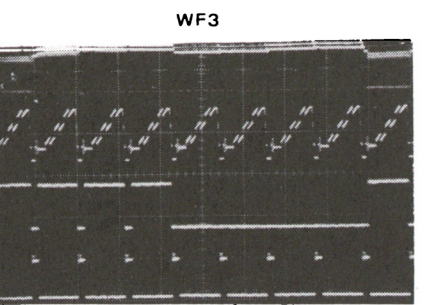
TWO OR MORE VERTICAL BARS IN THE MONITOR VIDEO INDICATE A FAULT IN THE DIGITAL PATH

THE DISPLAY SHOWN IS THE RESULT OF GROUNDING PWA 8 PIN 79 (BIT 3 OF THE 24 BIT BYTE, A 3.58 MHz RATE FAULT)

10.7-MHz RATE FAULT



A FAULT IN ONE OF THE 10.7-MHz RATE 8 BITS (A/D AND THE DATA SECTION OF THE S/P AND P/S CONVERTERS) APPEARS AS STEPS IN THE VIDEO OUTPUT (WF2 ABOVE). THE RESULT OF GROUNDING PWA 7, PIN 42, AT INPUT TO S/P CONVERTER.



- (A) PWA 8, U14-4
- (B) VIDEO OUT 1
- (C) PWA 8, U15 2/BIT 3
- (D) PWA 8, PIN 35

WITH BIT 3 LOW AT THE S/P CONV, INPUT, PIN 42. NOTE IN WF3 THAT THE STEPS APPEAR IN ALL EIGHT LINES (TRACE B). TRACE (D) IN WF3 SHOWS THE LOW OUTPUT FOR BIT 3 (OF THE SERIAL 8 BIT BYTE). PINS 43 AND 51 (BIT 3 OF THE SECOND AND THIRD SERIAL 8 BITS) ARE SIMILARLY LOW

A MISSING 1 OF 8 BIT IS EASILY IDENTIFIED BY MISSING BITS AT THE 3 CORRESPONDING BIT LOCATIONS EVERYWHERE IN THE 3.58 MHz RATE PARALLEL 24 BIT PATH.

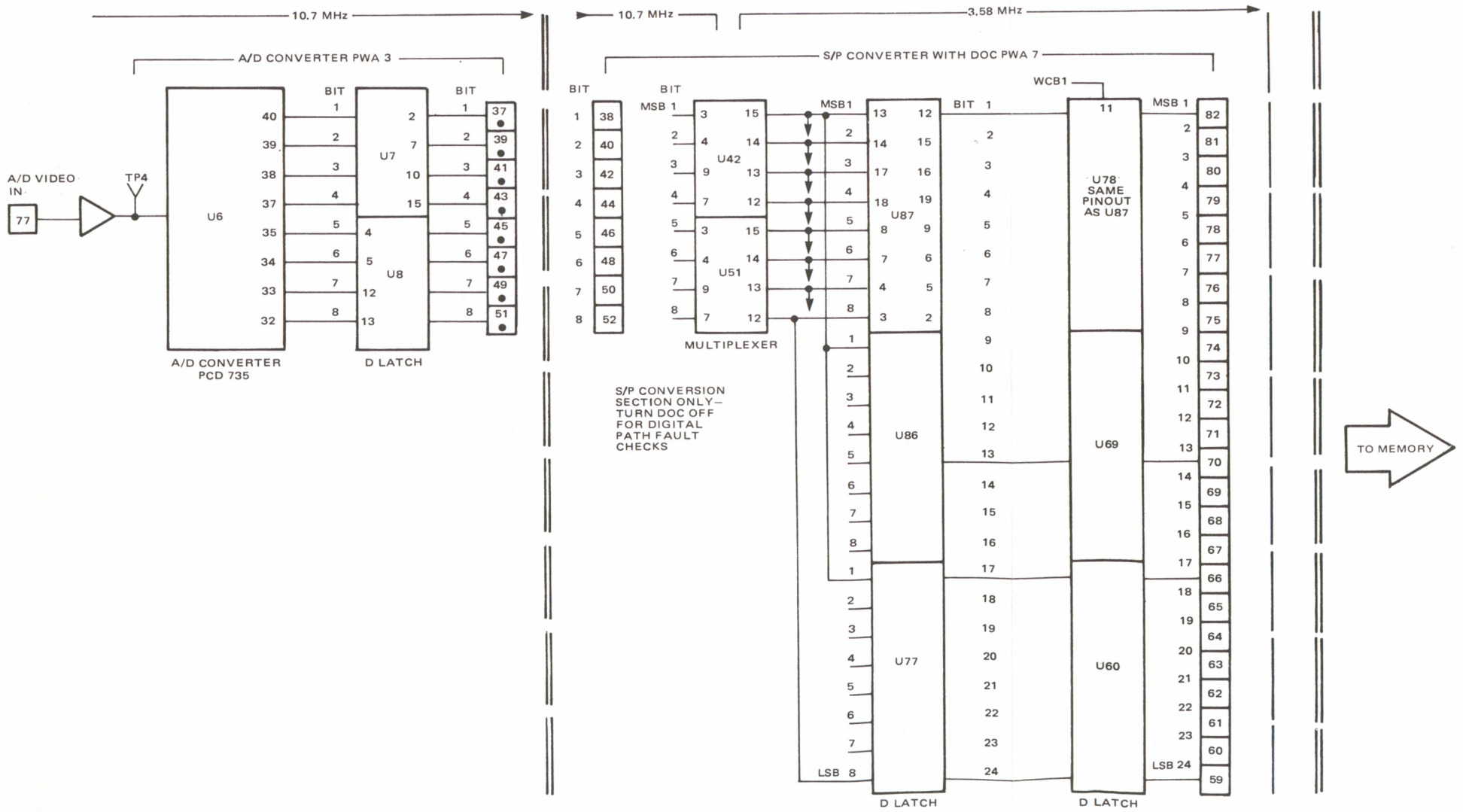
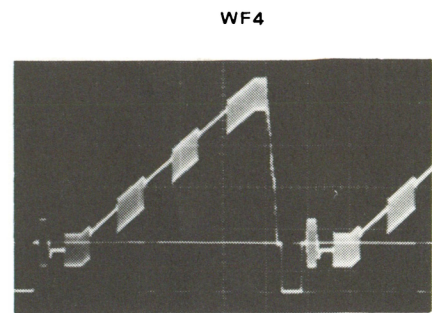
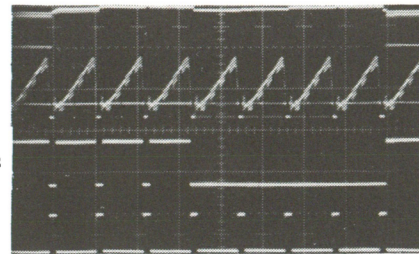


Figure 3-4.
Digital Path Interconnection and Test
Ramp Bit Finder (Sheet 1 of 2)

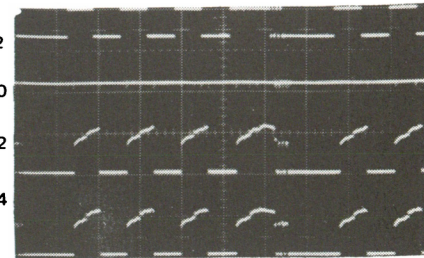


A FAULT IN ONE OF THE 3.58 MHz RATE 24 BITS (MEMORY AND THE PARALLEL SECTION OF THE S/P AND P/S CONVERTERS APPEARS AS BURST RATE NOISE ON THE RAMP AT THE VIDEO OUTPUT SHOWN IN WF4 ABOVE. THE RESULT OF GROUNDING PWA 7, 80 (BIT 3 OF 24).

- WF5
- (A) PWA 8, U14-4
 - (B) VIDEO OUT 1
 - (C) U15-2 BIT 1 PWA 8
 - (D) PWA 8, PIN 35



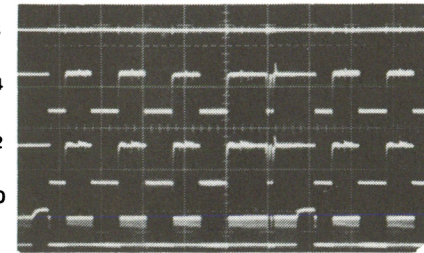
- WF6
- (A) PWA 7, PIN 42
 - (B) PWA 7, PIN 80
 - (C) PWA 7, PIN 72
 - (D) PWA 7, PIN 64



THE BURST RATE NOISE IS SEEN ON ALL EIGHT LINES AT TRACE (B) OF WF5. THE MISSING BIT 3 IS SHOWN IN TRACE (D) IN WF5, MEMORY OUTPUT, AND IN TRACE (B) IN WF6 (NOTE ALSO THAT TRACE (A) IN WF6 IS THE 10.7-MHz RATE BIT 3 INPUT TO THE S/P CONVERTER, AND TRACES (B), (C), AND (D) ARE THE PARALLEL OUTPUTS FOR BIT 3—BITS 3, 11, AND 19). BIT 3 IS ALSO LOW AT THE A13 INPUT IN TRACE (A) OF WF7, WHILE BIT 11, TRACE (B), AND BIT 19, TRACE (C) ARE NORMAL. COMPARE THE ABNORMAL TRACE (D) WITH WF8.

WF8 AT RIGHT SHOWS TYPICAL CONDITIONS FOR A BAD MEMORY IC. NOTE THAT ONLY LINE 5 HAS THE BURST NOISE IN THE RAMP. LINE 5 IS ON MEMORY PWA 9, LINE 1. IN THIS CASE, U23-10 FAILED.

- WF7
- (A) PWA 13, PIN 36
 - (B) PWA 13, PIN 44
 - (C) PWA 13, PIN 52
 - (D) PWA 13, PIN 20



- WF8
- (A) PWA 8, U14-4
 - (B) VIDEO OUT 1
 - (C) PWA 9, U15-2
 - (D) PWA 9, PIN 35

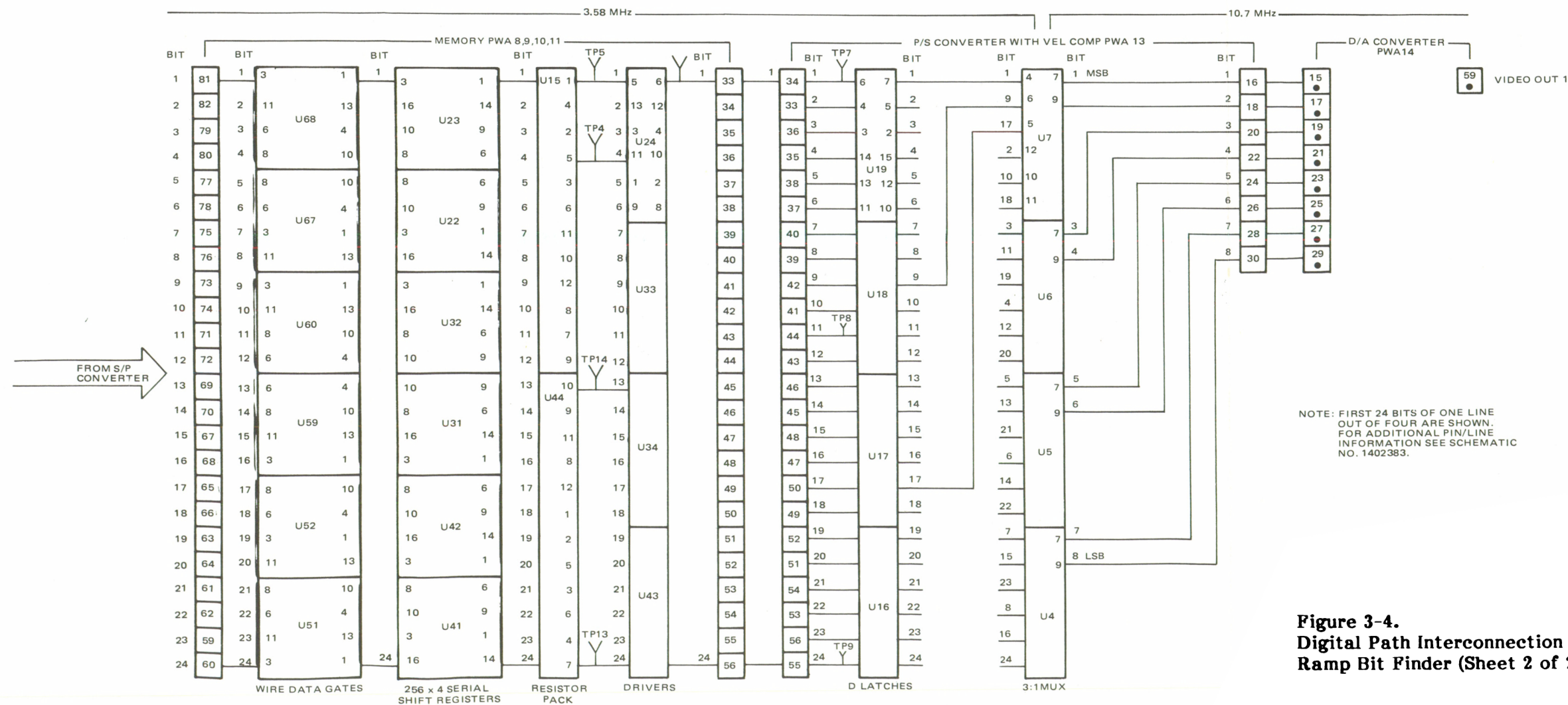
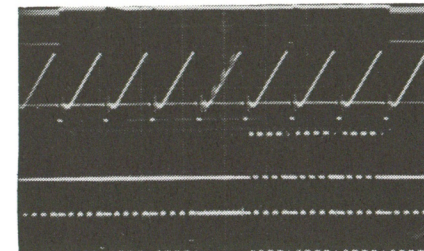


Figure 3-4.
Digital Path Interconnection and Test
Ramp Bit Finder (Sheet 2 of 2)

PART II

SECTION 4

MAINTENANCE INTRODUCTION AND POWER SUPPLY

4-1 INTRODUCTION

In Part II of this manual each of the printed wiring assemblies (PWAs) is presented in a separate section. Within tables and figures, references to the printed wiring assemblies are often abbreviated by PWA number for easy reference. The power supply, which does not have a PWA number, is discussed in this section.

Each PWA section has the same three-part organization:

- Description
- Maintenance
- Reference data

4-2 PWA-LEVEL DESCRIPTION

Theory consists of a general description of the functions of the PWA at the block diagram level. Block diagrams, simplified schematics, and timing waveforms supplement this discussion with additional circuit detail as well as system interconnect information to aid in following functional details not directly addressed in the text. The maintenance procedure should also be studied to round out circuit details for a fuller understanding of the TBC system.

4-3 PWA-LEVEL MAINTENANCE

Maintenance protocol for the TBC-3 is outlined in Section 3 of Part I and should be reviewed before undertaking any adjustments. Be sure to follow the alignment sequence of Table 3-2 to make accurate adjustments. To reduce variables in field testing, isolate the TBC from the VPR using the procedures of paragraph 3-6 and Figure 3-2.

Maintenance procedures are aimed at:

- Reestablishing factory-set parameters following repair or misadjustment.
- Providing the proper context for adjustment of certain controls for unique VTR or facility requirements.
- Providing key data points for fault isolation.

TBC-3

Adjustments should not be made outside the context of a given procedure. Some controls (chiefly filters) are factory-only adjustments. These will be noted in the adjustable controls summaries in the reference section for each PWA. Failure to meet adjustment parameters at any point in the PWA-level procedures may indicate a fault or misadjustment of a prerequisite interactive function. Simplified schematics provide an easy means of tracing an interactive series of adjustments through the system with the use of the interconnect data. Waveforms may also be consulted for normal TBC operation.

4-4 REFERENCE DATA

Reference data at the end of each section supports both the description and maintenance texts and consists of a series of foldouts containing block diagrams, simplified schematics, timing and test waveforms, and other illustrative material. These are listed in the introduction to each section. The introduction also contains a summary of the major functions of the PWA for quick reference.

The arrangement and type of data are the same for each PWA and consist of the following:

- An overall block diagram, providing a functional layout with component designators referenced to the schematics.
- Simplified schematics which can be used for a study of the system and for fault analysis. Use the documents of the parts lists and schematics manual for final proof of faults. In addition to waveform call-outs, these schematics provide calculated one-shot times, counter preloading, and notes on circuit operation. The interconnect data provides a guide to system interactivity.
- Waveform illustrations. Waveforms are referenced in the description and maintenance text using alphanumeric designators such as WF12/WF13 (H). This indexing accommodates the repetition of certain waveform test points for several operational and timing modes. As timing diagrams, waveforms provide a record of normal operation with a VTR.
- Maintenance data is always the last reference sheet in the section and contains information regarding test points, adjustable controls, and jumper summaries as well as a component locator diagram to locate PWA devices called out in the maintenance procedures. Factory-only adjustments are listed in the adjustable controls summary.

4-5 POWER SUPPLY

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual:

Assembly No. 1409155
Schematic No. 1409157

See the following reference information:

Power Supply Block Diagram, Figure 4-1
Power Supply Test and Maintenance Data, Figure 4-2

4-6 Power Supply Description

The power supply transformer/regulator assembly is mounted behind the control panel; the output load transistors are mounted on the rear hinged heat sink panel which also has a 15A circuit breaker. The mechanical configuration is shown on the maintenance access diagram, Figure 3-1 in Part I. Figure 4-1 is a detailed block diagram with interconnections.

4-7 Power Supply Check**Note**

The power supply does not require routine adjustment and should not be adjusted unless the need is well established. Power supply output voltages should be checked under typical line voltages and load conditions.

Fuse requirements, location and normal output voltages are given in Figure 4-2.

Check output voltages as follows:

- STEP 1 Insert PWA extender board into position number 1 of card rack.
- STEP 2 Check voltages at test points given in the *Power Supply Output Limits* table of Figure 4-2.

Note

If all voltages measured in prior steps are within given tolerances, make no adjustment. Even with out-of-tolerance voltage readings, be reasonably assured that an overload is not causing the condition before attempting voltage adjustment. A misadjusted power supply can cause all PWA adjustments to be out of tolerance.

4-8 Power Supply Adjustment

- STEP 1 Referring to the maintenance access diagram, Figure 3-1 in Part I, pull card rack from cabinet. Two controls are seen on the regulator PWA. See the component locator in Figure 4-2 for the test point locations.
- STEP 2 At voltage regulator assembly, connect digital voltmeter between TP8 (REF +12V) and TP6 (REF GND).

CAUTION

EXERCISE CARE WHEN MAKING ADJUSTMENTS. CONTINUOUS OVERVOLTAGE OPERATION OF SOLID-STATE COMPONENTS CAN SHORTEN THEIR LIFE.

Note

The +12V must be adjusted before the -12V.

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- STEP 3** Turn power on and adjust R85 (+12V ADJ) for +12.000V.
- STEP 4** Connect digital voltmeter between TP7 (REF -12V) and TP6 (REF GND).
- STEP 5** Adjust R85 (-12V ADJ) for -12.000V.
- STEP 6** Using digital voltmeter, verify the following sense voltages between TP6 (REF GND) and specified test points:
- a. TP1: +5.000V \pm 0.050V
 - b. TP2: -5.200V \pm 0.100V
 - c. TP3: +12.000V \pm 0.100V
 - d. TP4: -12.000V \pm 0.010V
- STEP 7** Switch power off and return card rack to cabinet.

PART II

SECTION 5

COLOR PROCESSOR PWA 1

DESCRIPTION AND MAINTENANCE

5-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual:

Assembly No. 1463589
Schematic No. 1406117

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section.

- Figures 5-1 and 5-2, overall block diagrams
- Figures 5-3 and 5-4, simplified schematics
- Figure 5-5, waveform illustrations
- Figure 5-6, maintenance data

Color Processor PWA 1 functional summary:

- The processed video output maintains a coherent relationship between the subcarrier and the leading edge of the horizontal sync pulse (sync-coherent 3.58 MHz) for single-wire heterodyne EIAJ video and VPR slow-motion and still-frame modes of operation.
- For slow-motion and still-frame, the frame/2 signal from Memory Control PWA 6 alternates the phase of the chroma signal to simulate a color frame.
- In the single-wire heterodyne mode, the B-Y and R-Y components are decoded synchronously by locking a 3.58-MHz crystal VCO to the decoded R-Y component. The B-Y and R-Y components of the signal are then encoded using the sync-coherent 3.58-MHz clock from the Tape H Comparator PWA.
- The two-wire heterodyne system functions as previously described, except the color processing is accomplished by circuitry in the heterodyne VTR. In the two-wire system, sync coherent subcarrier is routed back to the VTR so that remodulation can take place within the VTR.

5-2 DESCRIPTION

Color Processor PWA 1 performs a dual function. It permits the TBC to be used with a VPR in slow motion and also with a heterodyne VTR. The heterodyne VTR must be of the nonsegmented helical-scan type.

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A heterodyne VTR produces a video output signal with a sync-coherent luminance component but with a chrominance component that is not sync coherent. Before this signal can be time-base corrected, the sync coherence of the chrominance signal must be reestablished. To do this, the Color Processor PWA strips chrominance from the video and demodulates this chrominance with an off-tape, burst-derived 3.58-MHz subcarrier. The Color Processor PWA then remodulates the chrominance with a sync-coherent subcarrier and adds it to luminance, providing a video signal containing sync-coherent luminance and chrominance that produces a standard NTSC signal after time base correction.

During slow motion or still framing, the VPR plays back a single recorded field repeatedly. During slow-motion operation, a recorded field is played back many times before the next field is played back. As a result, the phase of the off-tape chroma may be identical through field after field, and for long periods of time. This is inconsistent with NTSC requirements for a 180° phase reversal of the subcarrier between fields. While being supplied with still-frame or slow-motion video from a VPR, the Color Processor PWA maintains chroma phasing necessary to simulate the four-field color frame of the NTSC signal. The PWA does this by separating chrominance from luminance and then providing inverted and noninverted chrominance simultaneously at an electronic switch input.

Memory Control PWA 6 provides this switch signal to either the inverted or noninverted chroma.

5-3 Heterodyne Processing

When the NORMAL/HET switch on the TBC-3 front panel is set to HET, the Color Processor PWA processes off-tape video from a heterodyne-type VTR. The video signal from the VTR enters the color processor on PWA pin 21. The luminance low-pass filter and the chroma bandpass filter separate the video signal into its chrominance and luminance components. The luminance-delay circuit delays the luminance by the same amount of time that the chroma-processing circuit delays the chrominance. This ensures that the phasing of the two components is unchanged when they are added at the video amplifier. The chroma output of the chroma bandpass filter is separated into its B-Y and R-Y components in the B-Y and R-Y decoders, respectively. The decoders are synchronous detectors with the 3.58-MHz decoding signal developed from the off-tape burst.

B-Y and R-Y video components are encoded in B-Y and R-Y encoders, which are balanced modulators. The carrier used in the encoding process is a sync-coherent 3.58-MHz signal developed by Tape H Comparator PWA 4. Sync-coherent B-Y and R-Y components are summed together to form the required sync-coherent chrominance. The chrominance is applied through switch U12 to current source Q27. The chrominance is then added to the luminance in the video output amplifier. The resulting sync-coherent video is passed through a 4.5-MHz low-pass filter and then through emitter-follower Q31 to PWA pin 81. The dc level of the video signal provided at PWA pin 81 is clamped by a feedback loop comprised of sample-and-hold amplifier U14, Q24, and current source Q27. The sample-and-hold amplifier samples the level of the back porch and compares it with a reference value developed by potentiometer R189. The difference in the compared voltages is

amplified and provided through a current source to alter the bias of the video output amplifier to establish the dc level. The sampling circuit in the sample-and-hold amplifier is driven by the clamp pulse driver U13/Q23 which amplifies the video clamp pulses applied to the PWA at pin 47 by the Tape VCO PWA 5.

The crystal VCO generates the 3.58-MHz signal used by B-Y and R-Y decoders. The off-tape burst determines the phase of the 3.58-MHz signal. Under timing control of the sync logic circuits, the crystal-controlled circuit samples the output of the R-Y decoder during burst time. The crystal oscillator maintains the phase of burst on a line-by-line basis. The burst is not H-sync-coherent. If the decoder oscillator follows the cyclic variations of burst phase, the chroma is decoded to a true dc equivalent of the chroma phase vector. Re-encoding of the chroma signal with the sync-coherent subcarrier establishes a chroma signal that can be processed by the TBC to produce a standard NTSC signal.

The sync-coherent 3.58-MHz driver receives the sync-coherent 3.58-MHz signal from Tape H Comparator PWA 5, reshapes it into a sinusoid, and produces the 3.58-MHz drive current required by B-Y and R-Y encoders.

5-4 Slow-Motion and Still-Frame Processing

When the NORMAL/HET switch on the TBC front panel is set to NORMAL, the Color Processor PWA processes video from the VTR operating in slow motion or still frame. At tape speeds other than normal, the Color Processor PWA inverts the chroma component of the video as required to simulate the NTSC four-field color frame. Luminance and chrominance are separated as described previously in the paragraph on heterodyne processing. The chroma signal from the chroma bandpass filter is applied to a chroma inverter circuit. The chroma inverter circuit either inverts or transmits the chroma signal directly. Direct or inverted transmission through this circuit is under control of the frame/2 signal produced by Memory Control PWA 6. During still-frame playback this signal varies in proportion to the speed of the tape during slow-motion operation. Chroma is added to luminance in the video output amplifier in the same way as it was in heterodyne processing.

5-5 MAINTENANCE

See Figure 5-5 for the waveform illustrations and Figure 5-6 for the test point, jumper, and adjustable components information, and locator diagram called out in the following procedures.

Before undertaking any adjustments to the Color Processor PWA review the system alignment sequence in Table 3-2 and the tape/reference test loop discussion of paragraph 3-6, Part I, for an understanding of the nature and scope of these field adjustments. Also consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the color processor and interactive functions between it and other PWAs.

5-6 Heterodyne Section Alignment

Use basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN. With power off put Color Processor PWA on an extender.

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5-7 Chroma and Subcarrier Oscillator Alignment

- STEP 1** Adjust R22 (chroma level) fully clockwise for maximum chroma. Monitor at TP9 with oscilloscope triggered on pin 47 (clamp pulse).
- STEP 2** Switch off burst at signal generation.
- STEP 3** Set jumper J1 to B-C position.
- STEP 4** Connect oscilloscope or digital voltmeter to TP4 for dc voltage measurement.
- STEP 5** Adjust R7 (crystal control offset) for $+3.5 \text{ Vdc} \pm 0.5 \text{ Vdc}$.
- STEP 6** Return burst to test signal.
- STEP 7** Connect oscilloscope to TP3; trigger on internal.
- STEP 8** Set jumper J1 to A-B position.
- STEP 9** Adjust L2 (VCO peaker) for maximum subcarrier.
- STEP 10** Connect oscilloscope to TP7; trigger on internal.
- STEP 11** Set MODE switch to HET.
- STEP 12** Adjust R144 (sync coherent subcarrier symmetry) and L8 (sync coherent subcarrier peaker) for maximum subcarrier.

5-8 Decode and Encode Circuit Alignment

- STEP 1** Set MODE switch to HET.
- STEP 2** Switch off R-Y chroma at signal generator.
- STEP 3** Connect oscilloscope to TP8; trigger on pin 47 (video clamp pulse in).
- STEP 4** Adjust R7 (crystal control offset) so that transition spikes shown in bottom trace of WF16(J) are set to zero level as indicated in top trace.
- STEP 5** Return R-Y chroma to test signal.
- STEP 6** Switch off B-Y chroma at signal generator.
- STEP 7** Connect oscilloscope to TP10; trigger on pin 47.
- STEP 8** Adjust L3 (decode quadrature) to reduce transition steps to zero level. Bottom trace of WF17(K) shows a misadjustment L3; top trace shows correct adjustment.
- STEP 9** Return B-Y chroma to test signal.

- STEP 10** Connect oscilloscope to TP19; trigger on pin 47.
- STEP 11** Set R47 (R-Y gain) to midposition.
- STEP 12** Adjust R48 (R-Y balance) and R108 (B-Y balance) for minimum rf on horizontal sync.
- STEP 13** Connect channel A of vectorscope to TP19 or VIDEO OUT 1.
- STEP 14** Trigger vectorscope on external subcarrier.
- STEP 15** Switch R-Y off at signal generator.
- STEP 16** Set vectorscope phase so vector is aligned vertically at 90° on graticule.
- STEP 17** Switch R-Y on, B-Y off at signal generator.
- STEP 18** Adjust L14 (encode quadrature) so vector is aligned horizontally at 180° on the graticule. This vector should be 90° from vector in step 16.
- STEP 19** Switch vectorscope to internal BURST D REF.
- STEP 20** Set jumper J1 to B-C position.
- STEP 21** Set vectorscope gain to maximum.
- STEP 22** Misadjust L1 (VCO frequency) slightly for an approximately 30-Hz beat of vector dot at center.
- STEP 23** Adjust R48 and R108 for minimum circle around dot at center of vectorscope.
- STEP 24** Set vectorscope gain to 75%.
- STEP 25** Adjust L19 (chroma peaker) for maximum chroma as seen on vectorscope (or on oscilloscope connected to TP15).
- STEP 26** Adjust R47 (R-Y gain) and L3 (decode quadrature) for minimum dot size at ends of vectors. A gross misadjustment of R47 is shown in WF18(L).
- STEP 27** Adjust L1 for 5.00 Vdc at TP4.

5-9 Heterodyne/VPR Slow-Motion Output

Note

Chroma and luminance level controls are optimized at the factory for common slow-motion and heterodyne circuit functions. This procedure is used only to adjust chroma and luminance levels to accommodate a particular heterodyne VTR and to readjust chroma gain of the slow-motion chroma inverter circuit for unity gain chroma of both circuit functions.

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5-10 Normal Output Level Adjustment

- STEP 1** Use tape/reference test loop with a terminated oscilloscope looped through vectorscope channel A connected to VIDEO OUT 1. Switch signal generator video off for a color black signal.
- STEP 2** With power off extend Color Processor PWA.
- STEP 3** Set MODE to HET.
- STEP 4** Observe one video line. Adjust R189 (clamp dc level) for zero blanking level. Slight tilt of video line should be averaged across zero and be the same for normal and heterodyne modes.
- STEP 5** Return 75% color bar to the input.
- STEP 6** Alternately select HET and NORMAL positions of MODE switch and adjust R193 (luminance level) for luminance in heterodyne to be the same as in normal.
- STEP 7** Alternately select HET and NORMAL positions of MODE switch and adjust R22 (chroma level) for chroma amplitude in heterodyne to be the same as in normal.

5-11 Chroma Inverter Adjustment

- STEP 1** Select still frame at the VPR.
- STEP 2** Adjust L18 (chroma peaker) for maximum chroma level.
- STEP 3** Adjust R178 (chroma invert gain balance) for minimum dot bounce on vector display.
- STEP 4** Alternately select HET and NORMAL positions of MODE switch and adjust R223 (chroma invert gain) for chroma amplitude in heterodyne to be the same as in still frame (NORMAL position).
- STEP 5** With power off return PWA to cage.

5-12 Filter Alignment

CAUTION

THIS PROCEDURE IS PROVIDED AS A REFERENCE ONLY AND SHOULD NOT BE ATTEMPTED WITHOUT A SPECTRUM ANALYZER AND VIDEO SWEEP GENERATOR. THERE SHOULD NOT BE ANY REQUIREMENT FOR A COMPLETE ALIGNMENT OF THE CHROMINANCE AND LUMINANCE FILTERS. EVEN FOLLOWING AN ACTIVE COMPONENT FAILURE, ALIGNMENT SHOULD BE RESTRICTED TO THE AFFECTED CIRCUIT.

5-13 Luminance and Chrominance Filter Alignment

- STEP 1** Remove test signal from TAPE VIDEO IN connector.
- STEP 2** Connect sweep generator to TP1. Set sweep generator for 1.5 Vp-p.
- STEP 3** Connect spectrum analyzer to TP19.
- STEP 4** Set MODE switch to HET.
- STEP 5** Set jumper J2 to B-C position.
- STEP 6** Set jumper J6 to B-C position.
- STEP 7** Adjust L9 (luminance low-pass filter) for minimum 3.671 MHz.
- STEP 8** Adjust L10 (luminance low-pass filter) for minimum 3.438 MHz.
- STEP 9** Set jumper J8 to B-C position.
- STEP 10** Adjust L15 (luminance low-pass filter) for minimum 1.576 MHz.
- STEP 11** Return jumper J8 to A-B position.
- STEP 12** Set jumper J10 to B-C position.
- STEP 13** Adjust T1 (luminance low-pass filter) for minimum 1.576 MHz.
- STEP 14** Return jumper J10 to A-B position.
- STEP 15** Set jumper J7 to A-C position.
- STEP 16** Set jumper J9 to B-C position.
- STEP 17** Adjust L16 (luminance low-pass filter) for minimum 4.301 MHz.
- STEP 18** Return jumper J9 to A-B position.
- STEP 19** Set jumper J11 to B-C position.
- STEP 20** Adjust T2 (luminance low-pass filter) for minimum 4.301 MHz.
- STEP 21** Return jumper J11 to A-B position.
- STEP 22** Return jumper J7 to A-B position.
- STEP 23** Set MODE to NORMAL.
- STEP 24** Connect oscilloscope to TP14.
- STEP 25** Adjust L18 (chroma peaker) for peak in response at 3.58 MHz.

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- STEP 26 Set jumper J15 to B-C position.
- STEP 27 Adjust L23 (chroma invert filter) for minimum 3.891 MHz.
- STEP 28 Return jumper J15 to A-B position.
- STEP 29 Set jumper J16 to B-C position.
- STEP 30 Adjust T4 (chroma invert filter) for minimum 3.891 MHz.
- STEP 31 Return jumpers J2, J6, and J16 to respective A-B position.
- STEP 32 Connect spectrum analyzer to TP9.
- STEP 33 Set MODE to HET.
- STEP 34 Adjust L6 (chroma band-pass filter) for minimum 2.000 MHz.
- STEP 35 Adjust L7 (chroma band-pass filter) for minimum 7.16 MHz.

5-14 Decode Filter Alignment

- STEP 1 Connect 75% color-bar test signal at standard level to TAPE VIDEO IN connector.
- STEP 2 Connect oscilloscope to TP10.
- STEP 3 Trigger oscilloscope from pin 47 (video clamp pulse in).
- STEP 4 Adjust L12 (B-Y decode filter) and L13 (B-Y decode filter) for squarest corner of greatest chroma transition (sharpest transition of chroma with no ringing or overshoots.).
- STEP 5 Connect oscilloscope to TP8.
- STEP 6 Trigger oscilloscope from pin 47.
- STEP 7 Adjust L4 (R-Y decode filter) and L5 (R-Y decode filter) for squarest corner of greatest chroma transition (sharpest transition of chroma with no ringing or overshoots).

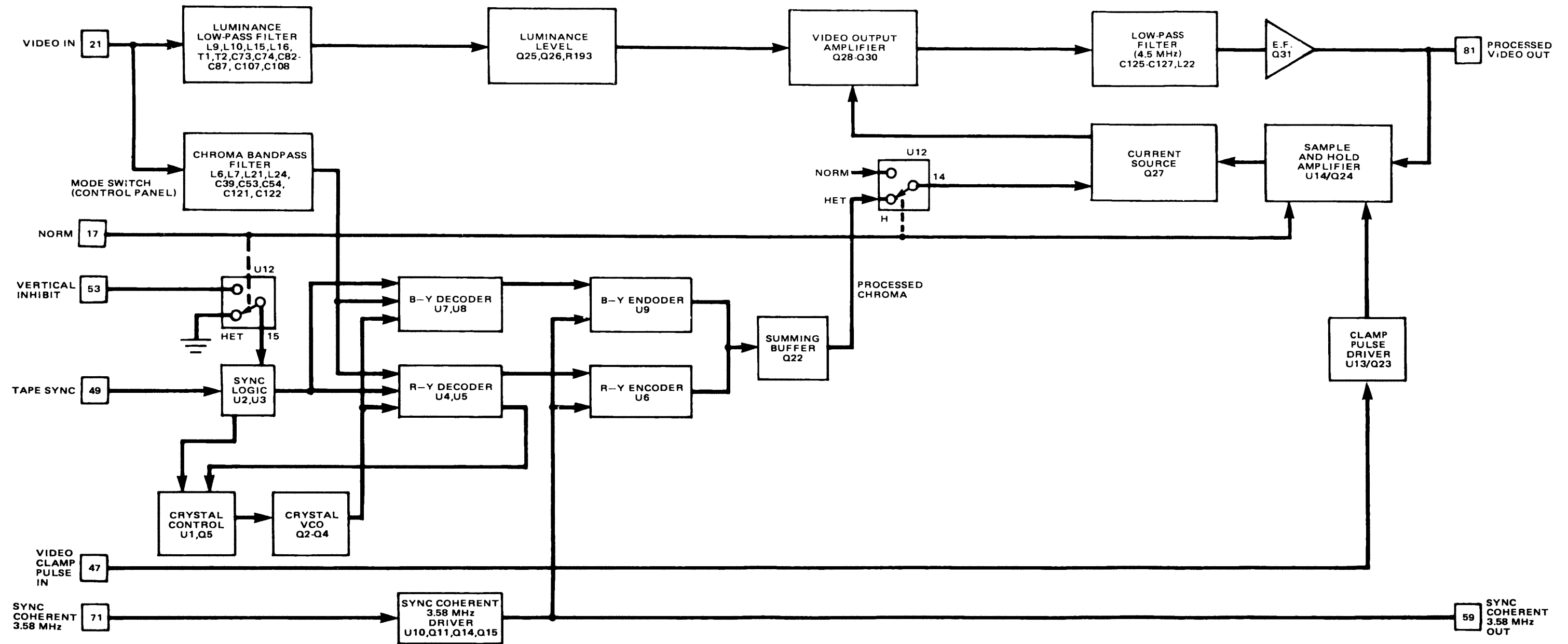


Figure 5-1.
Heterodyne Processing Mode, Color Processor
PWA 1, Simplified Block Diagram

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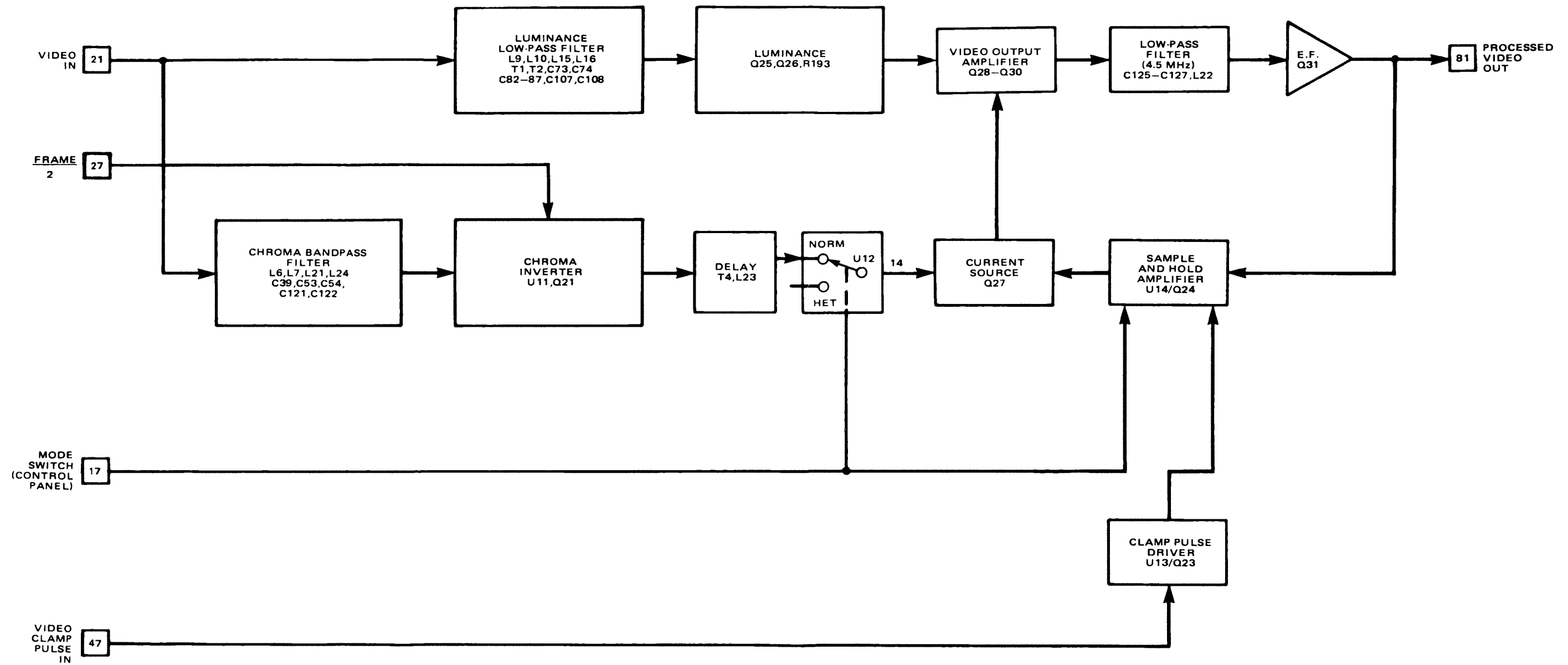


Figure 5-2.
Slow Motion Processing Mode, Color Processor
PWA 1, Simplified Block Diagram

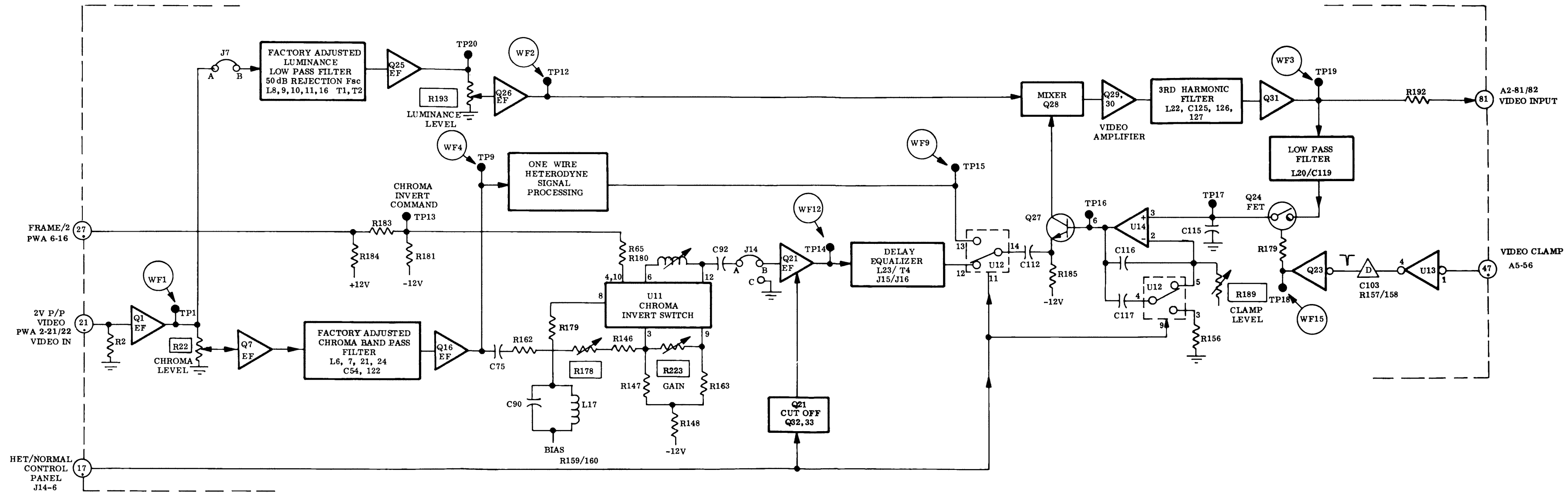


Figure 5-3.
Slow Motion Chroma Processor, Simplified Schematic
Color Processor PWA 1

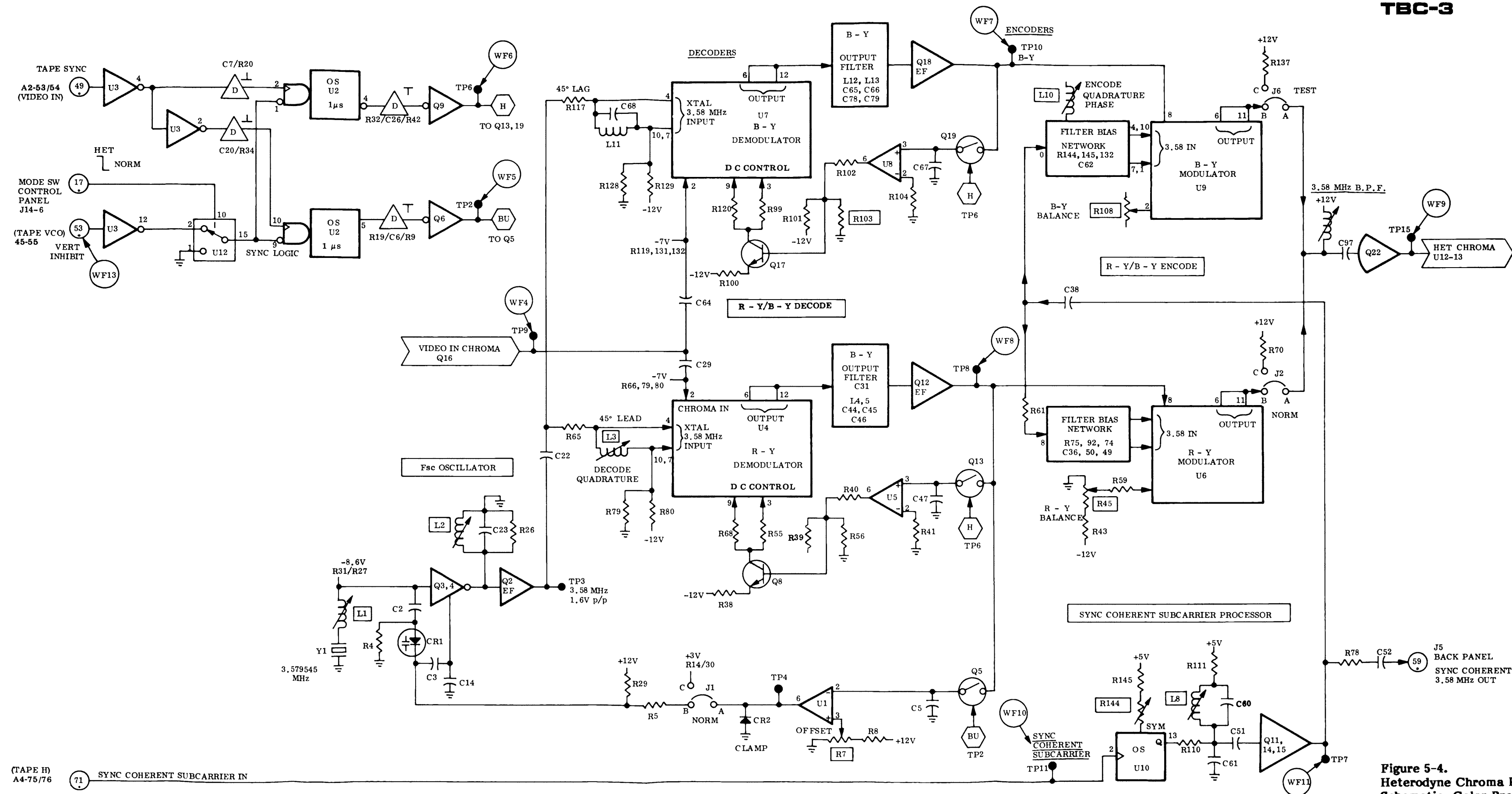


Figure 5-4.
Heterodyne Chroma Processing Simplified
Schematic, Color Processor PWA 1

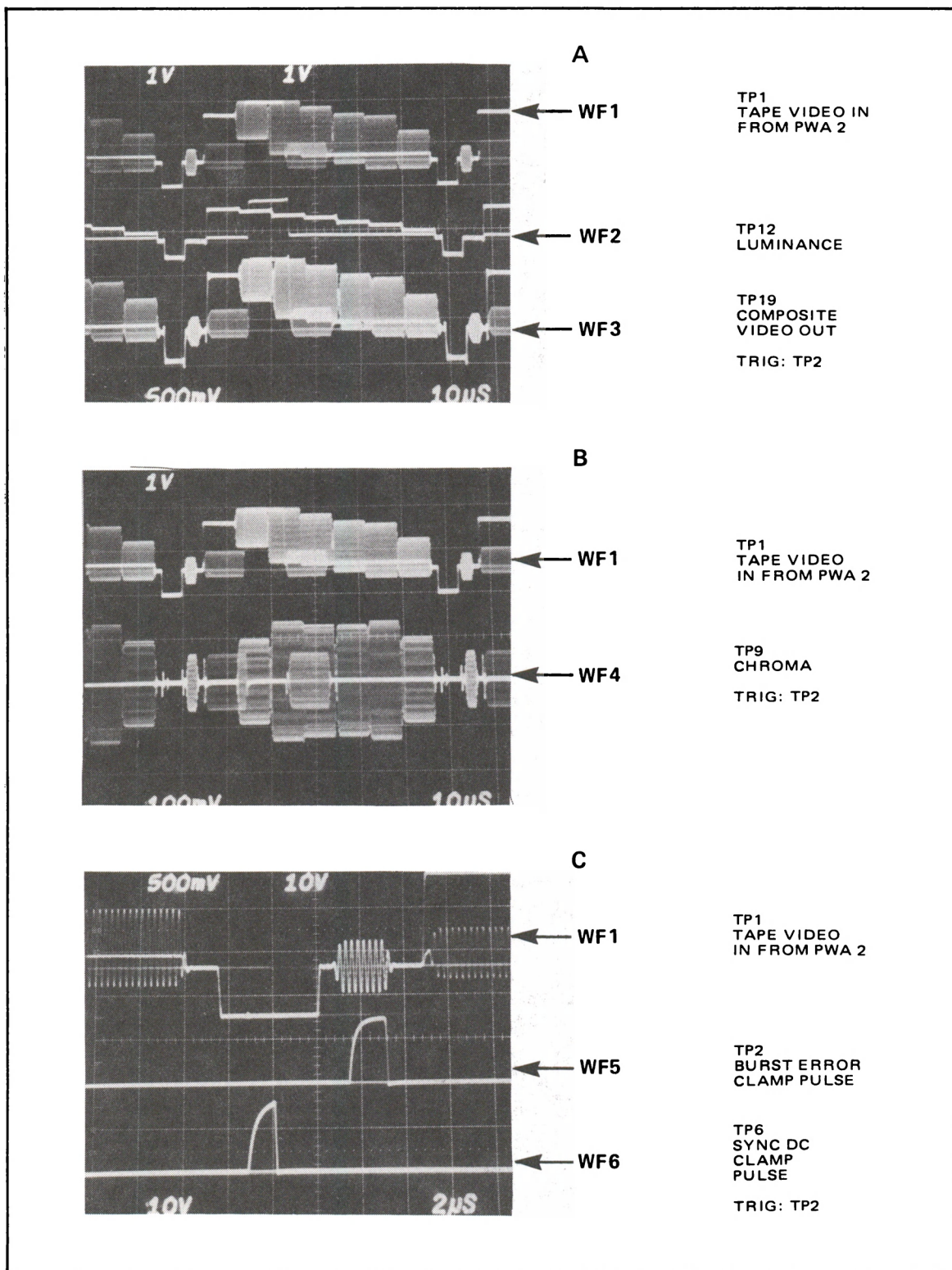


Figure 5-5. Color Processor PWA 1 Waveforms (Sheet 1 of 4)

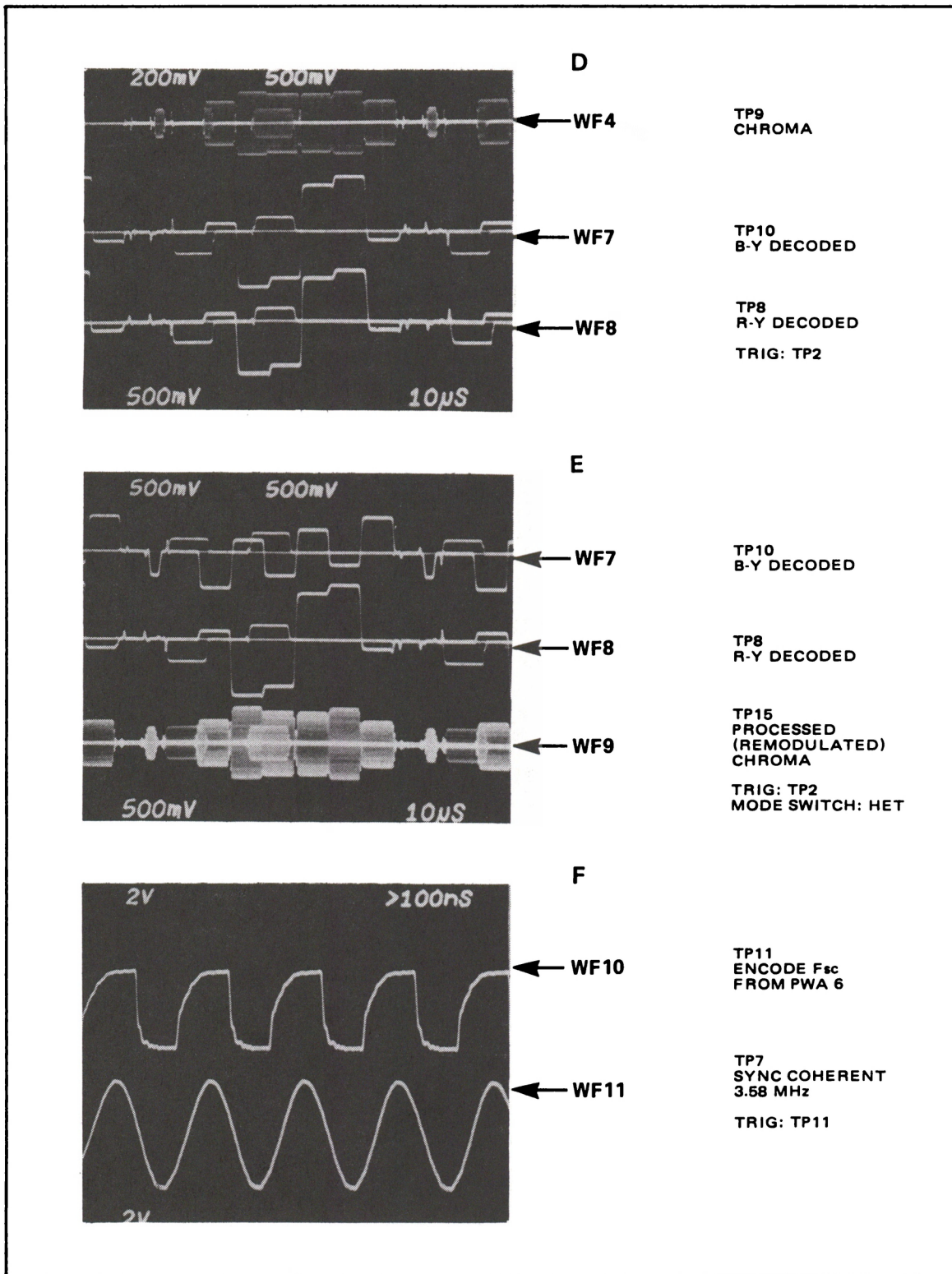


Figure 5-5. Color Processor PWA 1 Waveforms (Sheet 2 of 4)

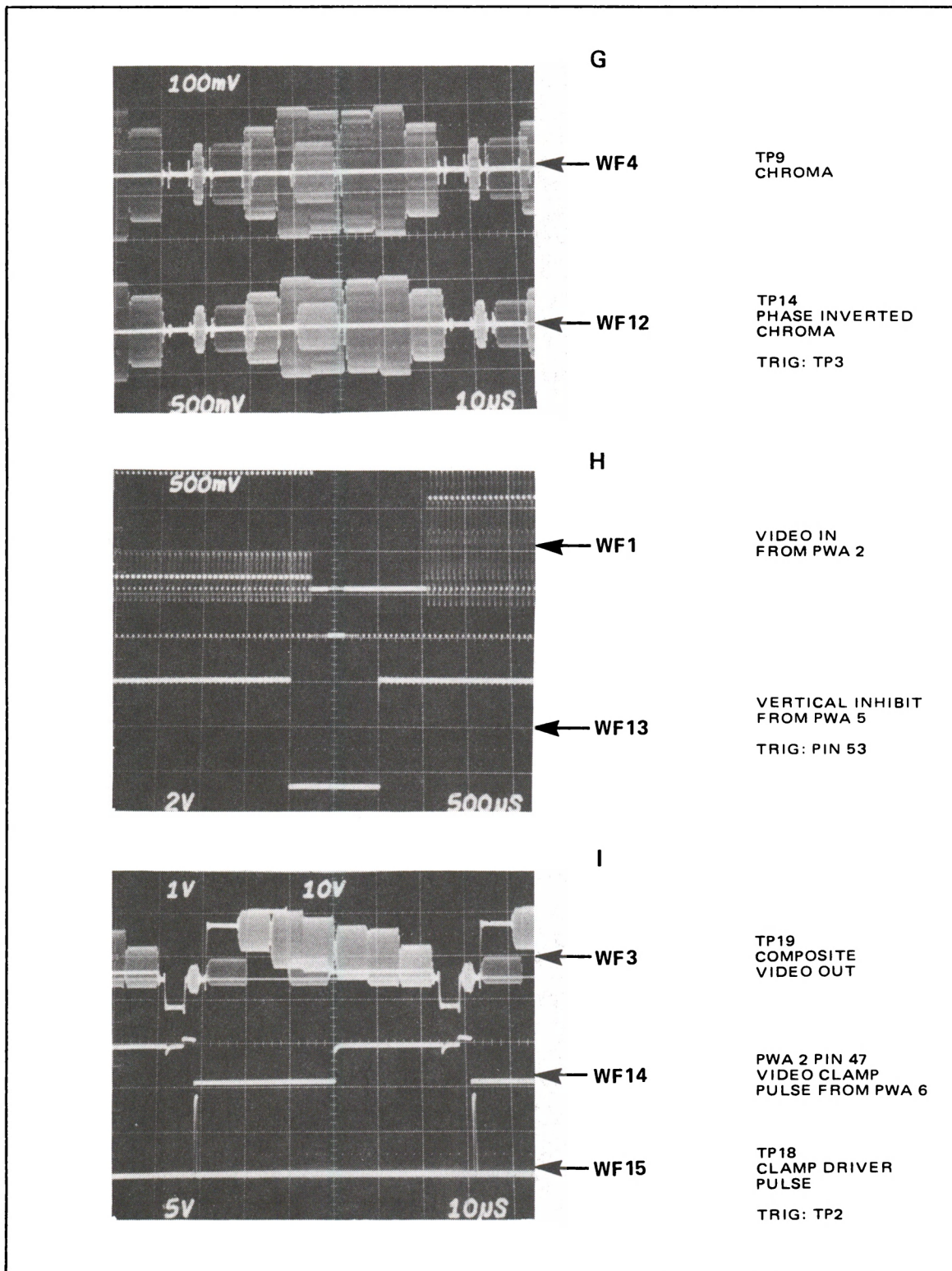


Figure 5-5. Color Processor PWA 1 Waveforms (Sheet 3 of 4)

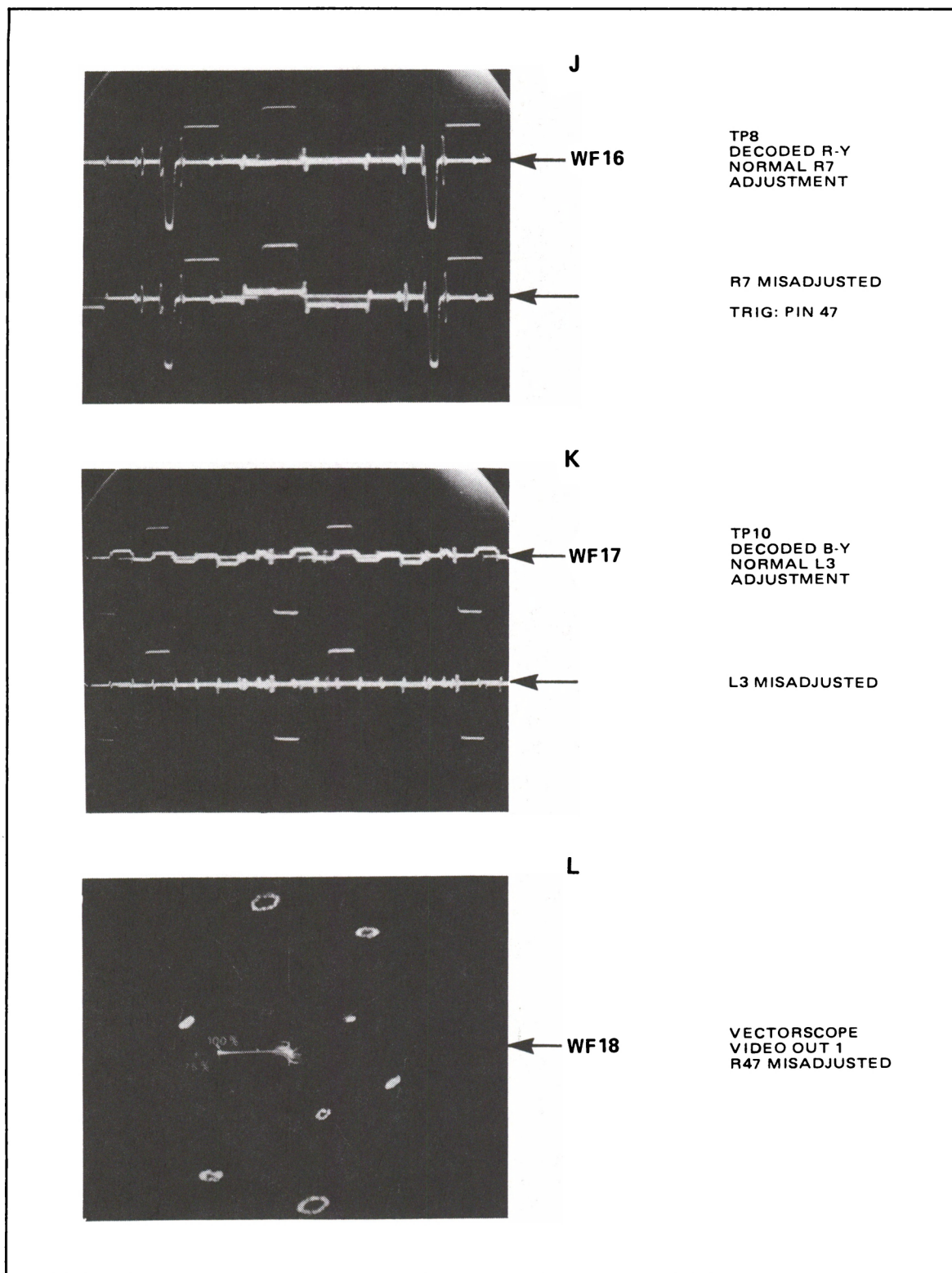
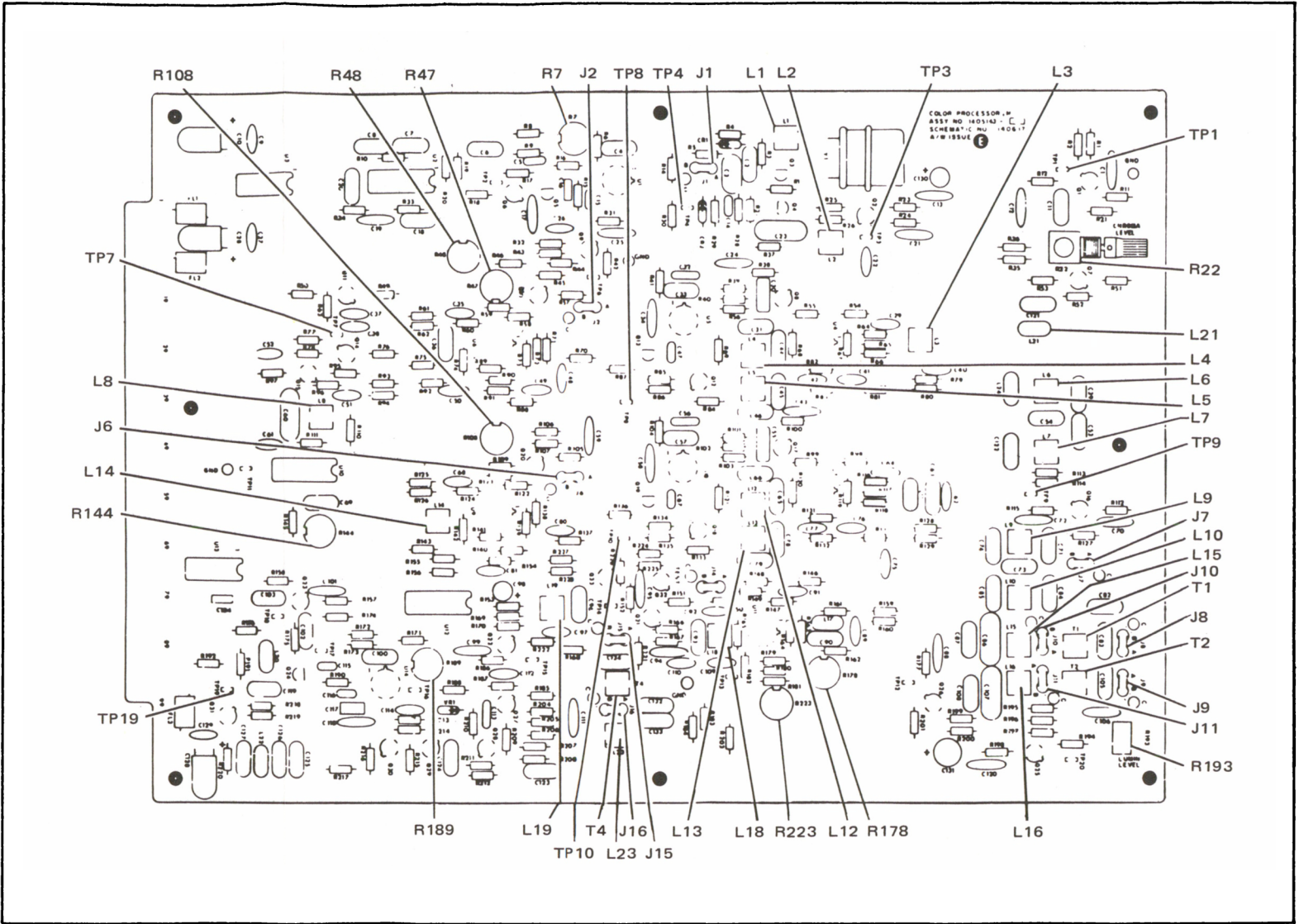


Figure 5-5. Color Processor PWA 1 Waveforms (Sheet 4 of 4)

PWA 1 Jumpers		
Jumper	Position-Function	
J1	A-B	Normal
	B-C	Test--fixed error voltage to crystal oscillator
J2	A-B	Normal
	B-C	Test--removes R-Y encoder
J6	A-B	Normal
	B-C	Test--removes B-Y encoder
J7	A-B	Normal
	A-C	Test--luminance low pass filter alignment
J8	A-B	Normal
	B-C	Test--luminance low-pass filter alignment
J9	A-B	Normal
	B-C	Test-- luminance low-pass filter alignment
J10	A-B	Normal
	B-C	Test-- luminance low-pass filter alignment
J11	A-B	Normal
	B-C	Test-- luminance low-pass filter alignment
J14	A-B	Normal
	B-C	Test--remove chroma inverter
J15	A-B	Normal
	B-C	Test--chroma invert delay filter alignment
J16	A-B	Normal
	B-C	Test--chroma invert delay filter adjustment

PWA 1 Adjustable Components	
Component	Function
L1	VCO frequency
L2	VCO peaker
L3	Decode quadrature
L4*	R-Y decode filter
L5*	R-Y decode filter
L6*	Chroma band-pass filter
L7*	Chroma band-pass filter
L8	Sync coherent subcarrier
L9*	Luminance low-pass filter
L10*	Luminance low-pass filter
L12*	B-Y decode filter
L13*	B-Y decode filter
L14	Encode quadrature
L15*	Luminance low-pass filter
L16*	Luminance low-pass filter
L18	Chroma peaker (Norm)
L19	Chroma peaker (Het)
L23*	Chroma invert filter
R7	Crystal control offset
R22	Adjusts chroma level
R47	R-Y gain
R48	R-Y balance
R108	B-Y balance
R144	Sync coherent subcarriers
R178	Chroma invert gain balance
R189	Clamp dc level
R193	Adjusts luminance level
R223	Chroma invert gain
T1*	Luminance low-pass filter
T2*	Luminance low-pass filter
T4*	Chroma invert filter
*Factory Adjustment Only	

Test Point	Function
TP1	Video input
TP2	Burst error clamp pulse
TP3	Decode subcarrier
TP4	Decode oscillator error
TP6	Sync dc clamp pulse
TP7	Sync coherent subcarrier output
TP8	R-Y chroma
TP9	Chrominance
TP10	B-Y chroma
TP11	Sync coherent subcarrier input
TP12	Luminance
TP13	Chroma invert frame/2
TP14	Inverted chroma
TP15	Processed chroma
TP16	Video clamp error
TP17	Video clamp sample
TP18	Video clamp pulse
TP19	Processed video out
TP20	Luminance



PWA 1 Component Locator

Figure 5-6.
Test Points, Jumpers, Adjustable Components,
Component Locator, Color Processor PWA 1

PART II

SECTION 6

VIDEO INPUT PWA 2

DESCRIPTION AND MAINTENANCE

6-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463650

Schematic No. 1463652

The following figures to which PWA descriptions and maintenance procedures refer are located at the end of this section:

- Figures 6-1 and 6-3, simplified block diagrams
- Figures 6-4 and 6-5, simplified schematics
- Figure 6-6, waveform illustrations
- Figure 6-7, maintenance data

Video Input PWA 2 function summary:

- Provides black level clamping and amplification of off-tape video signal.
- Switches to enable direct video or processed EIAJ video from Color Processor PWA.
- Switches between input or TBC-processed video to the video monitor.
- Strips sync and burst from input video for processing in the Tape H Comparator PWA.
- Provides jumper-selectable test ramp signal.
- Contains video low, video overload, and color presence detectors.
- Detects search mode.

6-2 DESCRIPTION

Video Input PWA 2 accepts off-tape video from the associated VTR, amplifies the signal to a standard amplitude level, and clamps the back porch to a 0V reference level. When used with an Ampex VPR, the output video signal is routed to Analog-to-Digital Converter PWA 3. In slow-motion or still mode, or when used with a heterodyne-process VTR, the signal is routed to the Color Processor PWA 1. After processing by Color Processor PWA 1 the video signal is sent back to the Video Input PWA 2 where black-level reference is inserted into the H-sync tip. The resultant video signal is then sent to A/D Converter PWA 3.

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The Video Input PWA also strips H-sync pulses from the video. These pulses are processed to produce various timing signals for use within the TBC system. Several features are provided to prevent incoming noise from introducing erroneous sync. Reference subcarrier (Fsc) burst is stripped from off-tape video and gated to the Tape H Comparator PWA 4. The presence or absence of burst is detected and converted to a TTL-level burst-present signal.

If edit mute is operated or if no video is present, Video Input PWA 2 provides a video mute signal to Sync Generator PWA 15. This signal locks the blanking signal supplied to Video Output PWA 2 to the on condition, thereby blanking out the video display. Composite video from the Video Output PWA 14 or off-tape video may be selected by MONITOR/VIDEO for routing from Video Input PWA 2 to the MONITOR VIDEO OUT connector. Video overload and low video detectors provide signals to lamps on the control panel for indication of abnormal amplitude conditions in Video Input PWA 2.

6-3 Tape H Control Signal Generator

See Figure 6-1 and Figure 6-6. Off-tape video entering the PWA at pin 15 is amplified by x5 amplifier Q37/U13 and stripped of chroma by series-resonant 3.58-MHz filter trap L11/C93. The stripped video is inverted by buffer U26. Leading and trailing edges of H-sync are defined by one-shots which operate sample-and-hold circuits. The leading-edge pulse samples the value of sync tip; the trailing-edge pulse samples the value of back porch. Stored values are summed and used as a reference for the 50% slice level detector (comparator) U40-9. H-sync from amplifier U26 is compared with the summed reference in U40-9 to establish the 50% sync point.

Normal video from the input gain amplifier is supplied to sync stripper logic circuits which extract horizontal sync from off-tape video. The sync stripper logic circuits consist of crude sync level detector Q34/U42/U41-1, crude sync slicer U28-7, and 50% slice level detector U40-9. Output of the sync stripper logic is the 50% sync pulse (composite sync).

Inverted video at U48-4 goes to the crude sync level detector which provides a reference level at approximately 25% of the difference between the sync tip and the back porch. This crude sync level provides a reference used by the crude sync slicer U28-7. The crude sync slicer is a level comparator supplying the trigger to the sampling one-shots in the 50% sync level detector circuitry, and also supplying the 50% sync pulse during color shuttle. The 50% sync level detector consists of two dual one-shots U16/U18 and two sampling voltage followers U29. Back porch sampler one-shots U16-5/U18-5 and sync-tip sampler one-shots U16-13/U18-13 are timed to sample the video during the back porch and during the sync-tip intervals, respectively. The voltages from the samplers are summed to provide a reference level half way between the sync-tip voltage and the back-porch voltage (50%). This reference voltage is supplied to 50% slice level detector comparator U40-9. The comparator compares the reference level with the inverted video and provides the 50% sync pulse if color shuttle is not active.

Sample-and-hold circuits have a relatively long time constant. During the vertical inhibit signal from Tape VCO PWA 5, sampling is inhibited, therefore the 50% slice

level will not be disturbed by 2H pulses. If a dropout present signal is received from the dropout compensator (PWA 7), sampling will also be inhibited.

Equalization pulses are used to detect the vertical interval. The noise gate sync goes to an equalizer pulse vertical detector. The noise gate sync triggers 3.0- μ s one-shot U21-13 whose output is gated by U22 to counters U20. When the equalizing pulses are gated to counter U20-9, it triggers equalizer vertical delay one-shots U21-12 and U19-3 which provide a tape vertical pulse to Tape H and Tape VCO PWAs. The equalizer vertical detector and delay circuits also inhibit subsequent equalizer pulses from retriggering during the tape vertical.

6-4 Servoed Pulse Generator and Sync Rate Detector

See Figures 6-1 and 6-2. The function of the servoed pulse generator is:

- To provide system timing pulses derived from tape H-sync.
- To provide an H-rate analog voltage proportionate to tape speed.

Functions of the sync rate detector are:

- To provide a TTL level signal to kill the burst signal from Video Output PWA 14 if tape speed is greater than $\pm 10\%$ of normal.
- To generate a mute signal for routing to Sync Generator PWA 15 if there is a loss of input signal.

To provide a window for ramp-delayed H-pulses occurring at a constant rate, the most elementary circuit is one which inhibits input for the time period between pulses. This could be done with a one-shot having a fixed time constant. Since the VPR can be operated in shuttle, slow-motion, and still modes, and because of time-base errors introduced in the recording/reproduction process, the guarded interval between ramp-delayed H-pulses must be servoed to track the stretching and shrinking of the horizontal line period as tape speed varies. This is done by servoing the timing circuit of the guard interval producing one-shot to the repetition rate of the received ramp-delayed H-pulse. In this way, the period of the one-shot tracks changes in the repetition rate of the ramp-delayed H-pulses. The servoed pulse generator produces a voltage proportional to H-rate. This voltage is fed back to the timing circuit of the servoed pulse generator one-shots to produce the required servo or tracking action.

Figure 6-2 shows the H-rate analog dc voltage (TP10) supplied as a function of tape speed by the servoed pulse generator. This voltage is used as a horizontal gate control for the sync rate detector. Also shown in the figure are the relationships of the sync rate detector output narrow/wide (wide -), up/down, and color shuttle (+) signals generated for a given tape speed. The up/down and narrow/wide signals are used to steer the oscillators on the Tape VCO 5 PWA. The color shuttle (+) voltage turns off burst if shuttle speed exceeds $\pm 10\%$.

The following paragraphs describe circuit operation. Sync rate detector U17/U22/U37/U38 is preceded by servoed pulse generator U34/U35/U45-8/U50-4/-U33-1/Q30-Q33 which prevents noise from entering the sync rate detector and

TBC-3

being read as H-pulses. The servoed pulse generator creates a window or period of time when a pulse can be gated through to the Tape VCO PWA via pin 35, gated sync (-). The window signal from one-shot U34-5 enables one-shot U35-5 only when a ramp-delayed H-pulse is expected to arrive. One-shot U35-5 is disabled at all other times in the guarded interval between the window signal. This eliminates all noise pulses that may be present outside the window.

The ramp-delayed H-pulse triggers 8- μ s one-shot U35-5, and the trailing edge of the pulse at U35-5 triggers servoed one-shot, U34-5, which has a nominal time-constant of 54 μ s. Input one-shot U35-5 is inhibited during this period. The trailing edge of the pulse at U34-12 triggers a nominal 2.8- μ s one-shot U34-13. The positive pulse from U34-13 overlaps the positive pulse from U34-5 throughout the operating range of the shuttle mode of operation, with minimum overlap at +30% H-rate. The integrating capacitor across amplifier U33-1 receives maximum positive charge at -50 times H-rate and minimum positive charge at +50 times H-rate. Voltage developed at pin 2 of U33-1 determines the charge rate of the RC circuit of U33-1. Thus, a window of approximately 13 μ s is provided for the incoming H-pulse. The same H-rate analog voltage is applied to current sources Q41/Q35 to change the delays of one shots U54-4 and U43-4. The H-rate analog voltage from U33-1 is also applied to comparator, U32-14, which will go low if the analog voltage falls below +1V, indicating video is not present at the input connector panel of the TBC.

The sync rate detector provides a TTL-level signal to indicate whether tape speed is less than or greater than $\pm 10\%$ of normal. The two signals are ANDed to produce a color-present signal (color/mono) for use within the TBC and to kill the burst signal from the Video Output PWA 14 when burst is not present or when tape speed exceeds $\pm 10\%$ of normal. Shuttle forward causes a net increase in tape H-rate; in shuttle reverse the result is a net decrease of tape H-rate. In slow motion or freeze, the sync H-rate detector is not tripped because the net change of sync H-rate is only 1%.

6-5 VTR 2H Gate

The 2H gate from the VPR-2B and VPR-3 via gate U49-10 inhibits incoming half-line 2H pulses during the vertical blanking interval and permits pulses that define the H-period to be passed. In heterodyne mode the 2H input is blocked.

6-6 Color Processor PWA Compensation

In slow motion or heterodyne operation, 690-ns one-shot U47-4, controlled by the position of the front panel MODE switch and the 2H gate pulse from the VPR, is switched in or out to compensate for the additional delay of the video signal introduced by the color processor.

6-7 Video Switching and Processing

See Figure 6-3. The function of the video switching and processing circuits is:

- To route tape video input either directly to A/D Converter PWA 3 (normal operation) or to Color Processor PWA 1 (slow-motion mode with the VPR, or heterodyne VTR).
- To gate subcarrier burst out to Tape-H Comparator PWA 4.

- To provide a TTL color-present signal.
- To provide control panel indication of abnormal video amplitude conditions in the Video Input PWA (video overload, video low).
- To provide selection of monitor video display of tape video input or TBC-3 composite video output.
- To provide an internally generated ramp for calibration of the system video processing circuits.

6-8 Input Video Amplifier

The tape video input amplifier, Q1 to Q7, is calibrated to provide a 2-Vp-p output (sync tip to white colorbar tip). The clamp pulse generator circuit, U3-6/U4-6/U7-6/U54-4/Q17-Q19, will clamp the back porch to a reference 0V. The clamp circuit is inhibited by loss of sync signal from the H-rate analog circuits, and vertical (+) from Tape VCO PWA 5. VPRs without the sync head option will have a vertical dropout during the vertical blanking interval and will not provide sync at that time. When the TBC is used with a heterodyne VTR, noise bursts which can upset the TBC circuits are encountered at the beginning of the vertical blanking interval.

6-9 Video Input Switch

In Tape VCO PWA 5, the color present signal is gated with het/normal, search (-), and slow motion to produce the video input switch signal. If the conditions are in color and heterodyne mode, or color and slow motion, then switches U57 and U1 will select the 2-Vp-p video from the Color Processor PWA (see Figure 6-3). In normal mode, as selected by the mode switch on the control panel, or in monochrome condition (burst not present) or in search condition (tape H-rate higher than the operating range of the 6-Fsc oscillator on Tape VCO PWA 5), output of the video input amplifier, Q1 to Q7, will be selected. Selected video will be routed to the remaining circuits of the Video Input PWA.

6-10 Video Output to A/D Converter PWA 3

Selected video is routed through a low-pass filter (0 to 6 MHz) to the output buffer amplifier, Q11 to Q13, which drives the A/D reference insert amplifier switch. The A/D reference is inserted into the horizontal sync to establish an arbitrary -30-IRE unit reference level within the TBC. In the editing process, not all program material necessarily has the same standard of sync tip level, therefore an internal standard is imposed to provide a reference level for the video signal. See Figure 6-6, WF4(B), which shows the insert level on the sync tip at PWA pin 78 (for 75% color-bar input). Nominal level at pin 78 is 1980 mVp-p from sync tip insert to 100% saturated color (equivalent to -30- to +139-IRE units) to match the 2V A/D conversion range with sufficient headroom for best S/N. The A/D reference insert switch is operated by the gated sync (+) from the servoed pulse generator. Black level control from the control panel permits adjustment of the black level value to suit studio conditions.

6-11 Burst and Color Present Circuits

Tape video input, whether directly from input video amplifier Q1-Q7, or via Color Processor PWA 1, is gated by U57 switch and amplified by chroma amplifier

TBC-3

Q25/Q26. Tape sync (-) from the servoed pulse generator circuits then triggers 3.3- μ s one-shot U46-13. During the 3.3- μ s period (when the burst is gated through) the burst passes through burst filter L7/L9 out to Tape H Comparator PWA 4.

Burst is also applied to burst threshold detector U11/U23-5 and is gated through to integrator comparator, U12-7, by gated sync (-) from the servoed pulse generator circuits. The resultant burst-present/not-present signal is ANDed with the greater-than/less-than $\pm 10\%$ tape H-rate signal developed by H-gate control overspeed tape H rate detector U17 to produce the color present signal. Color present is used in the Sync Generator PWA to kill the burst signal output of the Video Output PWA 2. It is also used for other functions related to tape H-rate in Tape H Comparator PWA 4 and Tape VCO PWA 5. Within Video Input PWA 2, the video input switch signal from the Tape VCO PWA 5 signal (derived in part from the color-present signal) determines whether the Color Processor PWA is used or not.

6-12 Test Ramp Generator

An internally generated test ramp on PWA 2, Assembly No. 1463650, is provided for maintenance and calibration of the TBC system video processing circuits. The test ramp can be substituted for the tape video input by connecting jumper J5 to the B-C (test ramp) position. The test ramp is triggered by ramp-delayed H-pulse from the servoed pulse generator.

6-13 Video Low Detector and Video Overload Detector

Video low detector U5/U7/U8 is held high by continuous retriggering of one-shot U8-13 by ramp-delayed tape H from the servoed pulse generator. If the video signal amplitude falls too low, comparator U5 will inhibit U8-13 causing the video low lamp on the control panel to light. If the video amplitude becomes too high, comparator U6-7 will trigger U8-12 causing the video overload light on the control panel to light.

6-14 Monitor Video Circuit

Monitor driver Q23/Q24 delivers tape video input (2 Vp-p) or TBC video from Video Output PWA 2 to the back panel via PWA pin 43/44 for use by the monitor as selected by the monitor switch on the control panel.

6-15 MAINTENANCE

See Figure 6-6 for the waveforms and Figure 6-7 for the component locator diagram, jumper, test-point, and adjustable-component summaries, called out in these procedures.

Before undertaking any adjustments to Video Input PWA 2 review the system alignment sequence in Table 3-2 and the tape/reference test loop discussion of paragraph 3-5 in the system maintenance section for a general understanding of the nature and scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Video Input PWA and interactive functions between it and other PWAs before making any adjustments.

6-16 Video Input PWA 2 Adjustment

- STEP 1 Use basic tape/reference test loop setup with a 75% color-bar test signal at standard level to TAPE VIDEO IN.
- STEP 2 With power off put Video Input PWA on an extender.
- STEP 3 Video level adjustment:
- a. Connect oscilloscope to TP2 (direct processed video); trigger on TP8 (vertical inhibit).
 - b. Adjust R13 (video in gain) for 2.0 Vp-p video.
- STEP 4 Burst phase adjustment:
- a. Connect oscilloscope as follows: CH1, TP5 (gated burst). Trigger TP8 (vertical inhibit)
 - b. Switch burst off at signal generator.
 - c. Adjust R159 (burst amplifier balance) for minimum error (best straight line).
 - d. Return burst to input video.
 - e. Connect vectorscope channel A to PWA pin 67/68. Trigger internally.
 - f. Adjust inductors L7 and L9 (burst filter) for maximum burst amplitude.
 - g. Retune L7 and L9 for best burst phase.

Note

Optimum phasing is indicated by a solid burst vector where out-of-phase loop shown in WF26(N) is closed to a solid line as shown in WF27(N). The slight loop shown in WF27(N) is the normal condition and is a compromise between heterodyne and normal mode burst vectors. If the TBC is to be used only in normal or only in heterodyne mode, the burst vector may be adjusted for a solid line to optimize phasing range in that mode.

- h. With power off, return PWA to its slot.

6-17 Vertical Internal Timing

The TBC-3 detects the first two equalizing pulses to provide vertical timing consistent with normal internal TBC vertical timing. Adjust timing as follows:

- STEP 1 Set up normal VPR configuration to play back standard 75% color bars.
- STEP 2 With power off extend Video Input PWA 2.
- STEP 3 Connect oscilloscope as follows: CH1, TP11 (noise gate sync); CH2, PWA Pin 58 (tape vertical). Trigger TP11 (noise gate sync).

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- STEP 4 Play tape and adjust R245 (equalizer pulse vertical delay) so that leading edge of positive pulse at pin 58 is delayed 20 μ s from start (negative edge) of the off-tape first vertical broad pulse at TP11.
- STEP 5 Connect oscilloscope as follows: CH1, TP11 (noise gate sync); CH2, U21 pin 2. Trigger on PWA pin 58 (tape vertical).
- STEP 6 Place VPR in E-E mode.
- STEP 7 Set TBC-3 MODE switch to HET.
- STEP 8 Adjust R338 (one shot U19-13 timing) so that signal at U21 pin 2 goes positive five horizontal lines before equalization pulses at TP11.

6-18 Servoed Pulse Generator Alignment

- STEP 1 Connect oscilloscope probe to U35 pin 5 and adjust R249 (servo pulse generator centering trim) for 8.0 μ s.
- STEP 2 Connect oscilloscope probe to TP10 (H-rate analog dc) and adjust R243 (servo pulse generator centering) for 8.0 Vdc.

6-19 Dropout Stretch Adjustment

- STEP 1 Connect oscilloscope as follows: CH1, TP9 (stretched dropout). Trigger Pin 33.
- STEP 2 Play back a tape known to have dropouts.
- STEP 3 Adjust R212 (DO stretch) for 10- μ s stretched dropout duration.

6-20 Monochrome Phase Correction Adjustment

- STEP 1 Connect oscilloscope to U55-7.
- STEP 2 Place VPR in E-E mode.
- STEP 3 Adjust R322 (monochrome phase correction) for 2.0 Vdc.
- STEP 4 Play back a monochrome tape in slow motion and note if monitor picture shifts when slow motion speed is changed.
- STEP 5 If necessary repeat steps 1-3 and trim R322 as required for no shift when speed is changed.

6-21 Color Processor PWA 1 Delay Compensation

- STEP 1 Connect scope probe to U47-4 and trigger scope on internal.
- STEP 2 Adjust R290 (color processor compensation) for pulse width of 690 ns.

6-22 Video Filter Response**Note**

The following procedure is for reference only and should not be attempted without proper test equipment.

- STEP 1** Remove shielded cable at E1/E2.
- STEP 2** Connect sweep generator to E1/E2.
- STEP 3** Connect spectrum analyzer to TP2 (direct processed video).
- STEP 4** Ground TP19 (initial sync slice).
- STEP 5** Install J1 to A-B and remove J2.
- STEP 6** Adjust inductor L1 for a minimum response at 7.159 MHz.
- STEP 7** Adjust L2 for a minimum response at 9.852 MHz. There is interaction between L1 and L2, so perform steps 6 and 7 several times to obtain minimum 7.159 MHz and 9.852 MHz.
- STEP 8** Install J2 to A-B.
- STEP 9** Adjust L3 for minimum response at 4.803 MHz.
- STEP 10** Remove jumper J1 and jumper J2.
- STEP 11** Adjust T1 for minimum response at 4.803 MHz.
- STEP 12** Install J2 to A-B.
- STEP 13** Verify that response from 0 MHz to 4.0 MHz is +0.1 dB (referenced to response at 1.0 MHz).
- STEP 14** Adjust L1 slightly for response at 7.159 MHz to be -45 dB from response at the 1.0-MHz reference.
- STEP 15** Verify that response from 7.2 MHz to 11 MHz is -25 dB from response at 1.0-MHz reference.
- STEP 16** Remove ground from TP19.
- STEP 17** Reconnect shielded cable to E1/E2.
- STEP 18** Connect shield to E2.

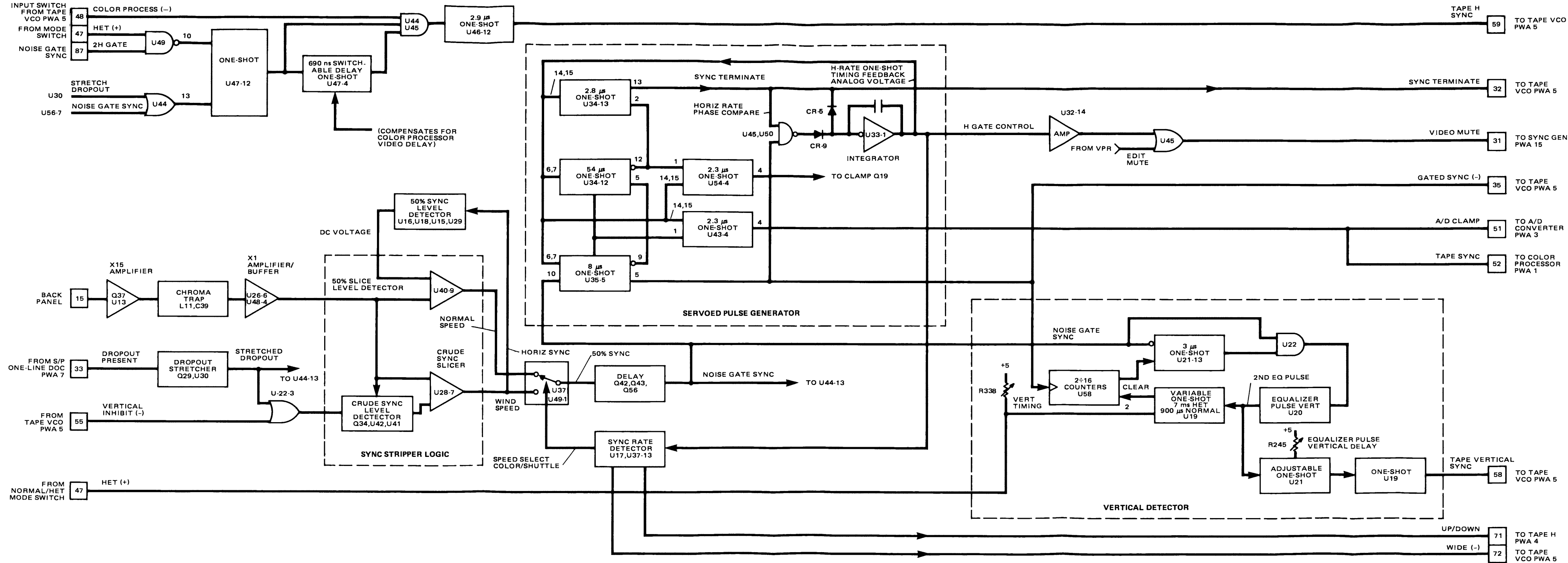


Figure 6-1.
Sync Processing Simplified Block Diagram,
Video Input PWA 2

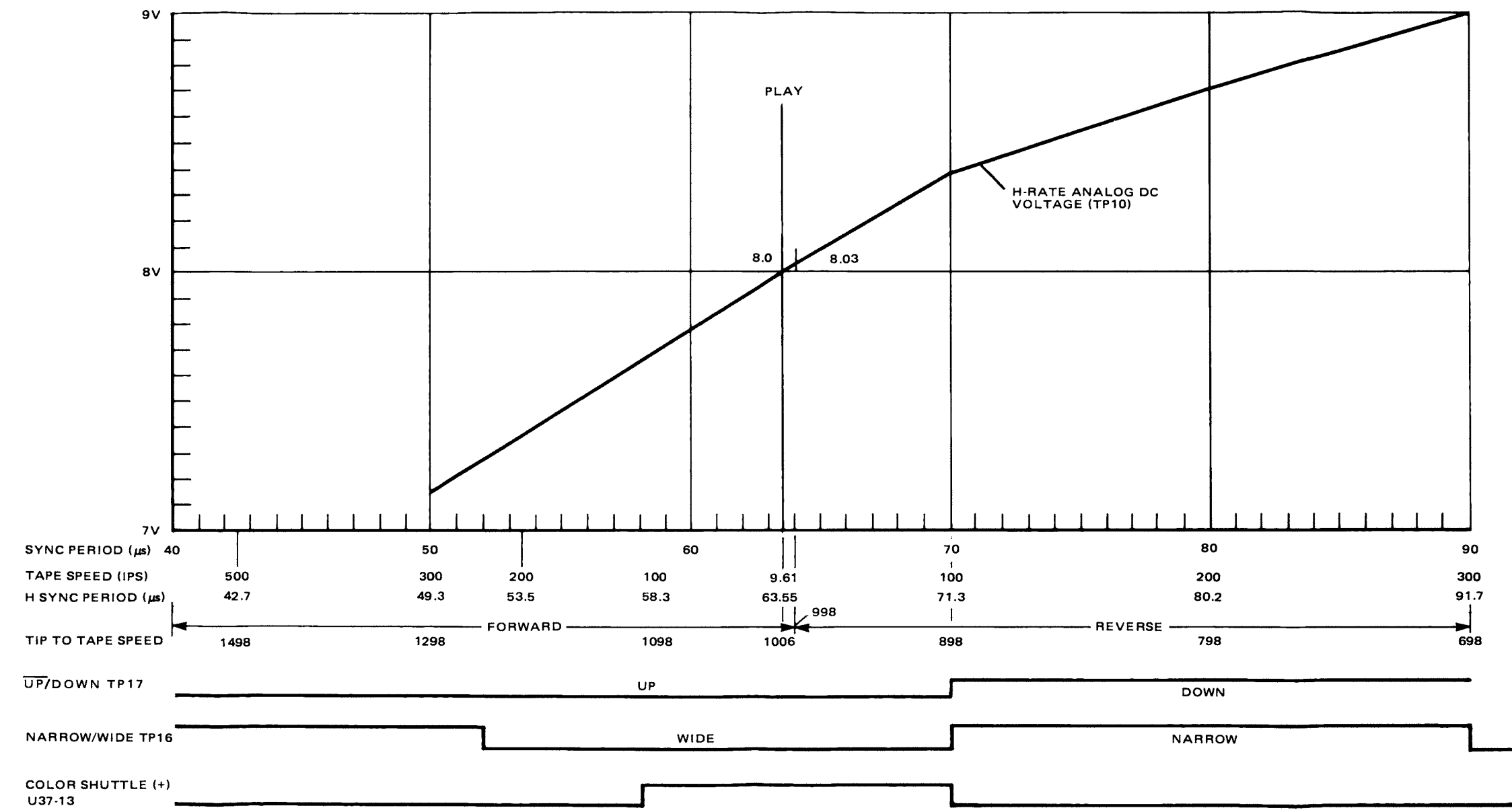


Figure 6-2.
Servoed Pulse Generator and Sync
Rate Detector Waveforms

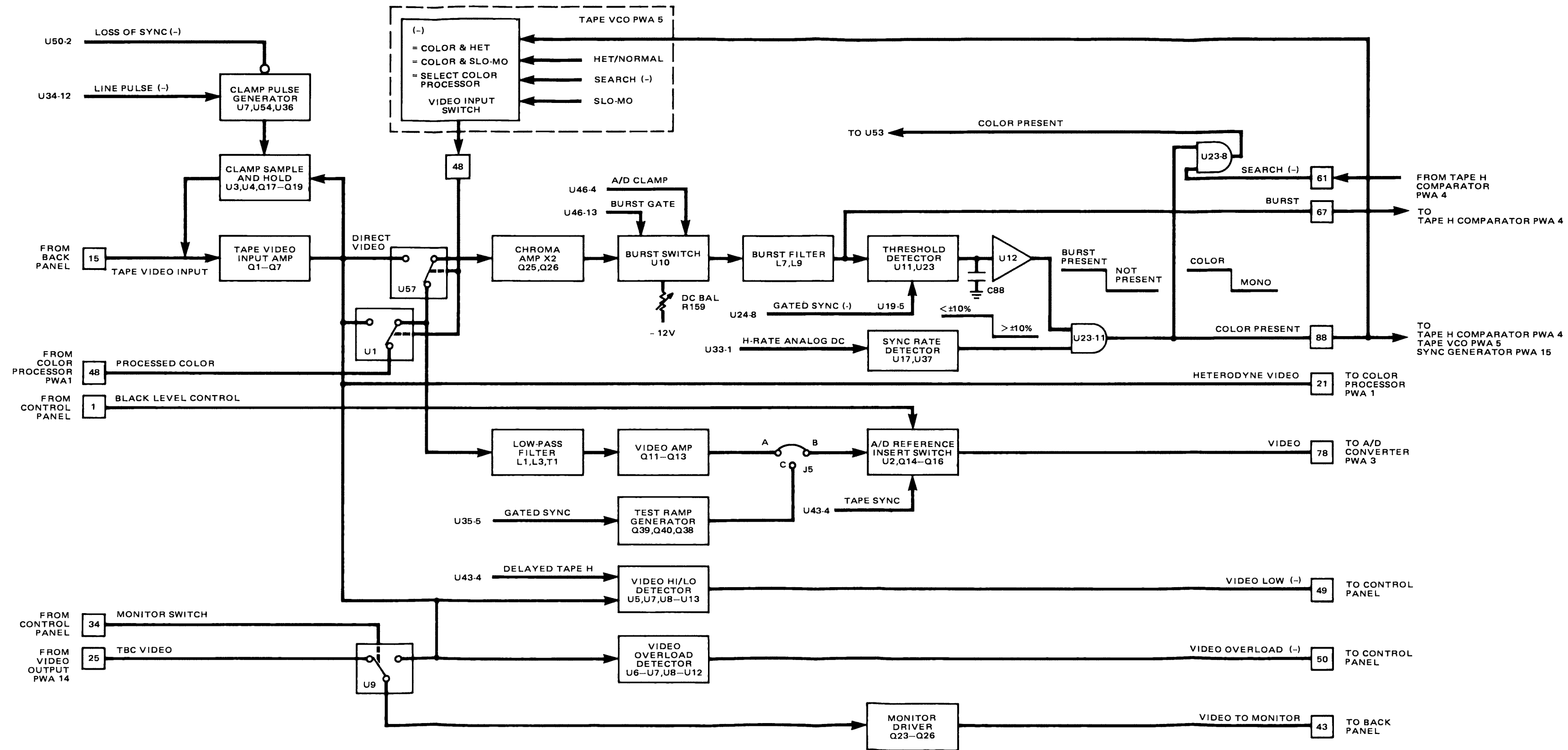


Figure 6-3.
Video Switching and Processing, Video Input
PWA 2, Simplified Block Diagram



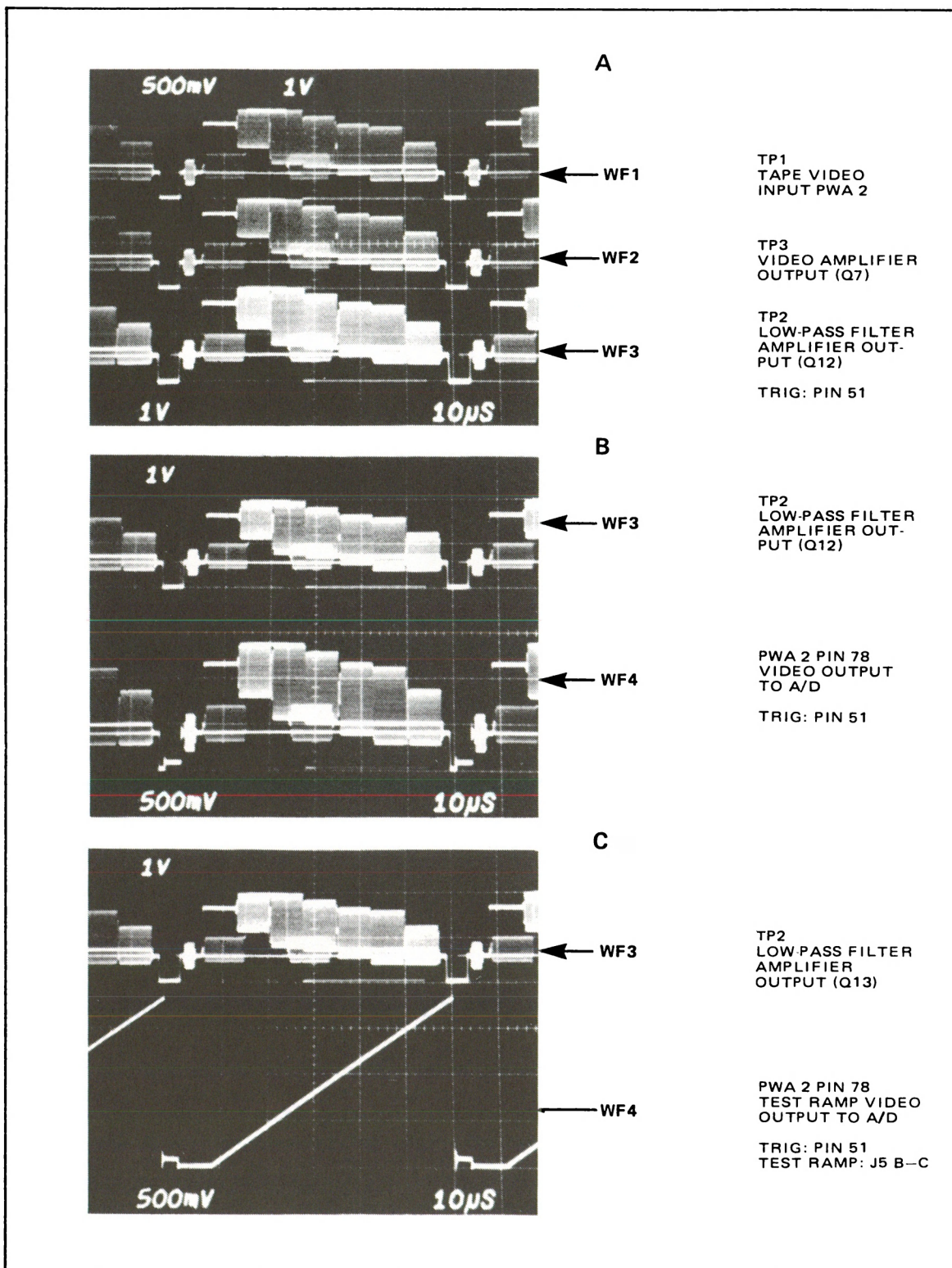


Figure 6-6. Video Input PWA 2 Waveforms (Sheet 1 of 5)

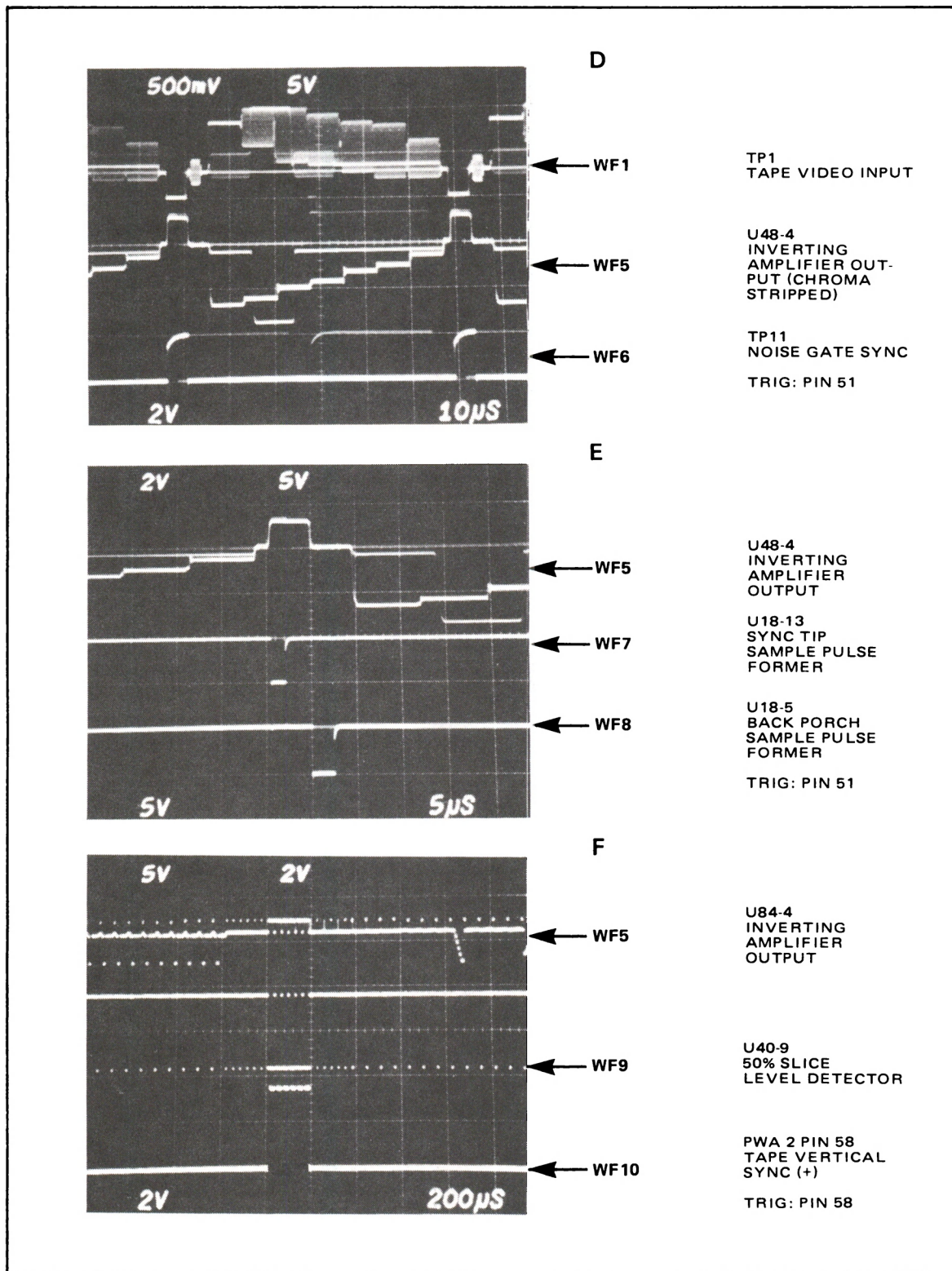


Figure 6-6. Video Input PWA 2 Waveforms (Sheet 2 of 5)

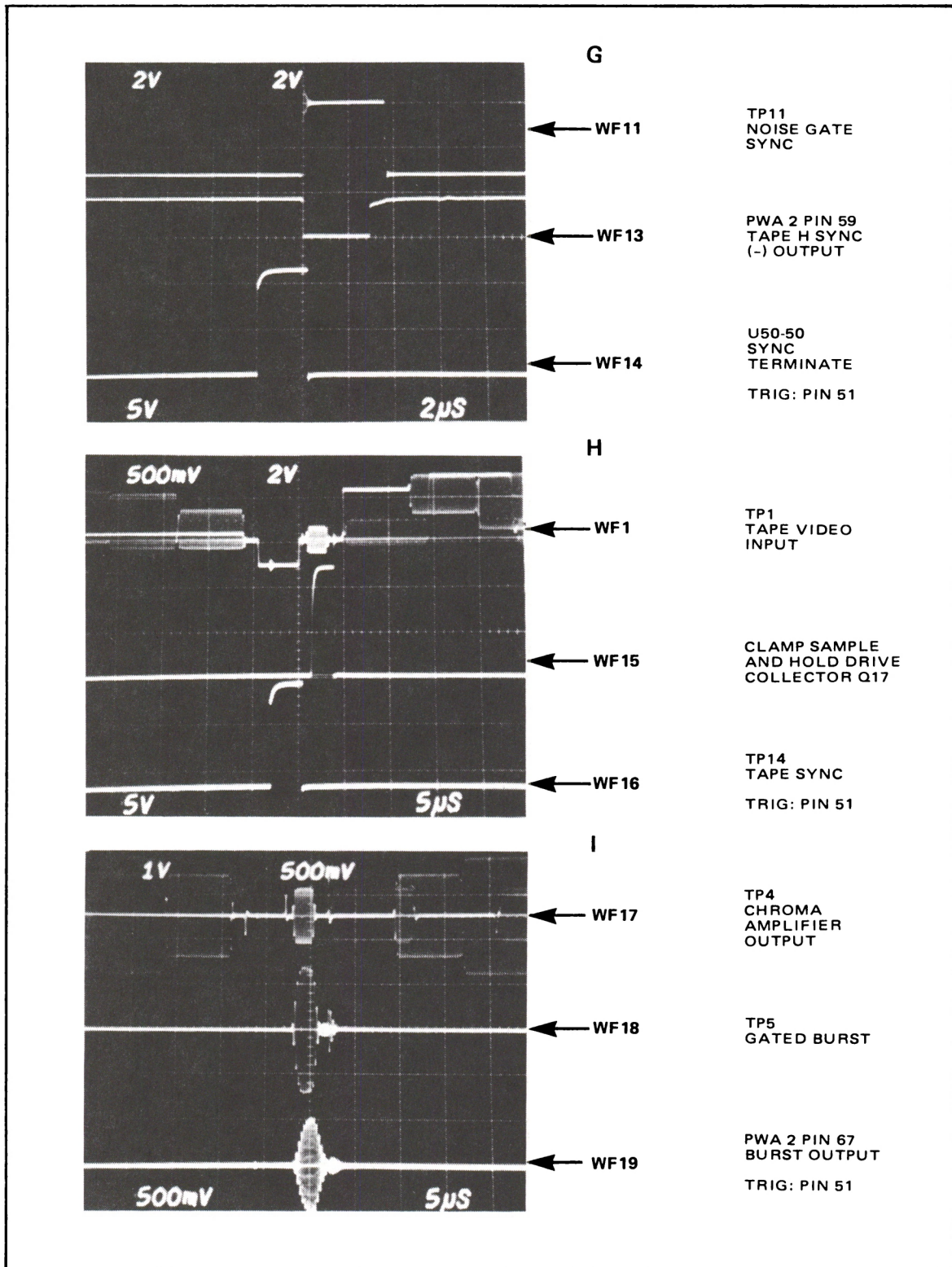


Figure 6-6. Video Input PWA 2 Waveforms (Sheet 3 of 5)

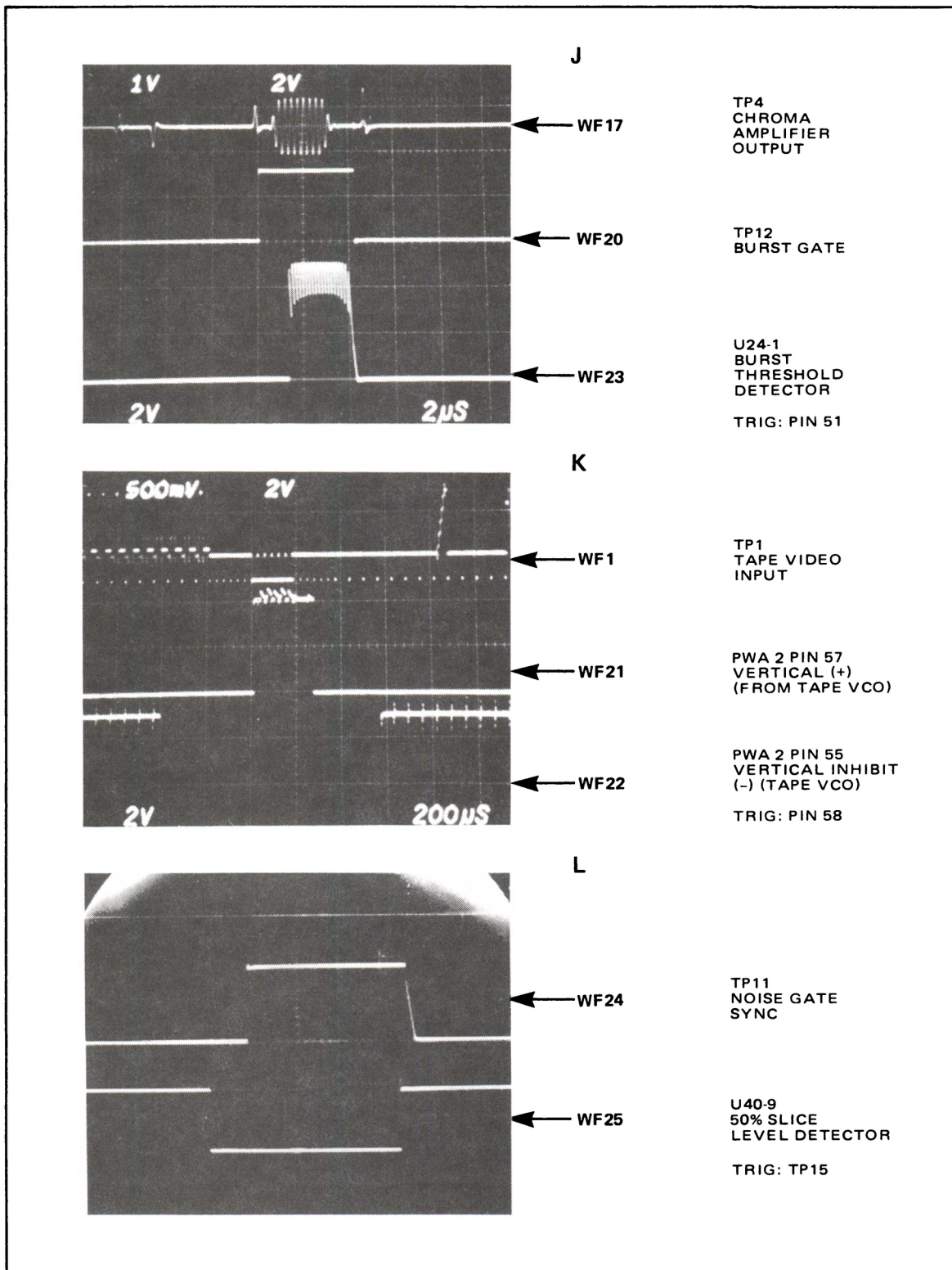


Figure 6-6. Video Input PWA 2 Waveforms (Sheet 4 of 5)

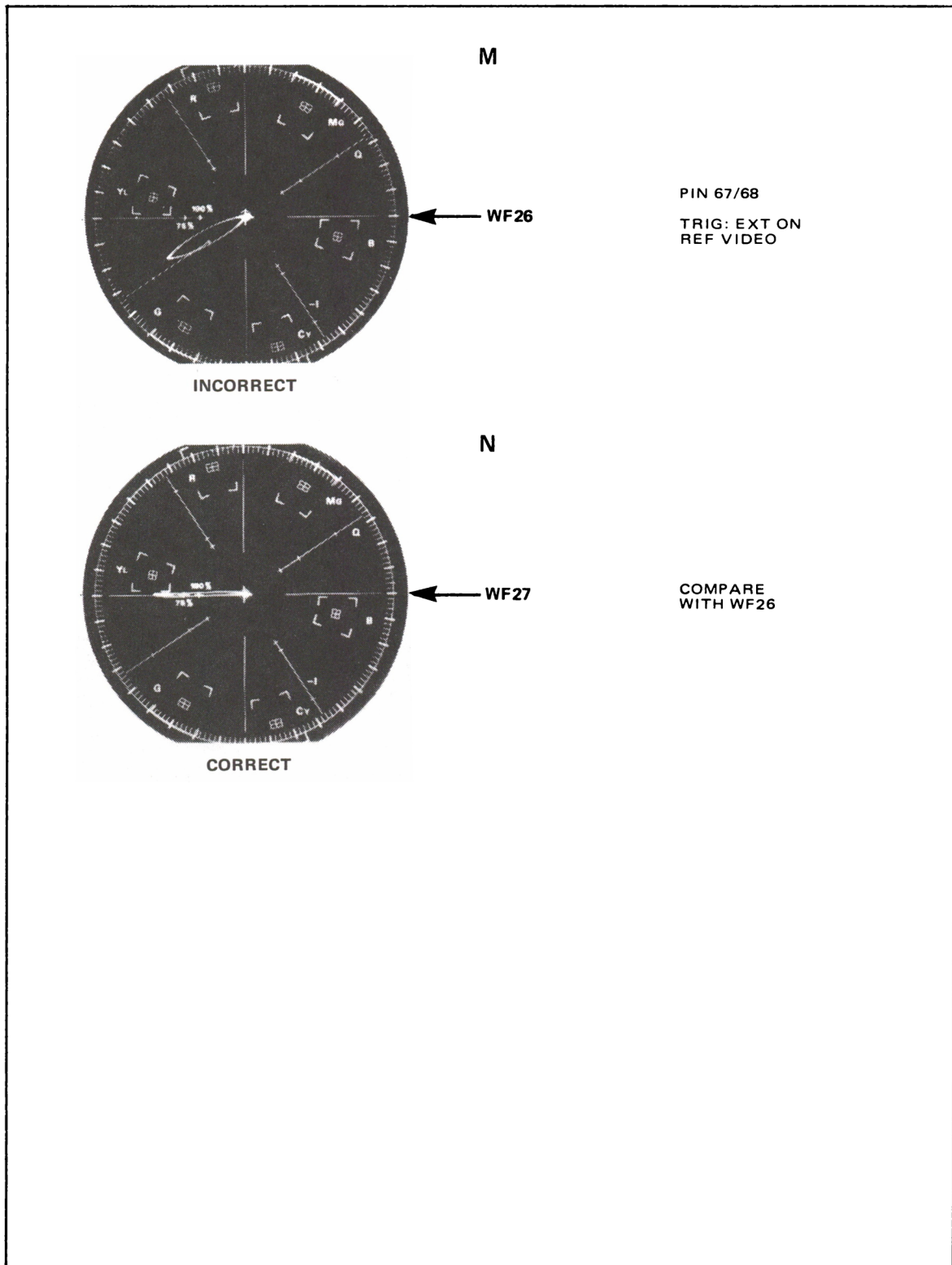


Figure 6-6. Video Input PWA 2 Waveforms (Sheet 5 of 5)

PWA 2 Jumpers

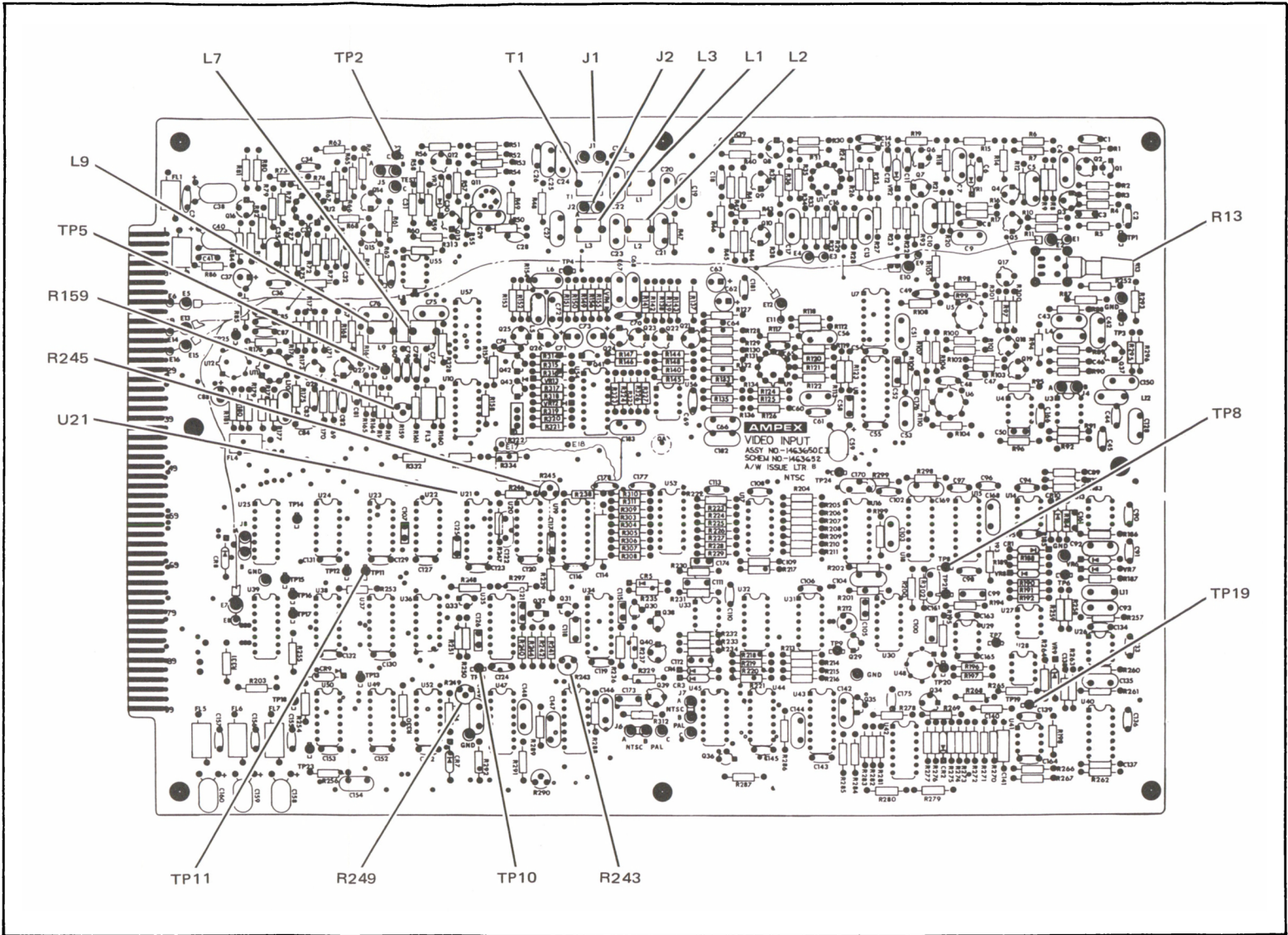
Jumper	Position	Function
PWA 2		
J1	Removed A-B	Filter Adjustmnet Normal Align filter L3/C27
J2	A-B Removed	Filter Adjustment Normal Test
J4	A-B Removed	Clamp Normal Defeats clamp
J5	A-B B-C	Ramp Generator Normal Test ramp
J6	A-B B-C	Standards Select NTSC PAL
J7	A-B B-C	Standards Select NTSC PAL
J8	A-B Removed	Burst Normal Force monochrome

PWA 2 Adjustable Components

Component	Function
L1	Low pass filter alignment
L2	Low pass filter alignment
L3	Low pass filter alignment
L7	Burst filter
L9	Burst filter
R13	Video in gain
R159	Burst amplifier balance
R212	Dropout stretch
R243	Servo pulse generator centering
R245	Equalizer pulse vertical delay
R249	Servo pulse generator centering trim
R290	Color processor compensation
R322	Monochrome phase correction
R338	Oneshot V19-13 timing
T1	Low pass filter alignment

PWA 2 Test Points

Test Point	Function
TP1	Tape video in
TP2	Direct/processed video
TP3	x2 Video
TP4	Chroma
TP5	Gated burst
TP6	Initial sync slice level
TP7	50% sync slice level
TP8	Vertical inhibit
TP9	Stretched dropout
TP10	H-rate analog dc
TP11	Noise gate sync
TP12	Burst gate
TP13	A/D clamp
TP14	Tape sync
TP15	Tape H sync (-)
TP16	Wide (-)
TP17	Up/down
TP18	Video mute
TP19	Initial sync slice
TP20	Back porch sample
TP21	Sync tip sample
TP22	Not used
TP23	Gated sync
TP24	Dropout
TP25	Color kill



PWA 2 Component Locator

Figure 6-7.
Jumpers, Adjustable Components, and
Component Locator, Video Input PWA 2

PART II

SECTION 7

A/D CONVERTER PWA 3

DESCRIPTION AND MAINTENANCE

7-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463553

Schematic No. 1409149

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 7-2, simplified block diagram
- Figure 7-3, waveform illustrations and maintenance data

7-2 DESCRIPTION

The video signal from the Video Input PWA 2 is converted to digital form in the A/D Converter PWA.

Amplitude of the video signal is sampled at three times the subcarrier rate (3 Fsc or 93 ns) and converted to an eight-bit binary number for each sampling period. Thus, one cycle of subcarrier is defined by three samples. The analog video signal is represented in digital form at the output of the A/D Converter PWA as a serial train of binary eight-bit words. Each word can range from 0000 0000 to 1111 1111 (-30 units to 139-IRE units) and represents any of 256 values. Waveforms 5 through 12 of Figure 7-3 show the conversion with the test ramp.

Note the A/D reference insert on the sync tip in waveform 1(A). The A/D reference insert is added in the Video Input PWA to establish a fixed, consistent sync tip insert level within the TBC. Video from the Video Input PWA for 100% saturated color bars is nominally 2V and is buffered by a clamp feedback amplifier in the A/D converter which clamps the sync tip reference to -2V. This establishes the quantization reference level of the video to the A/D converter LSI integrated circuit, U6.

The quantization range is shown in Figure 7-1 which gives the relationship between the 256 quantizing levels, peak-to-peak voltage to the A/D converter, IC, and equivalent IRE unit measure. The 0-256 bit range corresponds to a -30 to +139.3-IRE level. The clamp amplifier sets the 100% saturated yellow/cyan bar

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peak at -0.021V. This leaves a 2-1/2 quantizing level guard band for best signal-to-noise at peak 100% video level.

A/D conversion is performed by a single integrated circuit which uses a 1-bit pipeline delay technique. A sample is taken (comparators are latched) approximately 10 ns after the rising edge of the convert signal. This delay may vary by a few nanoseconds, but the short-term uncertainty (jitter) in strobe delay is less than 30 ps. The 255 to 8 encoding is performed on the falling edge of the convert signal, and the result is transferred to the output latches on the next rising edge. The outputs require a minimum time to begin changing to the new result. This permits the preceding result to be read on the same rising edge that read data N while acquiring sample N+2. All timing specifications are with respect to TTL threshold crossing (1.5V). Quantizing levels within the A/D converter are 7.8431 mV per step from 0V to 2V.

The A/D converter integrated circuit, U6, is a large-scale integrated (LSI) device in a 64-pin dual in-line package. It is an 8-bit fully parallel (flash) A/D converter capable of digitizing an analog signal at 3Fsc. A single convert signal (clock) controls the unit operation, which consists of 255 sampling comparators, combining logic and full-scale step input register. Recovery from a full-scale step input occurs within 20 ns. The digital output is in binary code.

Sampling time is controlled by a 10.7-MHz clock which is phase-locked to the leading edge of the incoming tape H-sync pulse. The phase-locked clock has its origin in a 10.7-MHz 3x subcarrier oscillator on the Tape H Comparator PWA 5.

The 8-bit binary value in the A/D converter device is clocked into an 8-bit output register on A/D Converter PWA 3 by the rising edge of the common 3Fsc clock. Thus, total pipeline delay of the A/D Converter PWA is two bits. The signal from the PWA output register is routed to Serial-to-Parallel Converter PWA 8.

7-3 MAINTENANCE

See Figure 7-3 for waveforms, component locator diagram, test points and adjustable component summaries.

Review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-5 for a general understanding of the context for maintenance on the A/D converter.

Consult reference waveforms and interconnect data on the simplified schematic to confirm normal operations of A/D Converter PWA 3 and interactive functions between it and other PWAs.

There are two controls on the A/D Converter PWA, but neither R10 (video damping) nor R22 (converter gain) require adjustment except that necessitated by component failure. Converter gain control R22 sets up quantizing increments. A 2.000-Vdc value at TP2 is correct for the unity gain levels on the Video Input PWA. Video damping control R10 affects high-end frequency response.

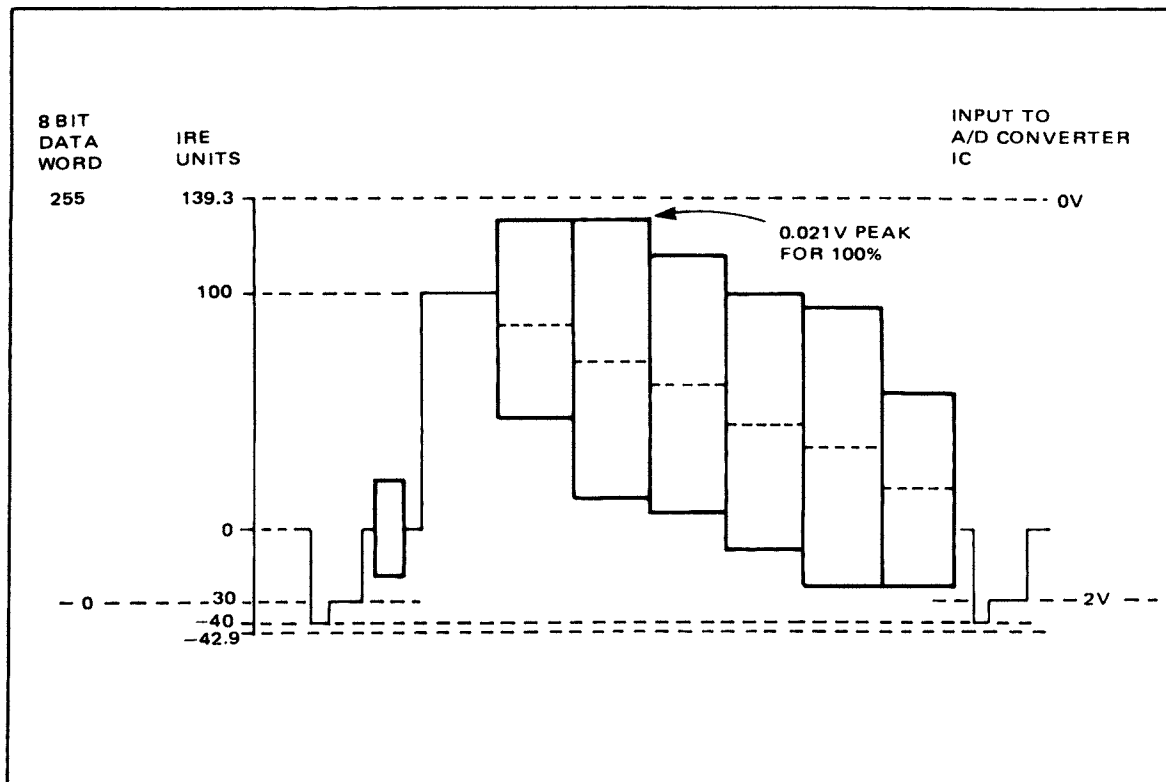


Figure 7-1. A/D Converter PWA 3 Level Definitions

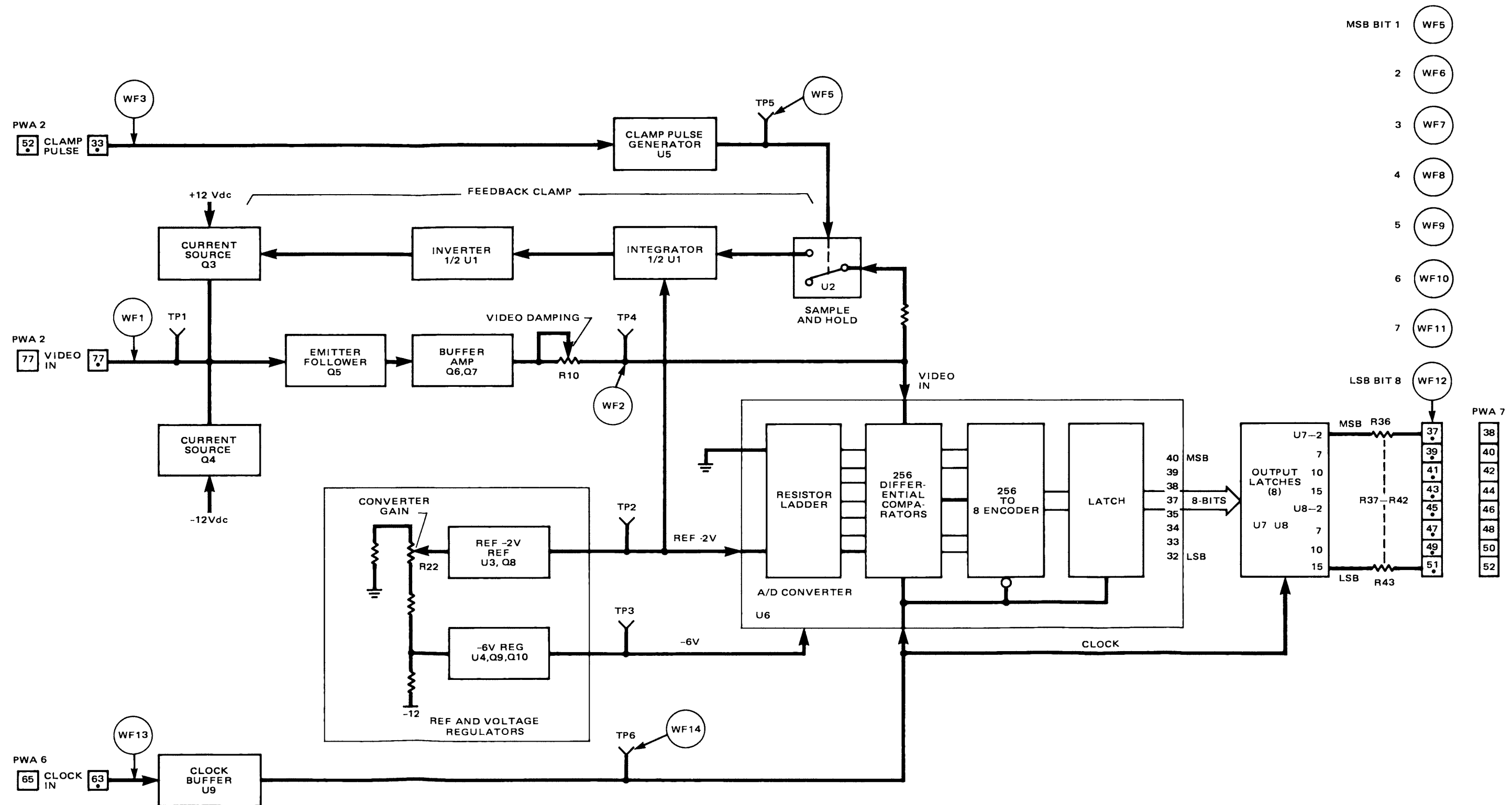


Figure 7-2.
A/D Converter PWA 3 Block Diagram

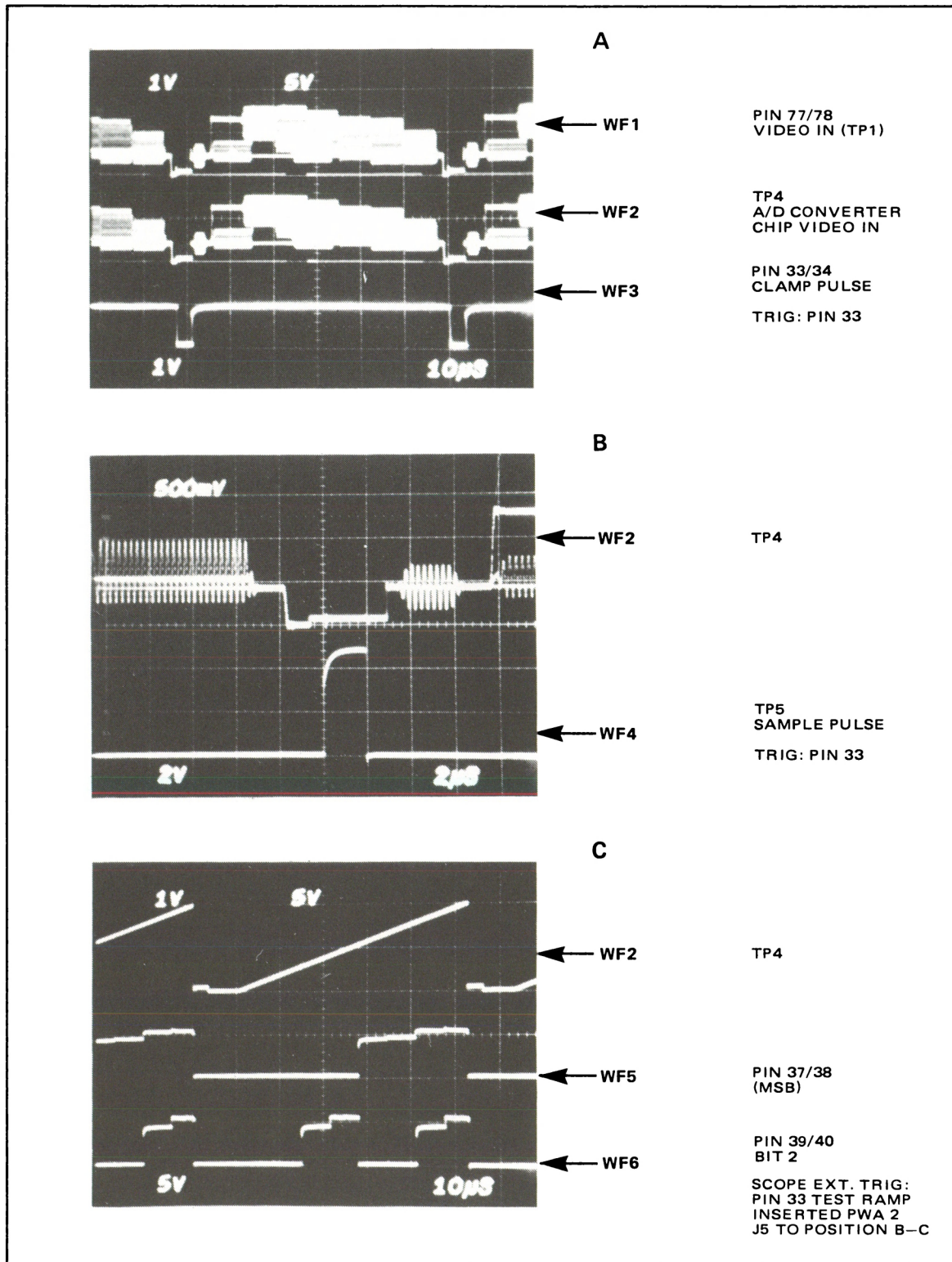


Figure 7-3. Waveforms (Sheet 1 of 4)

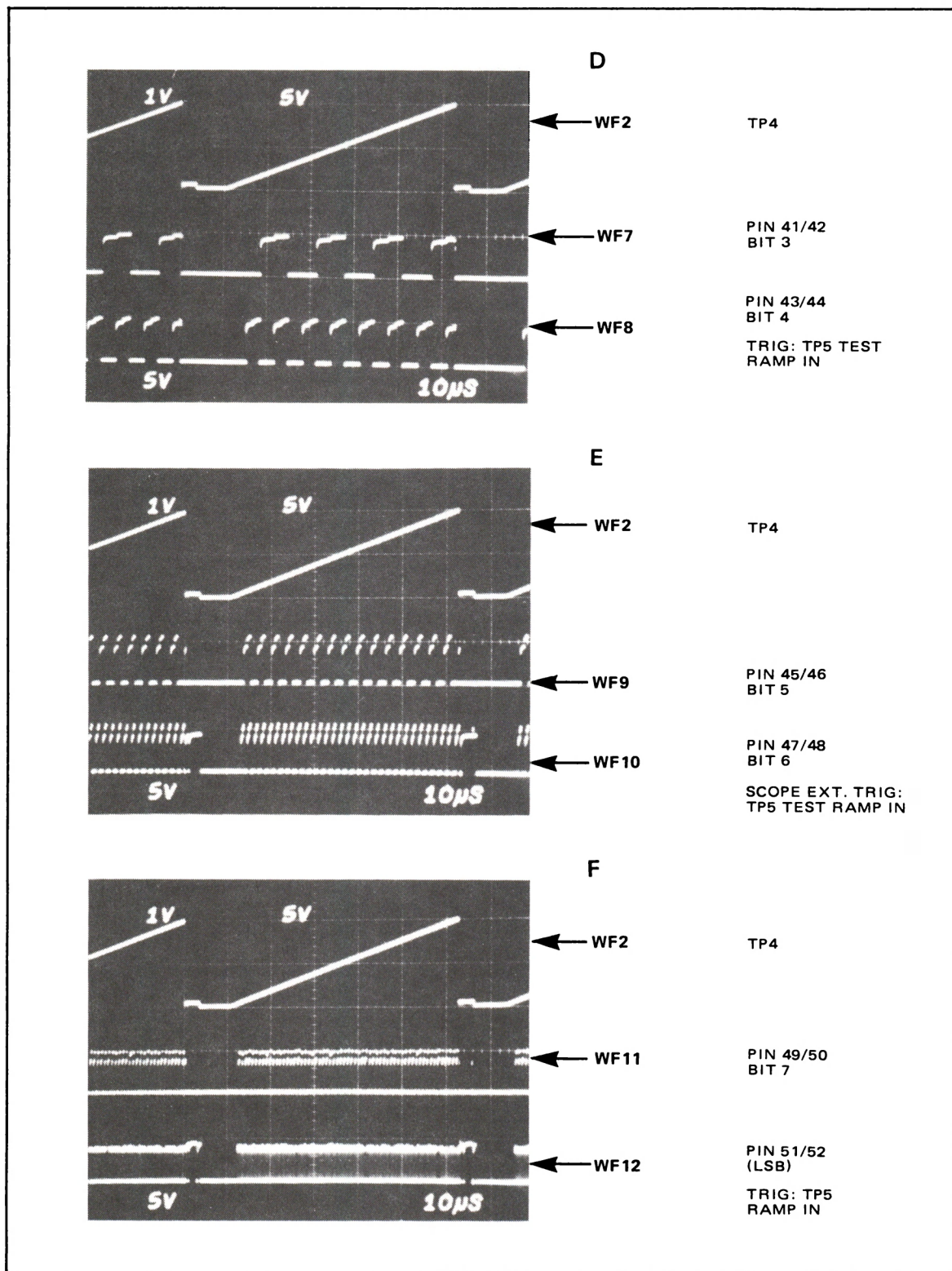


Figure 7-3. Waveforms (Sheet 2 of 4)

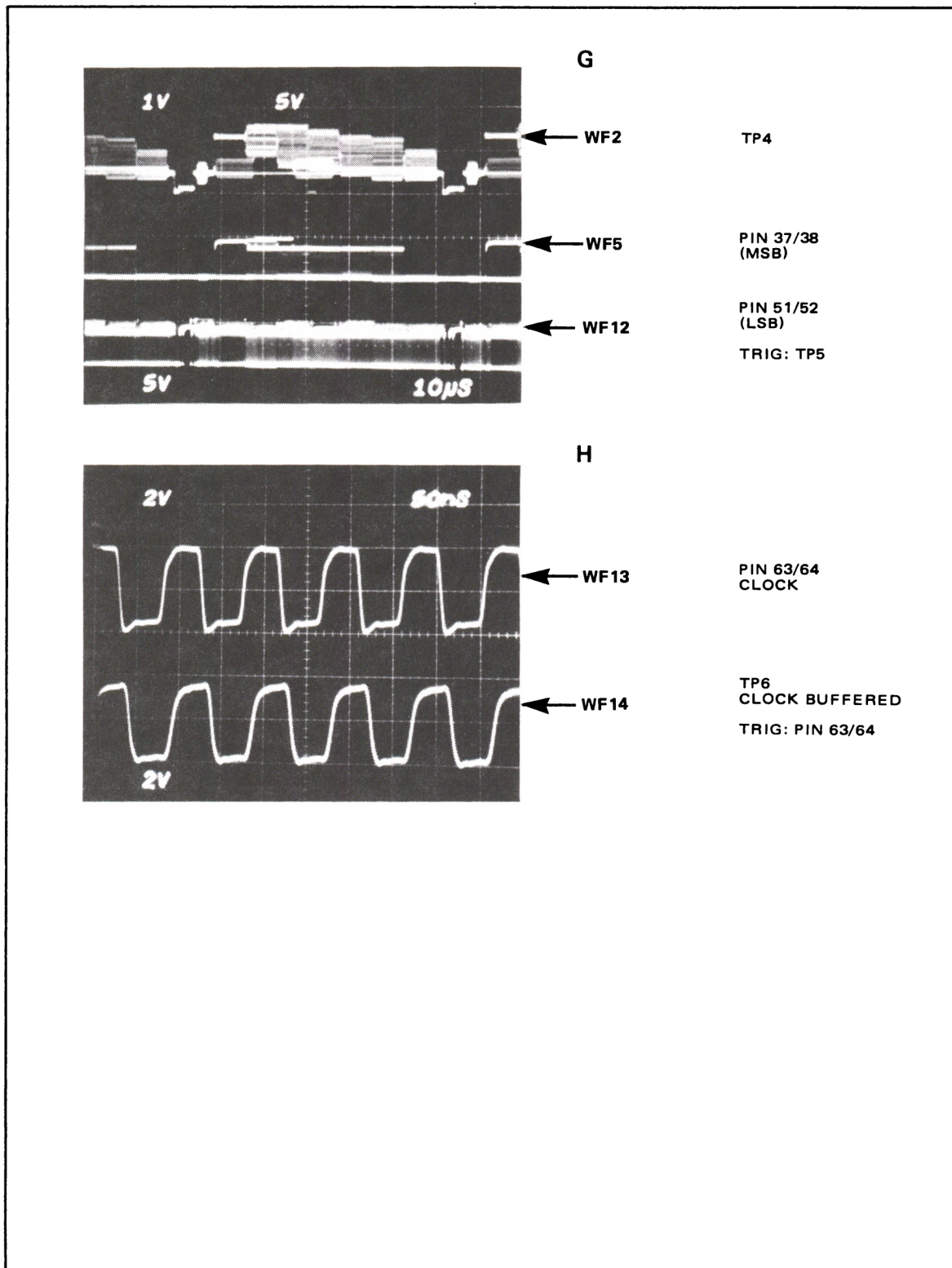
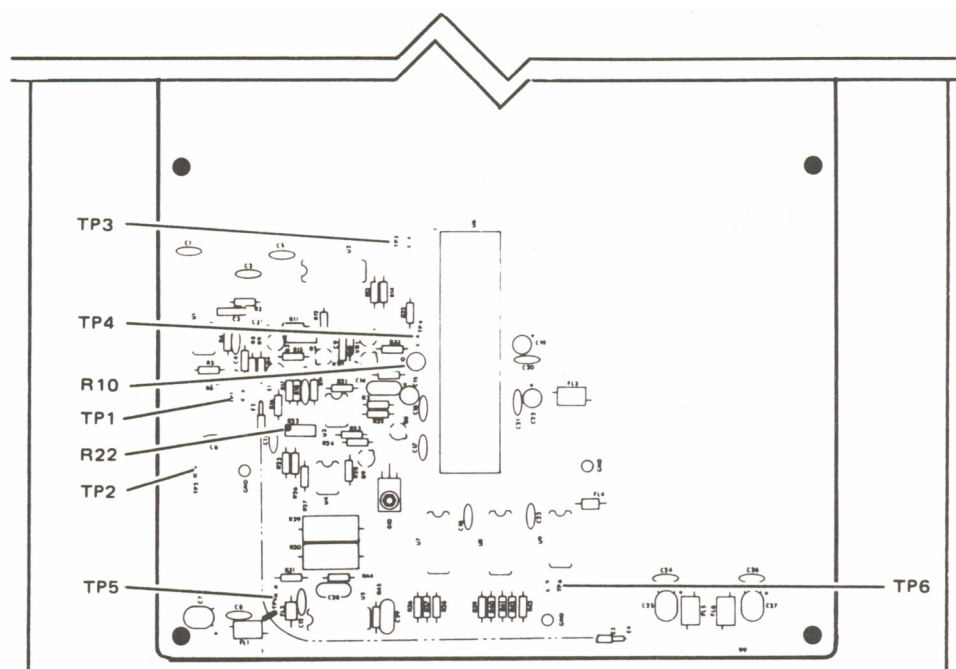


Figure 7-3. Waveforms (Sheet 3 of 4)



PWA 3 Component Locator

PWA 3 Test Points

Test Point	Function
TP1	Video in
TP2	-2.00 Vdc
TP3	-6.00 Vdc
TP4	Converter video
TP5	Sample pulse
TP6	Clock

PWA 3 Adjustable Components

Component	Function
R10	Video damping
R22	Converter gain

Figure 7-3. Test Points, Adjustable Components, Component Locator, A/D Converter PWA 3 (Sheet 4 of 4)

PART II

SECTION 8

TAPE H COMPARATOR PWA 4

DESCRIPTION AND MAINTENANCE

8-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463568

Schematic No. 1463570

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section.

- Figure 8-4, overall block diagram
- Figure 8-5, PWA 5 and PWA 6 signal relationships
- Figure 8-6, simplified schematic
- Figure 8-7, waveforms
- Figure 8-8, maintenance data

Tape H Comparator PWA 4 function summary:

- Works in conjunction with Tape VCO PWA 5 to synchronize the TBC memory write control signals to the off-tape H-sync pulses.
- Compares phase of off-tape H-sync pulses with phase of sync pulses produced by VCO on Tape VCO PWA 5.
- Produces a line-by-line velocity error voltage and provides it to the velocity compensator on Parallel/Serial Converter w/Vel Comp PWA 13.
- Provides sync-coherent subcarrier to Color Processor PWA 1.

8-2 DESCRIPTION

Tape H Comparator PWA 4 accepts synchronizing signals from Tape VCO PWA 5 and Video Input PWA 2 and processes them to produce (for the TBC system) sync signals that are phase-locked to a selected color burst crossing (Fsc). An exception to this process is heterodyne mode. In that mode, tape H sync from Video Input PWA 2 is selected by the TBC-3 MODE switch which operates the tape VCO sync select in Tape VCO PWA 5. See Figure 8-5.

The Tape H Comparator and Tape VCO PWAs are functionally one large interdependent circuit. In normal mode, with color present, signal processing begins on the tape H comparator with phase comparison of the timing relationship

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between the leading edge of a delayed tape H sync and a selected burst crossing from the Video Input PWA. When making color-frame edits, a horizontal picture shift can occur if playback tape start-of-burst relative to the leading edge of sync is not set according to the RS170A standard. An incorrect relationship is displayed on the VPR-3 Sch Φ meter. Also, the TBC-3 control panel EDIT READY indicator is off if the error is more than $\pm 40^\circ$.

To compensate for the problem, adjust the VPR-3 Sch Φ control to center the meter and cause the EDIT READY indicator on the TBC-3 to illuminate. Adjustment of the Sch Φ control routes a dc signal to the TBC-3 Tape H Comparator PWA 4 input pin 34. This dc level is amplified by U61-1 and applied to delay one-shot U20-12 to adjust the one-shot pulse duration. Thus the phase of the burst used by the sync/burst crossing phase comparator U48/U56 can be adjusted by remote control from the VPR-3.

Horizontal sync of tape VCO PWA 5 is derived from the selected burst crossing out of Tape H Comparator PWA 4. The 6Fsc oscillator is phase-locked to this H-sync and thus to the selected burst crossing.

With the exception of 6Fsc, signals from Tape VCO PWA 5 are derived from the 6Fsc divide-by-1365 counter decode. Thus, signals from tape VCO are phase-locked to selected burst crossing. However, these signals contain VCO errors which will be removed by Tape H Comparator PWA 4.

The normal 6Fsc oscillator has a long time constant of approximately 16 lines. Circuits on the Tape H Comparator PWA, centered around the control logic and the error voltage generator, provide a faster time constant phase correction of synchronizing signals from the tape H comparator to the TBC-3 system. Signals from Tape H Comparator PWA 4 to Tape VCO PWA 5 are comparator timing and 7.8 kHz. Signals from the Tape VCO PWA to the Tape H Comparator PWA are 6Fsc, half-line, qualified H-pulse, frequency error, and VCO write pulse. Tape VCO 6Fsc generates VCO 3Fsc via a divide-by-two counter. VCO 3Fsc is applied to a divide-by-three counter to produce VCO Fsc. VCO 6Fsc and VCO 3Fsc drive a two-stage phase shifter which is modulated by the error voltage generator. This provides line-by-line correction of the tape VCO 3Fsc output and write pulse output timing. These signals, with 7.8 kHz, are used by Memory Control PWA 6 to control the memory-write function at tape rate.

VCO Fsc is sampled and summed against voltage from the error voltage generator. The resultant line error output signal is used by the velocity compensator on Parallel/Serial Converter PWA 13 in the memory-read function to correct for timing errors introduced into the video signal during the horizontal line due to velocity errors.

In slow-motion operation, the frequency error signal from the Tape VCO PWA modulates the burst phase detector, and thereby the tape H comparator output signals, to correct for the phase shift of 3.58 MHz in the burst filter of the Video Input PWA. (In slow motion, burst is 3.58 MHz—1%.)

8-3 Burst Crossing to Tape H-Sync Phase Relationship

See waveforms G, H, I, Figure 8-7. To preserve the integrity of the H-sync-to-chroma-phase relationship, the video signal is tested on a line-by-line basis to determine if a burst is present. If the result is positive, the burst crossing selector is enabled. If burst is not present, the associated sync/burst phase circuitry is inoperative for that line. When enabled, the burst crossing selector is clocked to a reset condition by the selected burst crossing. Therefore, the trailing edge of the output pulse represents the selected burst crossing to the sync/burst phase circuitry. Because the chroma subcarrier is an odd multiple of one-half the horizontal rate, the phase of chroma relative to H-sync shifts 180° on the alternate lines. Therefore, the timing of the delayed tape H-sync on the Tape H Comparator PWA is shifted by 140 ns on alternate lines by the 7.8-kHz signal (one-half line divided by two).

$$F_{sc} = \frac{455}{2} \times 15.73426 \text{ kHz} = 3.579545 \text{ MHz}$$

$$1/2 \text{ cycle of } F_{sc} = 140 \text{ ns}$$

$$\text{one cycle of } F_{sc} = 279 \text{ ns} = 277.5 \text{ cycles of } F_{sc}/\text{line}$$

See Figure 8-1. The delayed tape H-sync (shifted 180°, alternate lines) is further delayed so that the leading edge occurs at a zero crossing during a negative-going transition of the selected color burst cycle. This pulse is used to enable the burst crossing voltage comparator. The next following positive zero crossing of burst clocks the selector reset and cancels the enable. The selected burst crossing from the burst crossing comparator is used in three ways:

- To reference the comparator timing output of the Tape H Comparator PWA to the burst crossing.
- As an input to the sync/burst crossing comparator to maintain a constant sync/burst crossing time relationship.
- As an input to the slow-motion burst phase correction circuit.

The Q output of the 7.8-kHz flip/flop is ANDed with selected burst crossing in one gate. The Q output is ANDed with selected burst crossing in another gate. When Q is high, the signal is delayed by 140 ns and applied to a one-shot which generates the comparator timing pulse. When Q is high (next line) the signal is applied directly to the comparator timing one-shot. Thus, the 140-ns phase shift on alternate lines for the burst crossing selector is removed and the comparator timing (H-sync) to the Tape VCO PWA occurs at a positive transition of F_{sc} on one line and at a negative transition on the next line.

See waveforms M, E, and F, Figure 8-7. The sync/burst crossing phase-comparator circuits, with the associated ±225° limit detector, modulate the burst phase vernier to maintain the sync/burst timing relationship. Delayed tape-H from the alternate line burst-phase-select one-shot dumps the charge on C36, setting the input of the buffer amplifier on a reference level of -5.2V. The burst crossing selector enable starts a ramp charge on C36. The selected burst crossing stops the ramp. The voltage value achieved is proportionate to the time relationship between

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the two signals. The burst crossing selector pulse operates the sample-and-hold circuit. The output of the sample-and-hold buffer is used two ways: it modulates the pulse width of the burst phase vernier one-shot, and it is applied to two limit detectors. The $\pm 225^\circ$ limit detector operates a reset to center range switch which dumps the charge on sample-and-hold capacitor C104 if the error signal is outside the reference limits. This condition can occur if color burst on the edited material is too far out of phase. Then the dump to a 90° offset is made and a new burst crossing is selected. When the burst phase is within $\pm 40^\circ$ of edit ready, control panel light is on.

See Figure 8-7, waveform M. The selected burst crossing is also applied as an input to the burst phase correction circuits. The frequency error signal is a measure of the long-term H-rate error from the tape. This is applied to one input of a voltage comparator. The other input is a ramp initiated by burst crossing. A programmable counter U11, started by burst crossing, resets the enable of the comparator at the end of its count.

The resultant pulse out of the comparator is a phase correction for burst crossing when tape speed is other than normal. The corrected burst crossing starts the action in the control logic. An entry flip/flop is set with burst crossing and reset two 6Fsc pulses later. After the first of these 6Fsc pulses, the load data is removed from the programmable counter. After the second 6Fsc pulse, a two-stage shift register resets the entry flip/flop and holds the load data high until the carry from the programmable counter, clocked by 6Fsc, resets the shift register. The carry also latches data from the divide-by-two and divide-by-three (3Fsc, Fsc) counters. After a few nanoseconds of gate phase delay, the carry resets the 3Fsc and Fsc counters to zero and the count starts over. The number stored in the latch is a measure of the length of the previous line as predicted by the VCO 6Fsc oscillator. This oscillator has a time constant of approximately 16 lines and is therefore capable of only relatively long-term corrections. The number stored in the latch is converted to an analog value by a D/A converter.

The pulse developed by the entry flip/flop will actually be three 6Fsc pulses in length if there is no tape error and the 6Fsc oscillator is phase-locked to burst crossing. If an error exists, the pulse will be decreased in direct proportion to the phase errors. The pulse is used to initiate and time out a ramp generator in the phase error voltage generator. The voltage developed by the ramp at the termination of the pulse is stored in a sample-and-hold circuit. This error voltage is a line-by-line measure of velocity error. It is summed with the value from the D/A converter in a summing amplifier and sent to the Parallel/Serial Converter PWA to provide a line-by-line error value on which the velocity compensation option operates.

See Figure 8-7, waveforms M, N, O, P, Q, and R. The output of the phase error voltage generator is also used to modulate the two-stage 3Fsc generator. Modulated 3Fsc from the Tape H Comparator PWA is used by the Memory Control PWA to sample the video signal. The sample must be made at a rate which is consistent with line-to-line velocity errors. Although the chroma may be in error relative to the station master subcarrier, it must be sampled with the velocity errors intact so that it can be clocked out of memory at the correct rate to

achieve time-base correction. The 3Fsc derived from the VCO 6Fsc is phase-modulated by the line-by-line velocity error signal to produce a clock which is phase-locked to H-sync and burst at a rate which reflects actual tape rate.

The VCO write pulse reclock circuit does two things: it provides a measure of the phase relationship of VCO write pulse to the next following VCO Fsc pulse, and reclocks the resulting pulse with the modulated 3Fsc. The reclocked VCO write pulse is one input of the encode Fsc phase shift circuits which will be discussed later.

8-4 Programmable Counter

Following are encoded inputs to the programmable counter:

	Color Normal	Mono Normal	HET Color	HET Mono
Bit 1	1	1 and 0	1	1 and 0
Bit 2	1	1	1	1
Bit 4	0	0 and 1	0	0 and 1
Bit 8	0	1	1	1
Count	12	4 or 1	6	4 or 1

The 7.8-kHz signal gated in by mono mode results in a difference of three 6Fsc pulses from one line to the next. The length of time the programmable counter is permitted to operate will have an effect on the number stored in the Fsc counter latch and ultimately on the voltage developed by the D/A converter.

8-5 Encode Fsc Circuit

The encode Fsc circuit is used in heterodyne mode to phase-lock Fsc to the VCO write pulse. The encode Fsc is reshaped as a sine wave in the color processor and sent to the heterodyne VTR to be used to remodulate the tape chrominance signal (sync-coherent 3.58-MHz out).

In heterodyne mode, H-sync circuits on the Tape VCO PWA are driven by tape H-sync from the Video Input PWA. This signal is derived from off-tape video from the heterodyne VTR. The 6Fsc oscillator on the Tape VCO PWA is phase-locked to the selected H-sync.

The 6Fsc oscillator is applied to a divide-by-1365 counter. One of the decodes of the counter generates the VCO write pulse. The encode Fsc is phase-locked to the VCO write pulse by the entire loop and therefore locked to the tape H-sync.

In the Color Processor PWA, the 3.58-MHz crystal oscillator is phase-locked to the same sync-coherent 3.58-MHz used by the heterodyne VTR remodulation. The output of the crystal oscillator is used to demodulate the B-Y and R-Y signals from the heterodyne VTR chrominance signal. The demodulated B-Y and R-Y signals are then encoded with tape sync-coherent 3.58-MHz. What was an asynchronous chrominance signal from the heterodyne VTR is now sent to the Video Input PWA with chrominance phase-locked to tape H-sync.

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The encode Fsc circuit consists of a divide-by-six counter clocked by $6F_{sc}$ and a three-stage counter circuit used as a digital phase-lock for the divide-by-six counter.

See Figure 8-2. The VCO write pulse clocks a flip/flop which is reset by the following Fsc pulse from a divide-by-six counter clocked by VCO $6F_{sc}$. The result is a pulse width which is proportionate to the time between the two events. This reclocked VCO write pulse enables the first stage of the digital phase lock. The counter is clocked by $6F_{sc}$. The load signal, inhibiting the counter, is removed just prior to the VCO write pulse time by a delayed H-pulse. If the counter result is greater than five at the end of the enable period, the second stage counter will decrement one count. If the result is less than four, the second stage will increment one count. The binary output of the second stage programs the third stage, the third stage is loaded by its carry output which also resets the divide-by-six counter. The third stage is therefore a variable delay to reset the divide-by-six counter, changing the phase relationship of encoded Fsc and VCO write pulse. The reset signal is ANDed with 7.8 kHz and as a result will only be applied to the divide-by-six counter on every other line. In case of a serious phase error, because the second stage counter is changed only one count per alternate line, many lines may be needed to complete the phase shift until the count of the first stage is either 4 or 5, the target window.

See Figure 8-3. From the preceding paragraphs it can be seen that the circuits on the Tape H Comparator, Color Processor, Video Input, and Tape VCO PWAs, and the heterodyne VTR are used as one long servo loop to maintain the sync-to-burst relationship.

8-6 MAINTENANCE

See Figures 8-7 and 8-8 for waveforms, component locator diagram, jumper, test-point, and adjustable component summaries called out in these procedures.

Before undertaking any adjustments to the Tape H Comparator, review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-5 in Part I for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Tape H Comparator and interactive functions between it and other PWAs before making any adjustments.

The Tape H Comparator and Tape VCO PWAs are uniquely interactive and any adjustment to the Tape H VCO PWA should be preceded by Tape VCO PWA checks to ensure the VCO and frequency error discriminator circuits are operating normally.

8-7 Tape H Comparator PWA 4 Alignment

Use tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN. For consistently color-framed edits it is imperative that the

signal generator burst/sync phase be set for RS170A (burst negative-going zero crossing coincident with the 50% point of H-sync leading edge on field 1) or standard reference of the facility.

8-8 Burst Crossing Calibration

STEP 1 With power off extend Tape H Comparator.

Note

Adjustment of R193 is only required when the TBC-3 is used with a VPR-3.

STEP 2 Set R193 (Sch dc gain) to center of its range.

STEP 3 Set R1 (burst/sync phase) to center of its range.

STEP 4 Connect oscilloscope: CH1—TP10 (burst crossing), CH2—PWA pin 69. Trigger PWA pin 25. Use delayed sweep and chop mode to display burst and two pulses as shown in WF4/29(V).

STEP 5 Adjust R117 (burst crossing) so negative edge of the later of the two pulses occurs just before peak of burst.

STEP 6 Carefully readjust R117 until EDIT READY light on control panel is illuminated.

STEP 7 Adjust R1, BURST/SYNC Φ , counterclockwise until EDIT READY light is extinguished. Note position of R1.

STEP 8 Adjust R1 clockwise until EDIT READY light comes back on and then goes out again. Note position of R1.

STEP 9 Set R1 midway between two points noted above. Verify that EDIT READY light is illuminated in this center position.

STEP 10 Verify a dc level of $+3.2 \pm 0.3V$ at U56-6 with EDIT READY on.

8-9 R193 Adjustment

STEP 1 Place VPR-3 in E-E mode.

STEP 2 Set VPR-3 UNITY/VAR to VAR.

STEP 3 Pull VPR-3 Sch Φ control knob out to variable. Turn knob in one direction and then the other so VPR-3 phase meter reads between limits of $+40^\circ$ and -40° . Observe that EDIT READY light is on steady but begins to flicker when the $+40^\circ$ and -40° limits are reached.

STEP 4 Adjust R193 so requirements of step 3 are met.

STEP 5 Repeats steps 3 and 4 as necessary to obtain desired results.

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8-10 Tape H-Sync-to-Video Timing

If the Tape H Comparator, Tape VCO, or Memory Control PWAs are repaired or the TBC is phased to a nonstandard reference, H-sync timing may require readjustment.

- STEP 1 Use tape/reference test loop setup with a 75% split field color-bar signal at standard level and sync/burst phase (or nonstandard facility reference) connected to TAPE VIDEO IN.
- STEP 2 Set MODE to NORMAL.
- STEP 3 With power off, remove Video Input PWA and connect a clip lead to TP12. Lead should be long enough to reach any convenient grounding point after PWA is reinserted into cage.
- STEP 4 With power off, extend Tape VCO PWA.
- STEP 5 Switch power on and verify that EDIT READY and Sync Generator PWA REF SYNC/BURST calibration indicators are on. Refer to tape H comparator and sync generator alignment procedures if indicators are not on.
- STEP 6 Connect oscilloscope to VIDEO OUT 1 and using delayed sweep, line up leading edge of white bar on the center graticule. Use sufficient sensitivity to see any horizontal shift within a subcarrier cycle. This will be reference point for next steps.
- STEP 7 ** VIDEO INPUT PWA*
Ground TP12-connected clip lead and note any shift of video.
- STEP 8 ** TAPE VCO PWA (5)*
Adjust R53 (H-sync phasing) to reposition white bar edge on the center graticule.
- STEP 9 Alternately open and short clip lead to ground while adjusting R53 for minimum horizontal shift.
- STEP 10 With power off remove clip lead from TP12 and return both PWAs to the cage.
- STEP 11 Turn power on and switch TBC between NORMAL and BYPASS. Note any shift in picture position.
- STEP 12 If there is a shift in picture position, turn horizontal phasing thumbwheel on Memory Control PWA to a position that minimizes horizontal shift.
- STEP 13 Switch TBC power on and off several times and verify that picture position remains the same.

8-11 Comparator Timing Adjustment

- STEP 1** Connect oscilloscope as follows: CH1—U25-12 (PWA pin 26, comparator timing). Trigger on U31-1. Use delayed sweep to display pulse shown in WF30(W).
- STEP 2** Set R2 to center of its range. The final setting for R2 will be made with write pulse reclock phase adjustment of paragraph 8-14.
- STEP 3** Adjust R128 (phase balance) minimum jitter of positive edge of pulse. The top trace of WF30(W) shows correct adjustment. The effect may also be seen with a vectorscope on video output where R128 is adjusted for minimum jitter of blue vector.

8-12 Phase Modulator Offset Search Adjustment

- STEP 1** Connect oscilloscope triggered on line or a digital voltmeter for a dc measurement at TP8.
- STEP 2** Position jumper J1 to B-C.
- STEP 3** Adjust R54 (test phase modulation) for -15 Vdc at TP8.
- STEP 4** Return J1 to A-B. R54 may be set for -0.8 Vdc in a dynamic mode (J1 in A-B) with VPR in shuttle at a speed that shifts picture to monochrome.

8-13 Tape 3 Fsc Symmetry Adjustment

- STEP 1** Connect oscilloscope triggered on internal to PWA pin 64 (tape 3Fsc).
- STEP 2** Adjust R180 (clock symmetry) so that slopes of lower 50% of waveform are symmetrical.

8-14 Write Pulse Reclock Phase Adjustment

- STEP 1** Connect oscilloscope as follows: CH1—TP4 (VCO write pulse). Trigger, signal generator H sync.
- STEP 2** Use delayed sweep and chop mode to display the two pulses (fields I, II).
- STEP 3** Adjust R2 fully clockwise, then counterclockwise until the right-hand pulse is between 130 and 150 ns at the 50% point as shown in WF31(X). The pulse width will change in 46-ns increments (6Fsc rate).

8-15 Heterodyne and Slow Motion Encode Fsc Symmetry Adjustment

- STEP 1** Connect oscilloscope as follows: CH1—U29-10 (PWA pin 75—encode Fsc). Trigger internal.
- STEP 2** Switch MODE to HET.
- STEP 3** Adjust R25 (symmetry) for a symmetrical square wave.

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STEP 4 Return MODE to NORMAL.

8-16 Velocity Compensator Line Error Adjustment

The R3/R4 modulator adjustments and the velocity compensation adjustments on PWA 13 are made at the factory with a highly accurate servo test instrument and should not be adjusted unless the need is well established. This procedure should precede the PWA 13 adjustments.

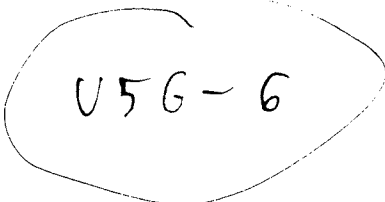
- STEP 1** With power off remove jumper J2 from P/S Converter PWA 13 and return PWA to its slot. This disables the second-order correction.
- STEP 2** Make the normal VTR/TBC hookup and monitor VIDEO OUT 1 with the vectorscope. Do not extend the PWA for the R3/R4 adjustment below.
- STEP 3** Play a recording of 75% color bars.
- STEP 4** Adjust R3 (phase modulator gain) for a minimum yellow vector dot.
- STEP 5** Switch velocity compensator on (PWA 13 S1 up).
- STEP 6** Adjust R4 (velocity balance) for minimum vector dot spread on blue vector.
- STEP 7** With power off return PWA 13 jumper J2 to A-B.
- STEP 8** Readjustment of chroma phase (PWA 15 R 146) may be required. Refer to sync generator PWA adjustment section.

8-17 Slow/Reverse/Still-Motion Adjustment with VPR-2B/VPR-3

Adjustment with the VPR requires a normal VPR/TBC configuration with both units fully operational and properly phased to the system reference (RS170A sync/burst phase or the facility standard reference). It is crucial to maintain normal video from the VPR for this procedure.

- STEP 1** Verify normal chroma output from the chroma inverter circuits of the Color Processor PWA as outlined in paragraph 5-9, heterodyne/VPR slow motion output.
- STEP 2** Connect waveform monitor and vectorscope to VIDEO OUT 1.
- STEP 3** Make a 10-min recording of split field color bars (RS170A or facility standard sync/burst phase).
- STEP 4** With power off extend tape H comparator.
- STEP 5** Connect digital voltmeter to TP12 (dynamic error).
- STEP 6** While playing back tape adjust R108 (dc offset) for 0.0 ± 0.1 Vdc at TP12.

- STEP 7** Connect digital voltmeter to U44 pin 7.
- STEP 8** Play back tape at normal speed and verify that EDIT READY indicator is on and voltmeter reads $4.10 \pm 0.01V$ at U44-7.
- STEP 9** On waveform monitor on VIDEO OUT 1, expand (x25 magnification) rising edge of I and Q signal of the split field and set this edge to a reference point on the graticule (or use the transition between green and cyan bars) for observation of picture shift during next step.
- STEP 10** Shift VPR to full-speed slow motion (carefully, to avoid losing head-to-tape contact), then to still frame and to full-speed reverse motion and observe the following:
- EDIT READY stays on.
 - No picture shift.
 - U44-7 voltage stays within 4.07—4.13V.
- If any of these conditions are not met the R170 (slow-motion static error) and R157 (slow-motion dynamic error) adjustments of steps 12 through 15 are required.
- STEP 11** Continue playback and turn VPR speed control to still frame mode (center detent).
- STEP 12** Verify that R157 is near mid-range and adjust R170 for 4.10 ± 0.1 Vdc at U44-7.
- STEP 13** Try step 9 again and note voltage at full speed forward and reverse motion. If voltages in step 9 are between 4.07 and 4.13V, go to next step. If not, with VPR in full-speed reverse slow motion, adjust R157 for a voltage at U44-7 midway between voltages noted in previous steps. Repeat steps 9-12 until voltage at U44-7 is between 4.07 and 4.13V.
- STEP 14** Play back VPR in normal speed and note position of vectors on vectorscope.
- STEP 15** Play back VPR in full speed reverse slow motion. Adjust R155 for vectors in same location as in play on vectorscope.
- STEP 16** Play back VPR in all speeds of slow motion: REVERSE, STILL, and FORWARD. Verify no picture shifts, no vector shifts, clean picture with no break-up, EDIT READY stays on, and colors are correct. Verify with VPR sync head both off and on (VPR-2B PWA 8).
- STEP 17** With power off return Tape H Comparator to rack.



U5G-6

TBC 3

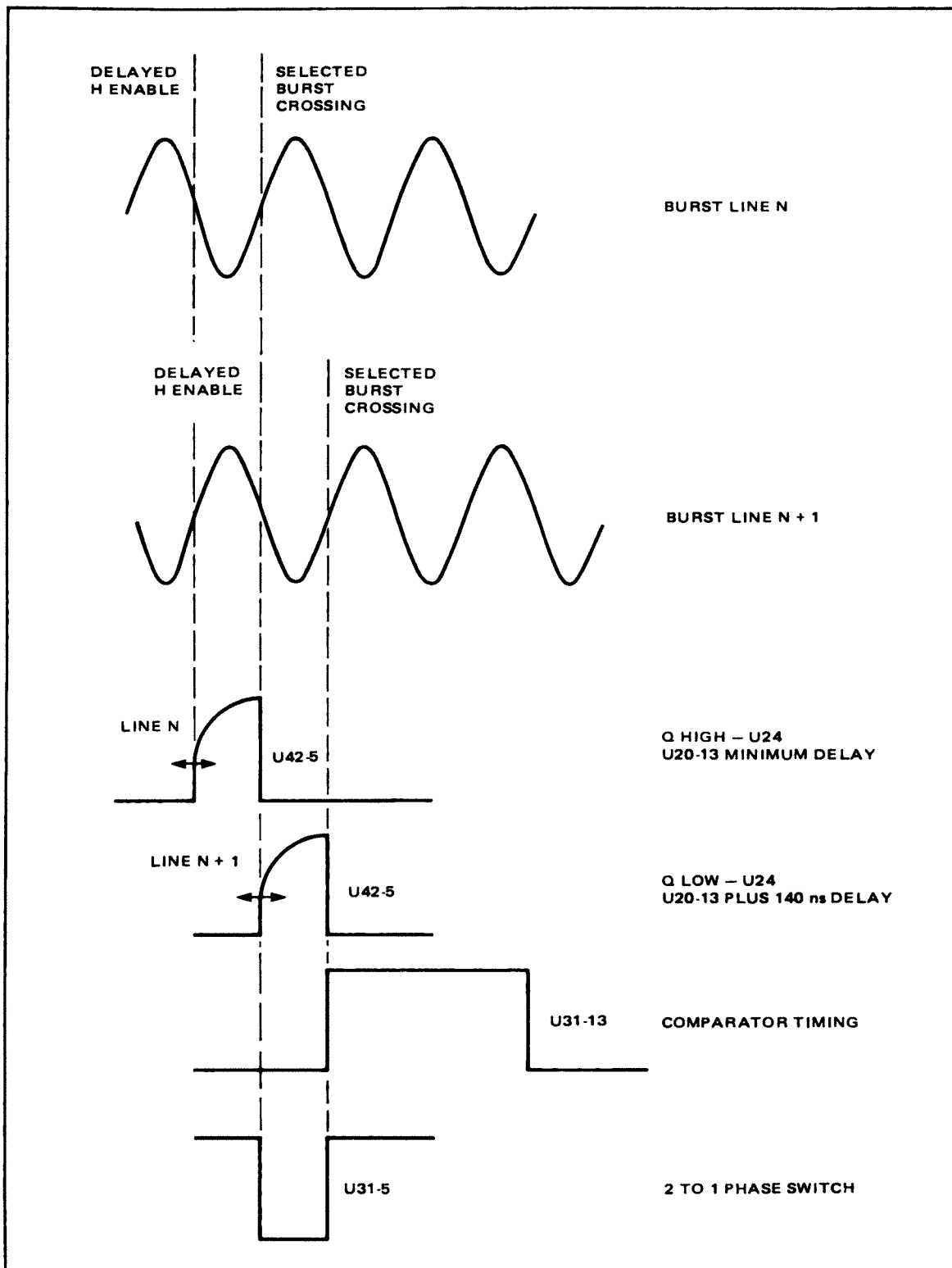


Figure 8-1. Selected Burst Crossing Timing Relationship

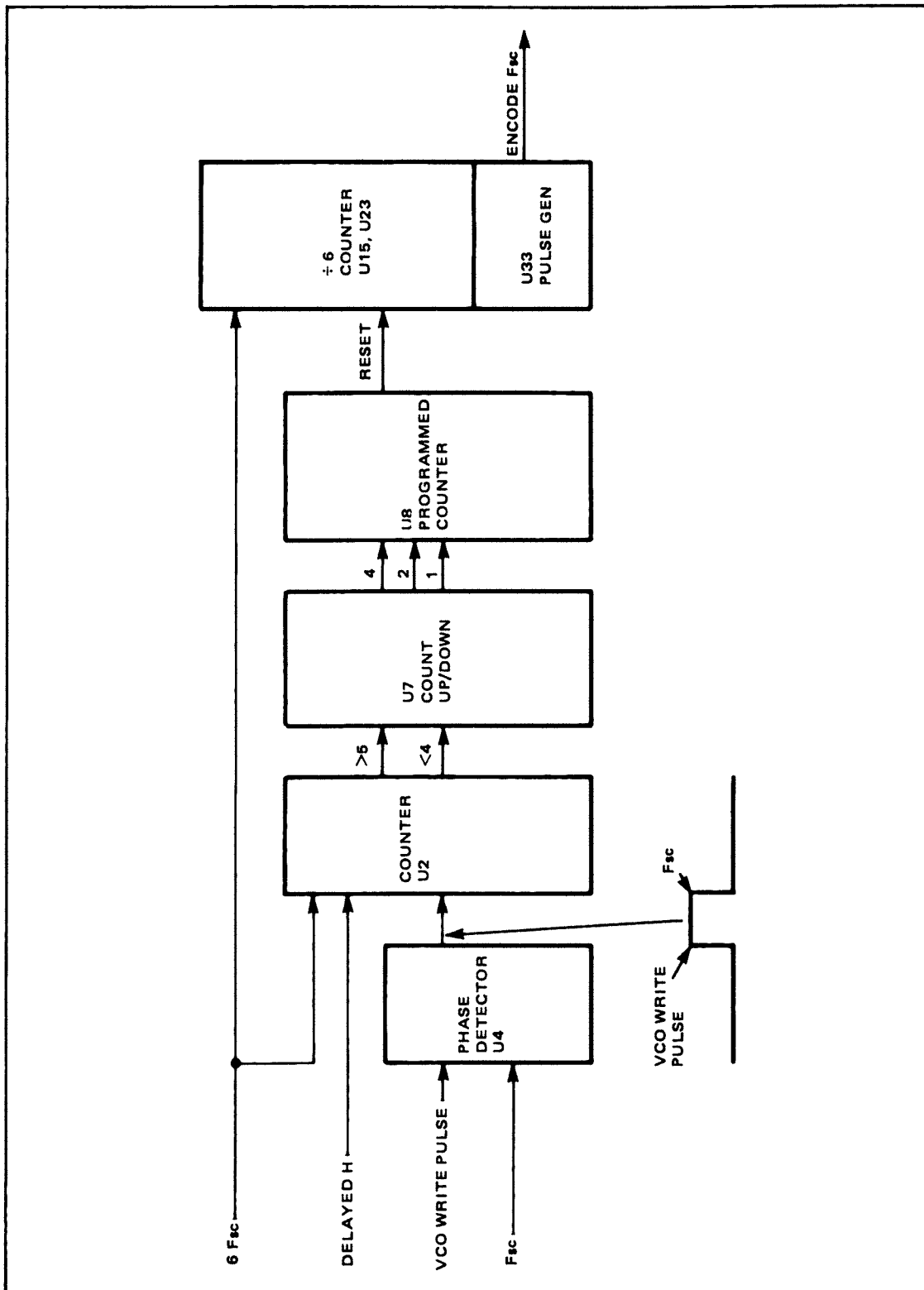


Figure 8-2. Encode Fsc Circuit Block Diagram

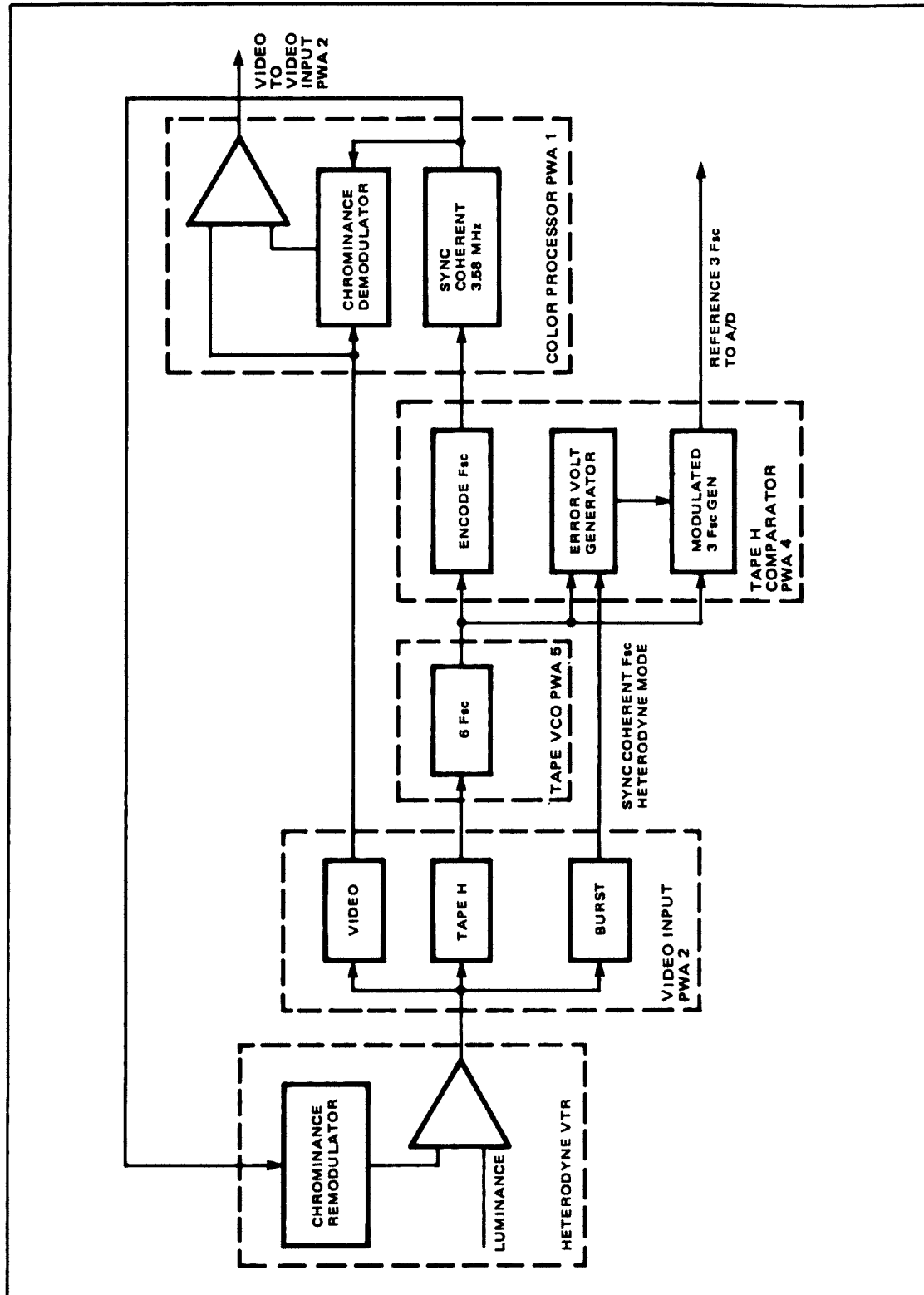


Figure 8-3. Heterodyne Two-Wire Connector

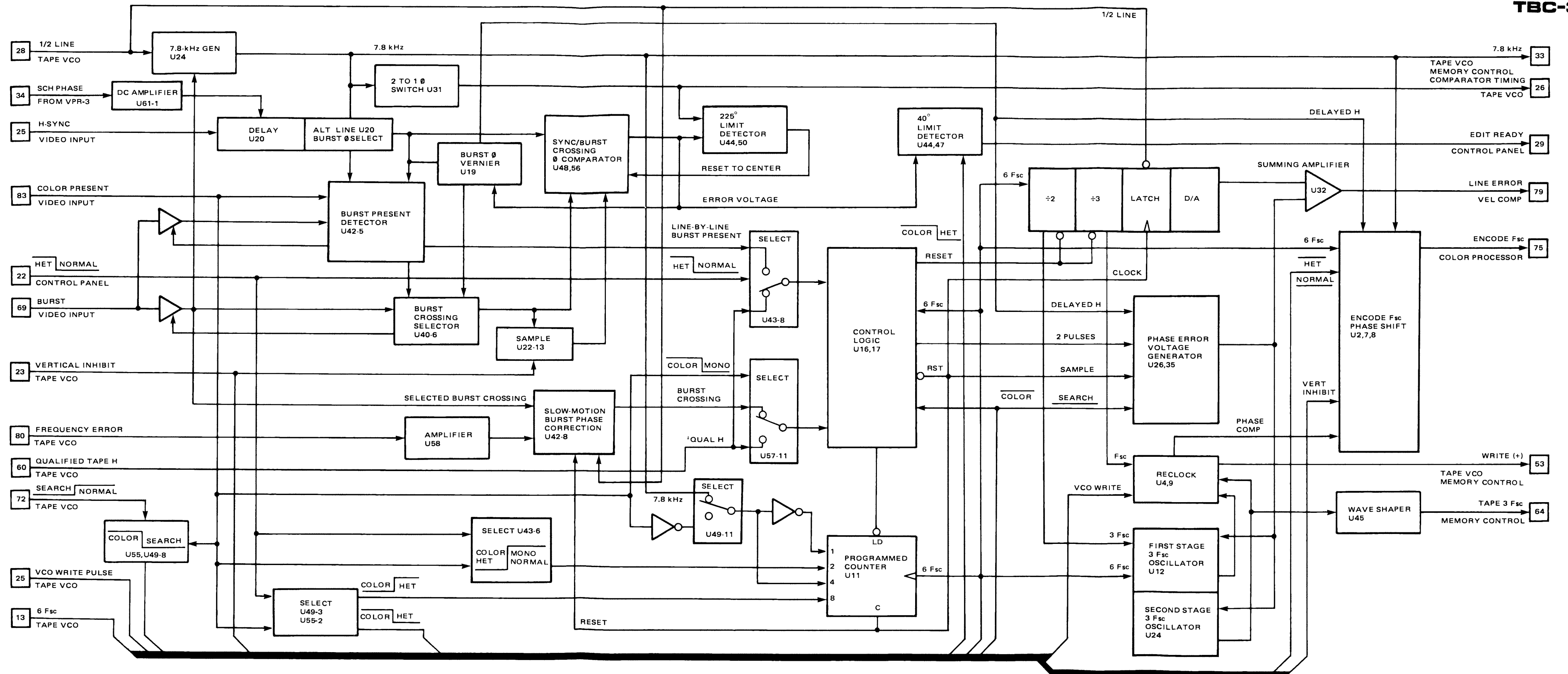


Figure 8-4.
Tape H Comparator PWA 4, Block Diagram

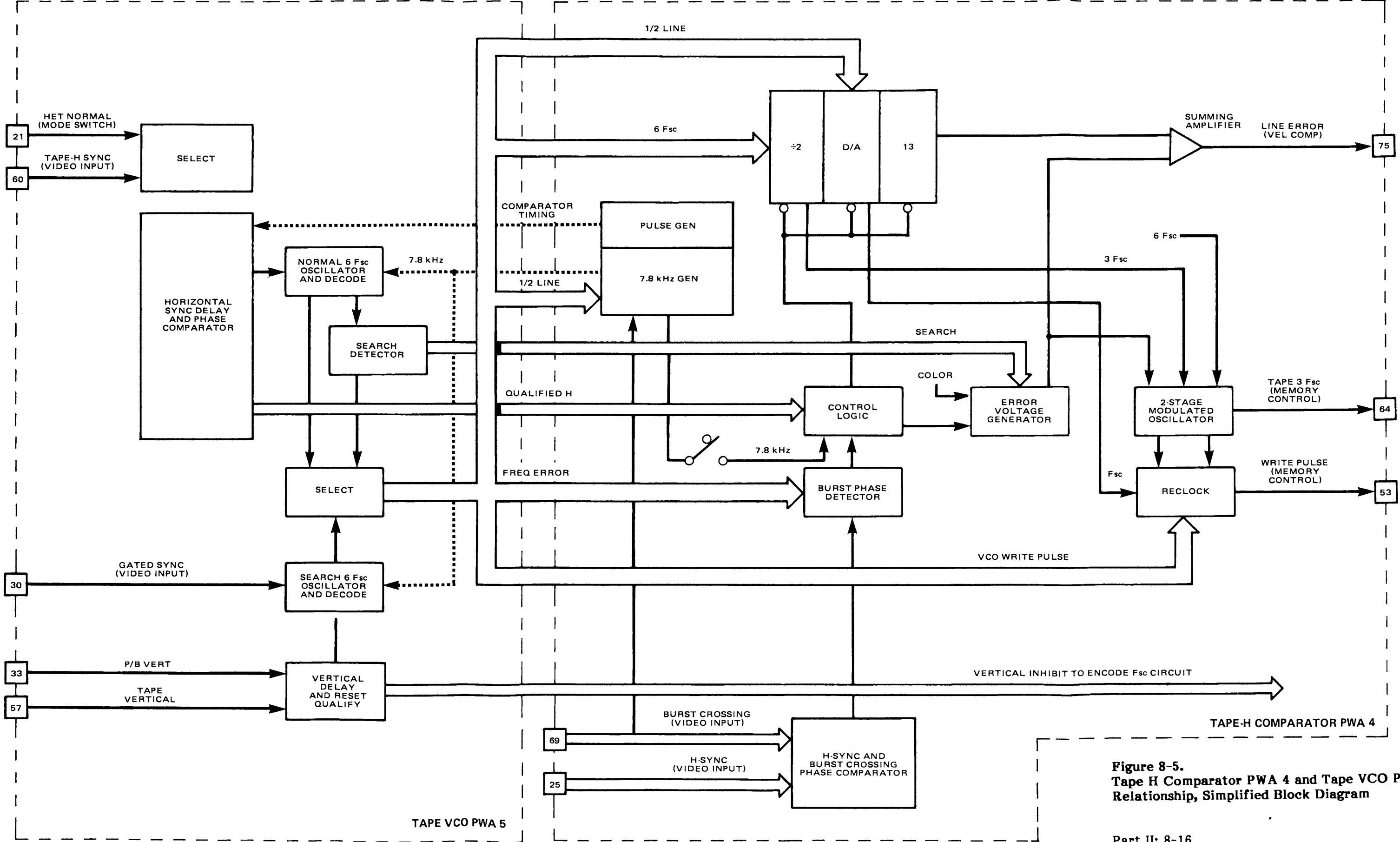


Figure 8-5.
Tape H Comparator PWA 4 and Tape VCO PWA 5 Signal
Relationship, Simplified Block Diagram

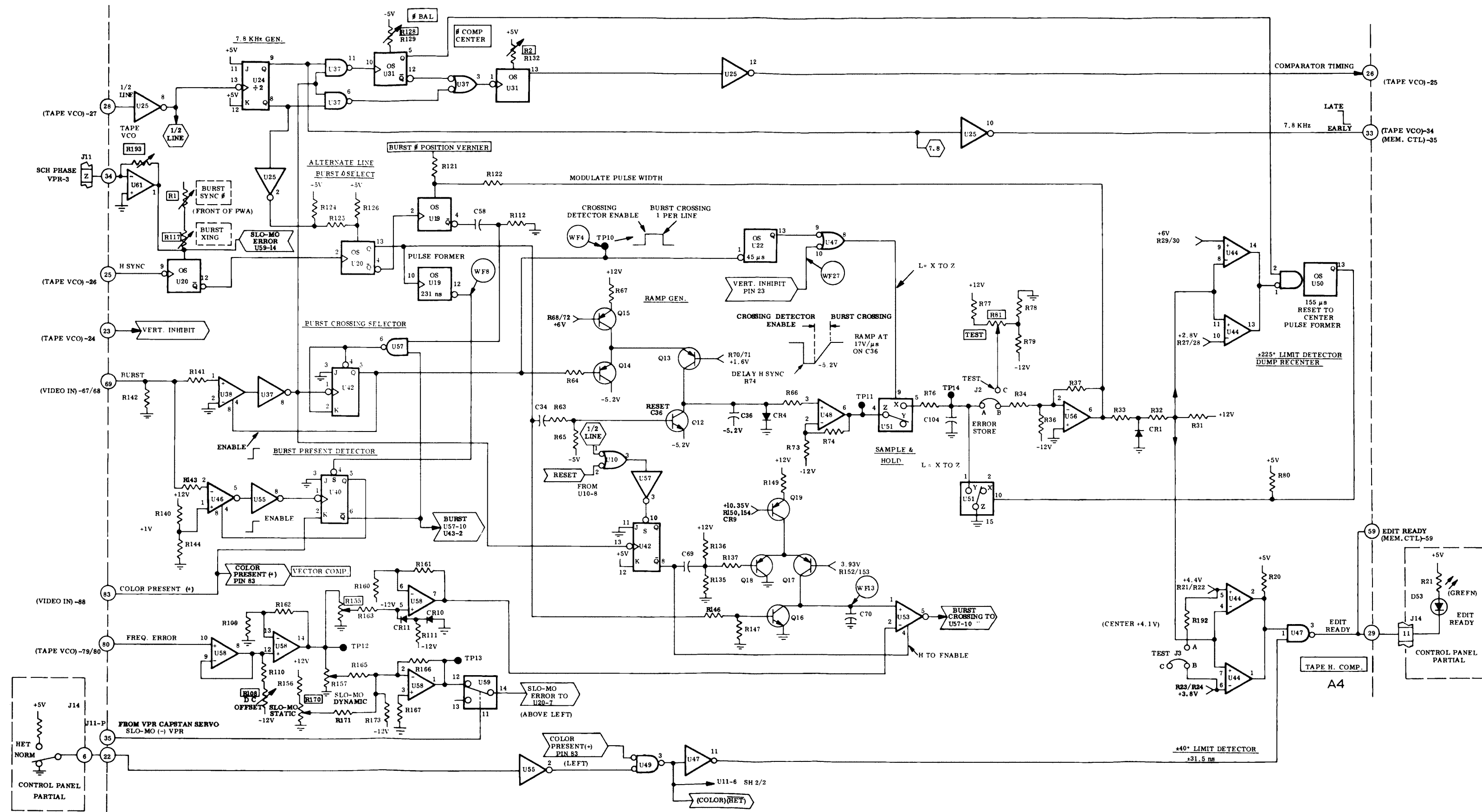


Figure 8-6.
Tape H Comparator PWA 4 Simplified Schematic
(Sheet 1 of 2)

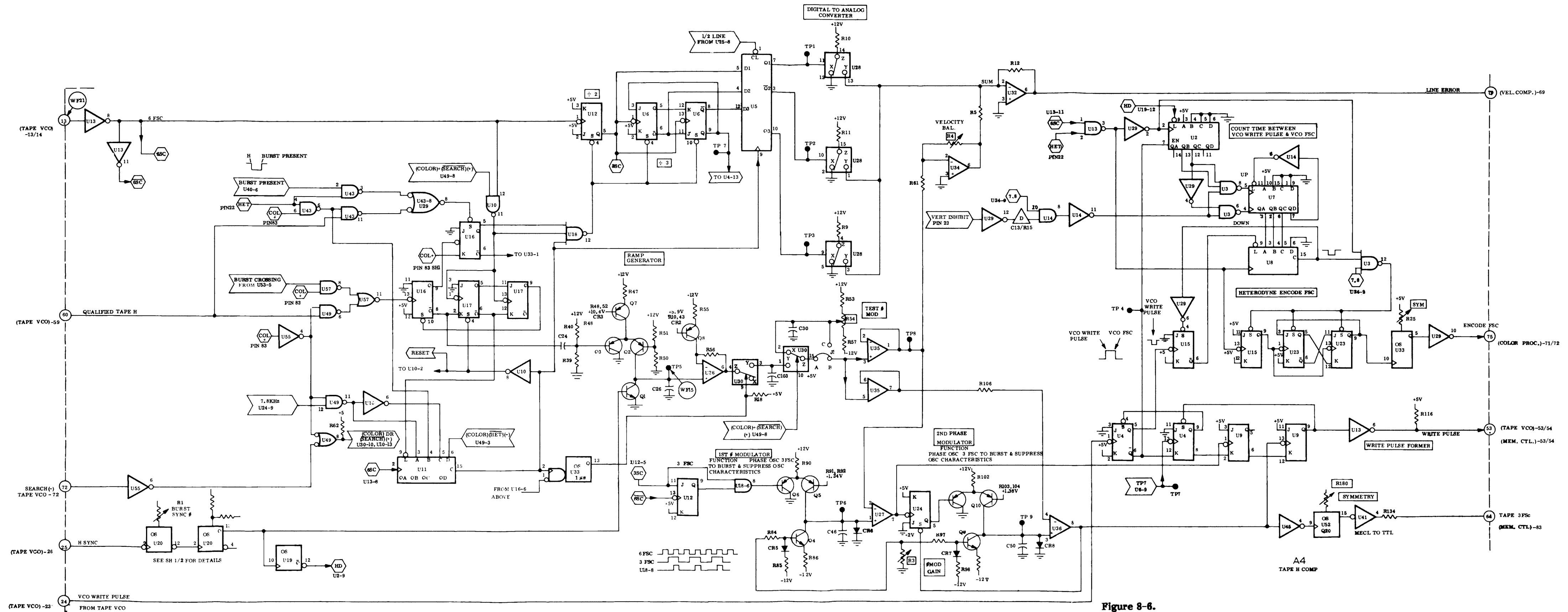


Figure 8-6.
Tape H Comparator PWA 4 Simplified Schematic
(Sheet 2 of 2)

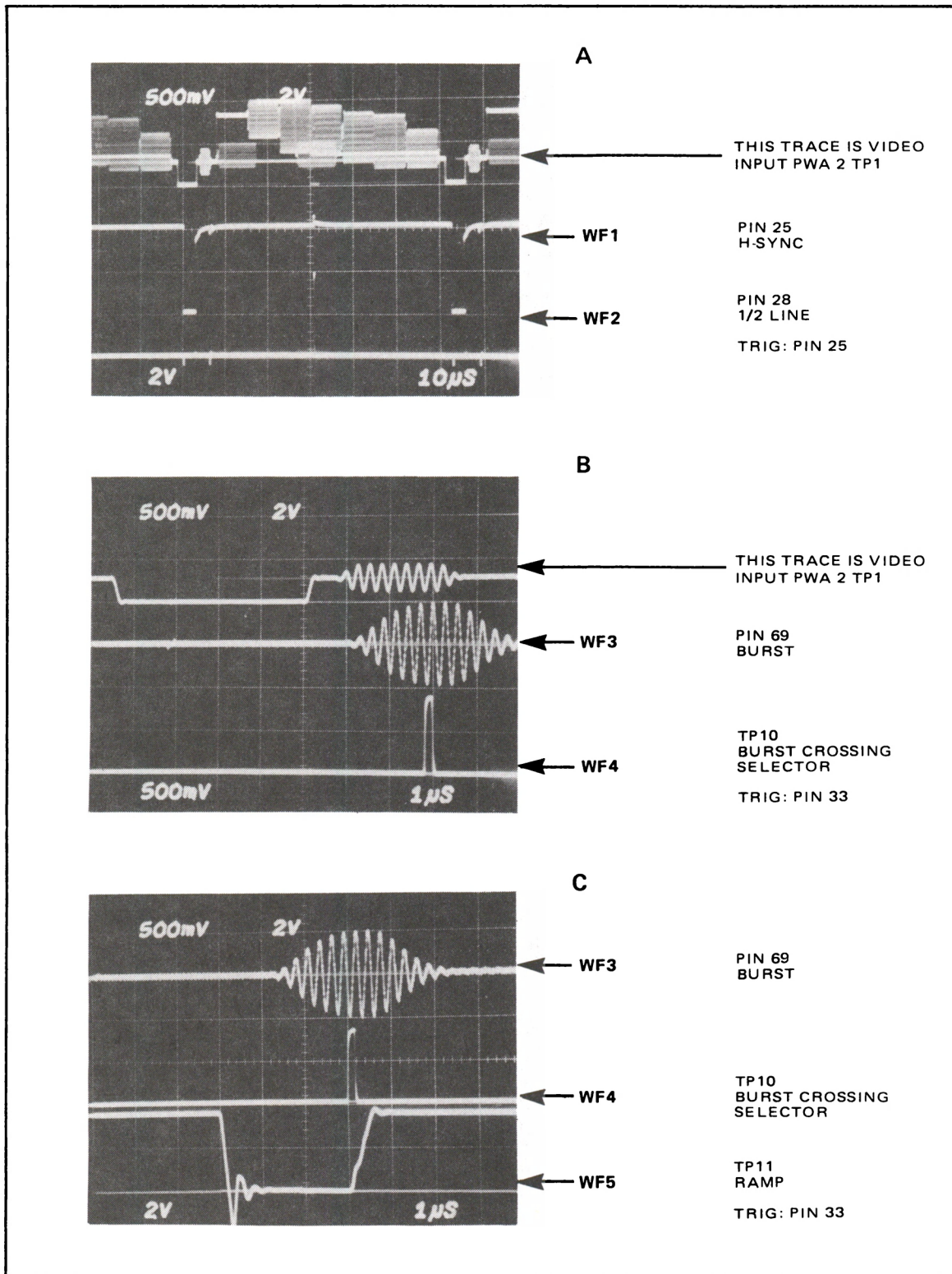


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 1 of 8)

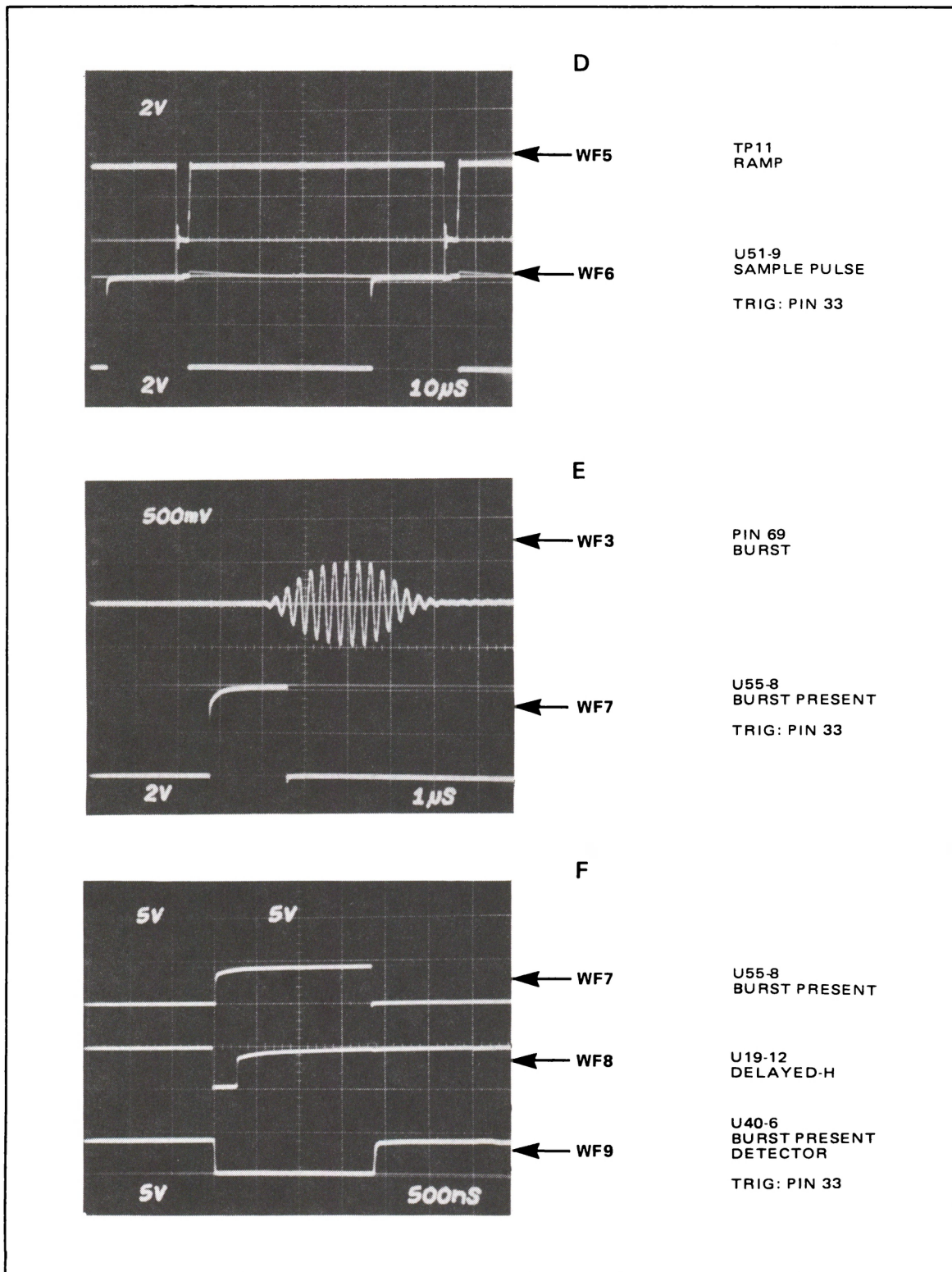


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 2 of 8)

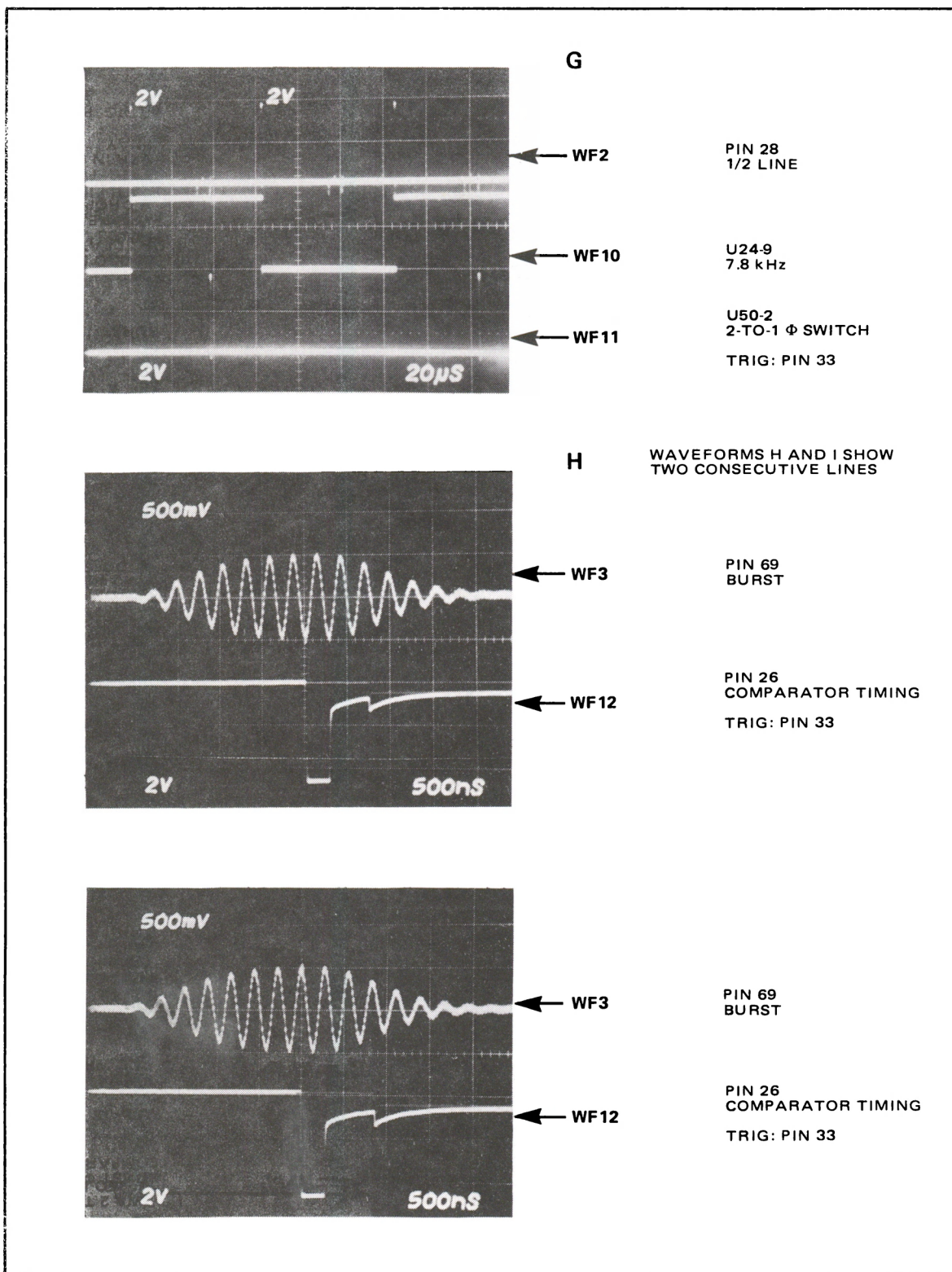


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 3 of 3)

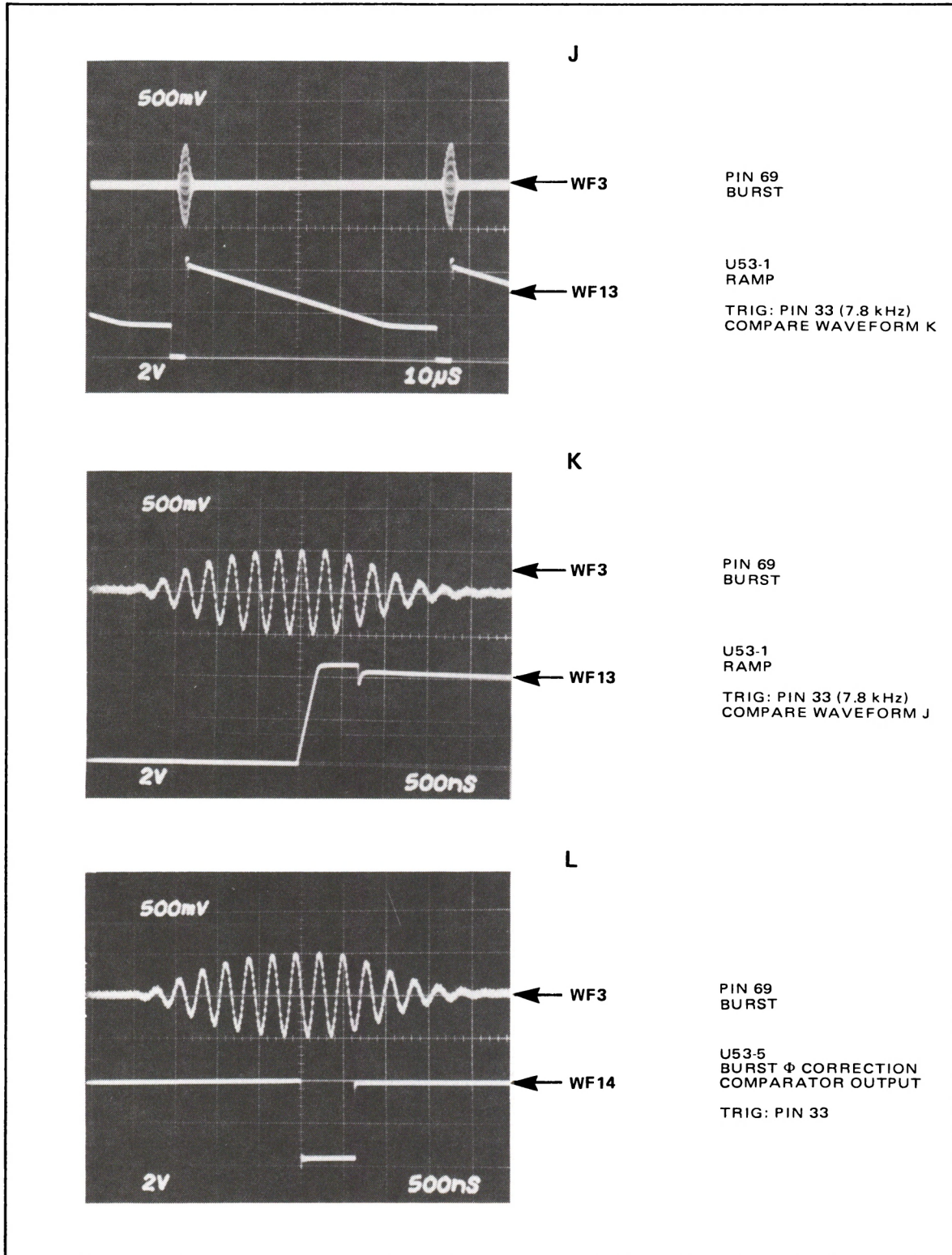


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 4 of 8)

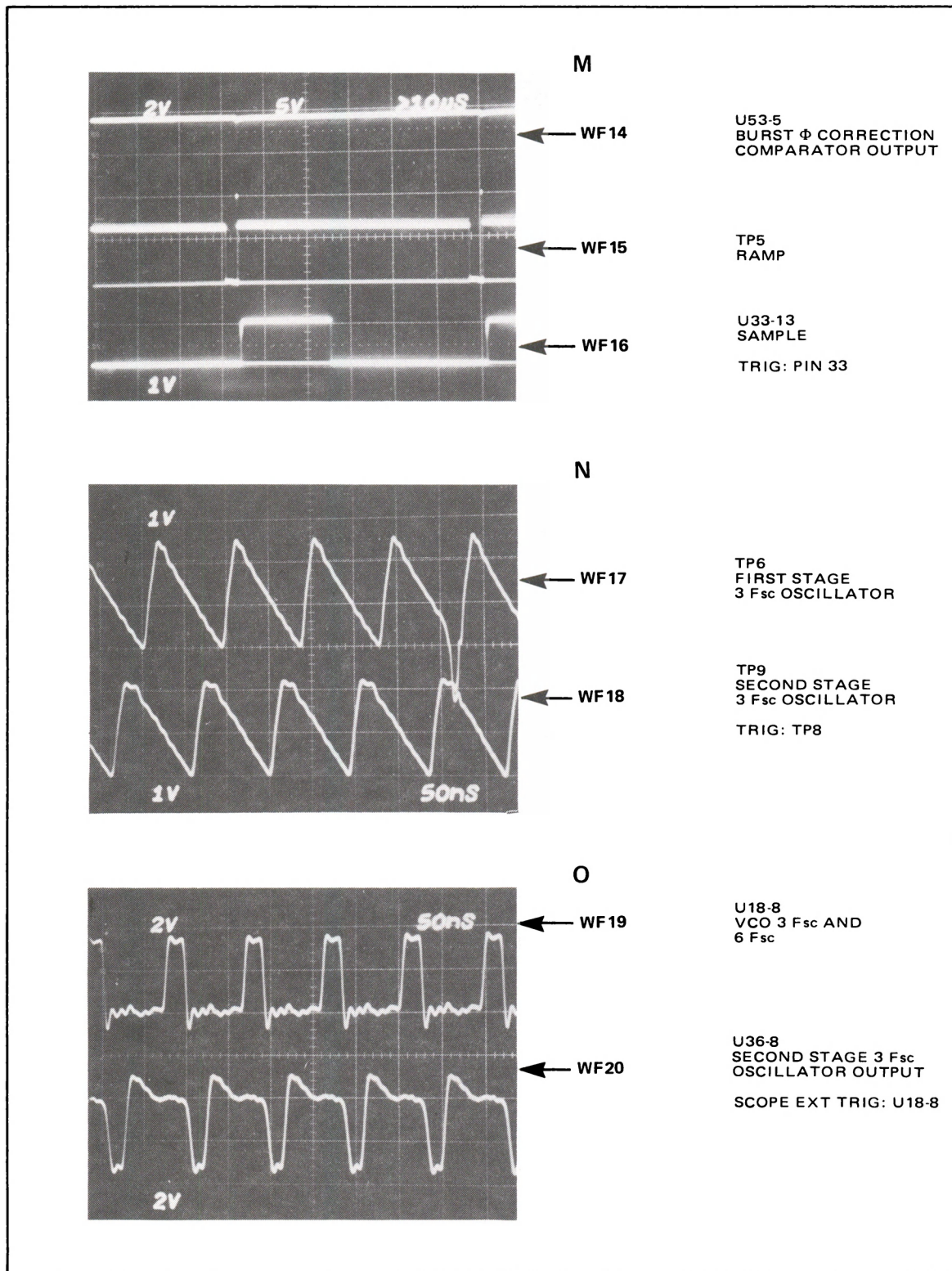


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 5 of 8)

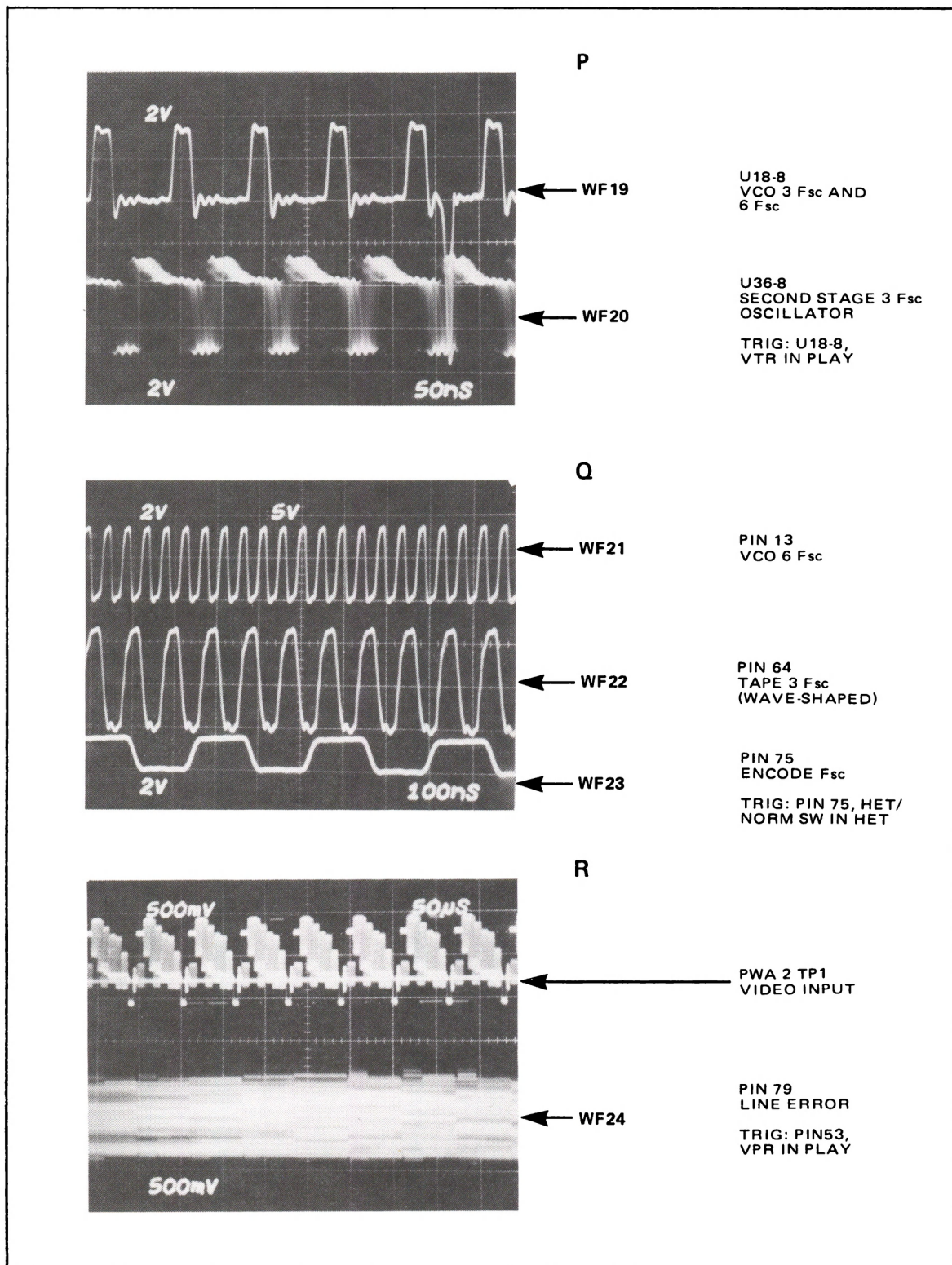


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 6 of 8)

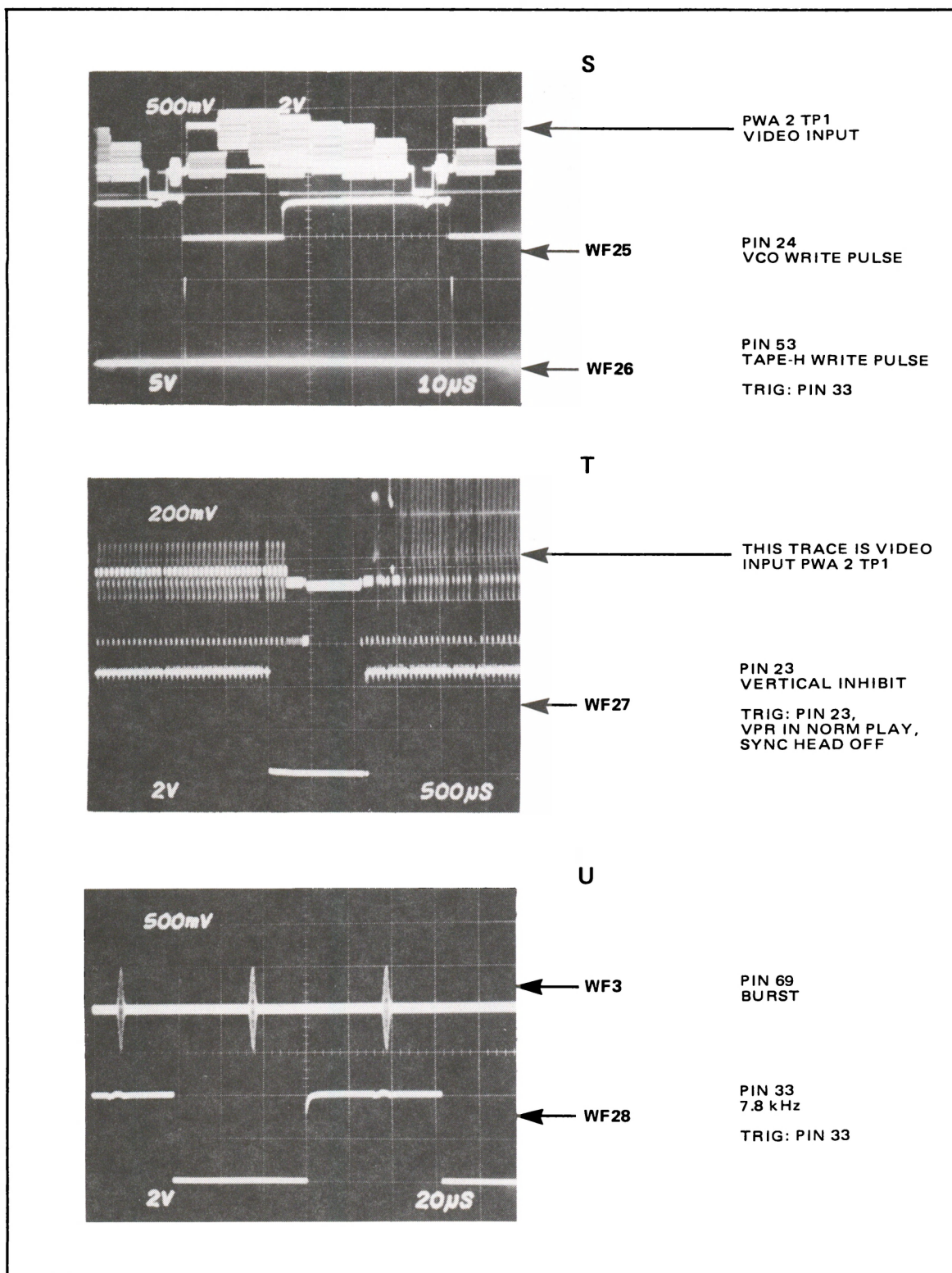


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 7 of 8)

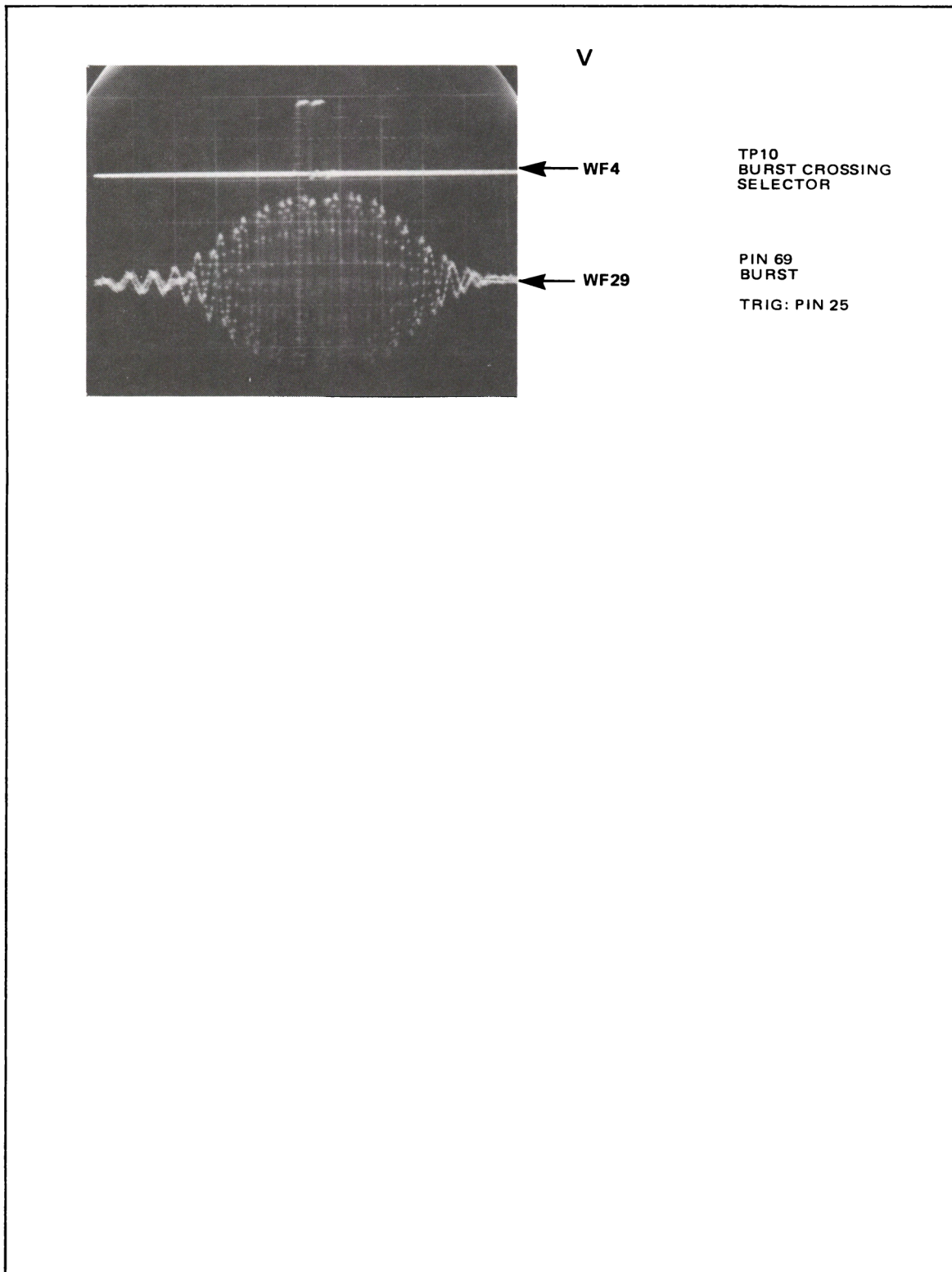
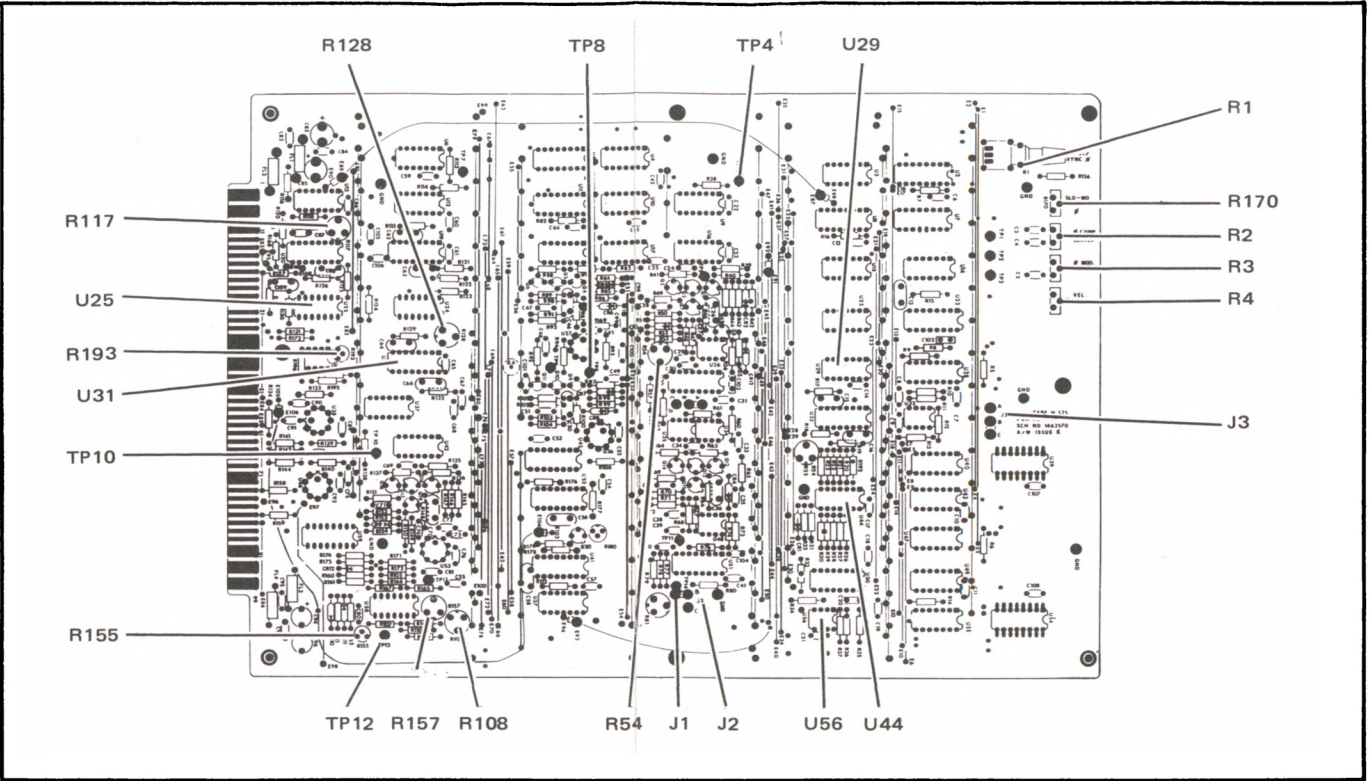
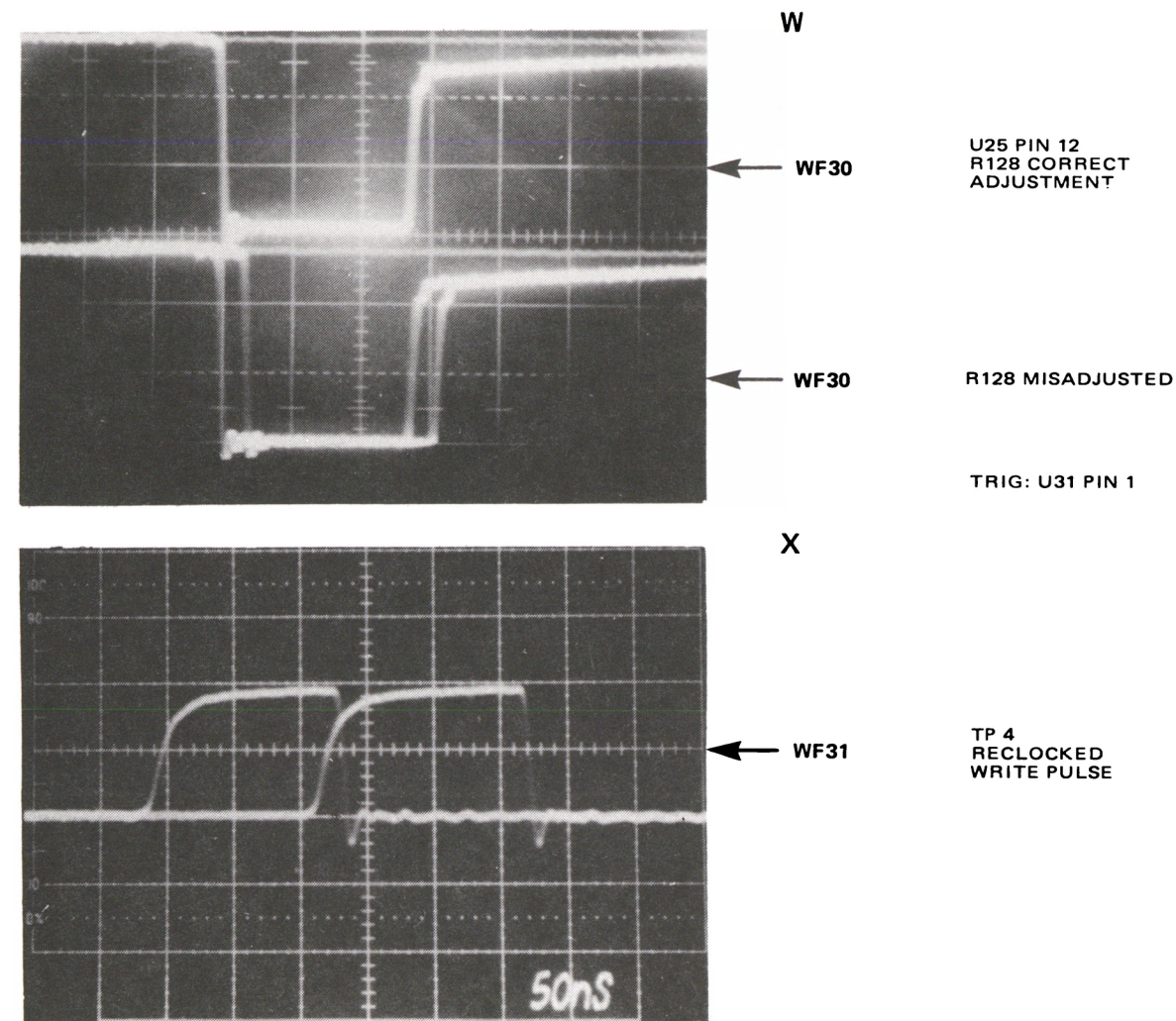


Figure 8-7. Tape H Comparator PWA 4 Waveforms (Sheet 8 of 8)



PWA 4 Component Locator

PWA 4 Jumpers		
Jumper	Position	Function
J1	A-B	Phase Modulation
	B-C	Normal Test –inserts fixed error voltage
J2	A-B	Edit Ready Loop Test
	B-C	Normal Inserts variable error voltage
J3	B-C	Edit Ready Window
	A-B	Normal: 40° window Approx 10° window

PWA 4 Test Points	
Test Point	Function
TP1	Vel comp 1/2-line error
TP2	Vel comp line error
TP3	Vel comp 2-line error
TP4	VCO write pulse
TP5	Gated H-rate ramp
TP6	3X subcarrier sawtooth
TP7	Subcarrier pulse
TP8	Line-by-line error
TP9	3X subcarrier sawtooth
TP10	Burst crossing
TP11	Gated H-rate ramp
TP12	Dynamic error voltage
TP13	Static error voltage
TP14	Error store

PWA 4 Adjustable Components	
Component	Function
R1	Burst sync phase
R2	Phase comparator center
R4	Velocity balance
R3	Phase modulator gain
R25	Symmetry
R54	Test phase modulation
R81	Test
R108	Dc offset
R117	Burst crossing
R128	Phase balance
R155	Vector compensation
R157	Slow motion dynamic
R170	Slow motion static
R180	Clock symmetry
R193	Sch dc gain

Figure 8-8.
Waveforms, Component Locator, Adjustable Components,
Test Points, Jumpers, Tape H Comparator PWA 4

PART II

SECTION 9

TAPE VCO PWA 5

DESCRIPTION AND MAINTENANCE

9-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463528

Schematic No. 1464530

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 9-4, overall block diagram
- Figures 9-5 through 9-8, simplified schematics
- Figure 9-9, waveforms
- Figure 9-10, maintenance data

Tape VCO PWA 5 function summary:

- Accepts vertical and horizontal sync from Video Input PWA 2 and playback mechanism and processes it to produce synchronizing signals for use throughout the TBC.
- Contains three oscillators that produce a 6Fsc signal used by the Tape H Comparator PWA to develop the tape 3Fsc and write pulses. Tape H comparator also develops the encode Fsc signal, used by the Color Processor PWA, from the 6Fsc signal.

Normal 6Fsc oscillator: An LC VCO used in normal operating mode and slow-motion. This oscillator is slaved to selected off-tape burst crossing. Locked to H-sync during monochrome operation.

Search-up oscillator: An RC voltage-controlled oscillator from which system write timing is derived during rewind shuttling. Oscillator is normally used during rewind shuttling, depending on rewind speed; locked to tape H, produces 6Fsc.

Search-down oscillator: An RC oscillator from which system write timing is derived during forward shuttling; locked to tape H, produces 6Fsc.

9-2 DESCRIPTION

Tape VCO PWA 5 accepts vertical and horizontal sync from Video Input PWA 2 and the playback mechanism, and processes it to produce synchronizing signals for use throughout the TBC (see Figures 9-1 and 9-2).

TBC-3

The normal horizontal reference is a selected burst crossing (color burst crossing through the zero point of the sine wave). The normal vertical reference is playback vertical which is predicted vertical sync from the playback mechanism. Tape H-sync and tape vertical sync from Video Input PWA 2 are used in special conditions such as shuttle or monochrome playback.

The Tape VCO PWA has three oscillators. The first is a normal voltage-controlled 6Fsc LC oscillator, which is phase-locked to the incoming H-rate signal. The basic relationship between H-rate and subcarrier is:

$$H = \frac{2Fsc}{455} \qquad H = \frac{2 \times 3Fsc}{13 \times 105}$$

$$H = \frac{6Fsc}{1365}$$

$$Fsc = 3.579545 \text{ MHz} \quad 6Fsc = 21.47727 \text{ MHz}$$

$$1 \text{ cycle of } 6Fsc = 46.56 \text{ ns}$$

The other two oscillators are RC voltage controlled oscillators located in the search oscillator circuitry. The search mode of operation is controlled by the position of Jumper J1. Position A-B, internal search, is always used for the VPR-2B. In this position, the normal 6Fsc oscillator operates until an error threshold is reached. This enables the search oscillator and switches control of the Tape VCO PWA synchronizing signals from normal oscillator circuits to search oscillator circuits.

Jumper J1 position B-C, external search, is always used for the VPR-3. In position B-C, the VPR-3 command (pin 74) places the Tape VCO PWA into search mode. This also enables the wide (-) and up (-) (pins 71 and 82) signals derived in the Video Input PWA to select the search up oscillator U81-7 or search down oscillator U81-10. In heterodyne mode, search mode is inhibited when operating with a VPR-2B or VPR-3 regardless of position of jumper J1. This permits the TBC-3 to be used in a preprocess mode when the VPR-3 is in the record mode.

The output of the normal 6Fsc oscillator is applied to a divide-by-13 counter. The 8-bit count (1.65-MHz rate) clocks the divide-by-105 counter. The final count of 1365 resets the divide-by-105 counter and loads an initial count of 25. The divide-by-13 counter is reset by its carry output and loads an initial count of three. The count of 1365 is one horizontal line in time and is therefore a prediction of the time of arrival of the delayed H-rate pulse. The digital phase comparator generates an error voltage proportional to the phase difference of these signals and thereby forms a closed loop which locks 6Fsc oscillator in phase with the incoming H-rate signal. The synchronizing signal for all except the format gap during the vertical interval is the color burst crossing. The 6Fsc oscillator is therefore in phase with the tape color burst. All of the timing components of the television signal are derived from the subcarrier frequency. The frame rate is H/525, and the field rate is 2H/525. In addition, in the TBC Tape H Comparator PWA 5 drives a 3Fsc signal from the tape VCO 6Fsc which is used by A/D Converter PWA 4 to sample the video at 3Fsc rate (10.7 MHz) prior to placing the digitized information in memory.

Several forms of timing error are introduced in the process of video tape recording. One is impact-generated by the head entering or leaving the tape and other mechanical irregularities inherent in the recording and playback process; another is program material from recordings that may not be properly time-base corrected. In slow motion or freeze the field is reproduced with an incorrect tape speed. In freeze, the tape is stationary and there is a 1% error in tip-to-tape velocity. Therefore a horizontal line is lengthened by 1%, subcarrier (burst) frequency is changed by 1%, and the field is reduced by 1%, (two and one-half lines). Video written into memory in digital form must be synchronized to the playback subcarrier, although, because of time distortion, that subcarrier frequency is not precisely 3.579545 MHz. The only measure of the subcarrier and its distortion by the record/reproduction process is the 9 to 10 cycles of burst on the back porch of the horizontal sync. In lines 1 through 9, color burst is not available. In addition, the helical recorder format gap occurs in lines 3 through 14. The horizontal synchronizing signal is switched from burst crossing to Tape H Sync in lines 2 through 9, allowing the Tape VCO PWA to maintain the integrity of its synchronizing outputs during the vertical interval. (See Figure 9-9, waveforms U and V.)

9-3 Decoding—Normal 6Fsc Oscillator

In the normal 6Fsc circuit, various outputs of the counter are decoded to provide synchronizing signals within the TBC-3. Because the Tape VCO is slaved to burst crossing, the predicated delayed H-pulse (1365) is generated approximately 7.6 μ s after the leading edge of horizontal sync (see Figure 9-3 and waveform H on Figure 9-9). A decoded count of 507 provides the 1/2-line pulse. The decoded count of 1201 provides flywheel sync which, is nominally (± 2 cycles of Fsc) coincident with the leading edge of horizontal sync. The decode of 1352 triggers the window of the tape-H quality circuit (see Figure 9-9, waveforms I, M). The 1.65-MHz signal (8 bits of the divide-by-13 counter) is applied to a frequency discriminator to produce a frequency-error signal to the Tape H Comparator PWA. It is also used, when no external input is available, to determine tape direction in fast forward or reverse. The discriminator output is nominal 6.5V in normal tape speed with a 200-mV change per 1% change in oscillator frequency.

A decoded count of three from the divide-by-13 counter is gated by 7.8 kHz from the Tape H Comparator. At the time of the count of 1365 the 7.8 kHz will be high for one line and low for the next. If 7.8 kHz is high, the count of three will be ANDed with the 1365 pulse. The start of the VCO write pulse will be 140 ns late (one-half cycle of Fsc). If 7.8 kHz is low, the start of the VCO write pulse will be initiated by the leading edge of the 1365 pulse. The half-cycle shift of data written into memory will, when read out of memory, provide exact registration of chroma interlace.

9-4 Search Oscillator

As stated previously, the search oscillator circuitry has two RC voltage-controlled oscillators. These oscillators are selected internally (VPR-2B) or externally (VPR-3). The feedback loop and decoding is similar to that used in the normal 6Fsc circuit, but with some significant differences. The counters are the same type—divide-by-13, preset to 3, and divide-by-105, preset to 25. A decode count of 507

TBC-3

provides the search half-line pulse. The decoded count of 1201 provides search flywheel sync, coincident with the leading edge of the horizontal sync. At the count of 507 the K-input of a JK flip/flop is set high. At the count of 1144, Q is clocked high, Q is ANDed with the count of 1201 to produce flywheel sync. A decoded count of 1355 sets the VCO write pulse flip/flop; the following half-line pulse resets it.

At the final count of 1365, the divide-by-105 counter is reset and loaded with a count of 25. Since the clock for divide-by-105 counter is the eight-count of the divide-by-13 counter, after five more counts the carry output resets the divide-by-13 counter and leads it with a count of three. The eight count also provides the search 1.65-MHz signal. The count of 1365 also presets the JK flip/flop which had been clocked by the 1144 count.

A flip/flop is preset by the end of vertical dropout signal and clocked by the next gated sync pulse. This enables a divide-by-14 counter. The carry output 8.5 μ s later resets the divide-by-105 counter.

In search mode, and for phase comparison, the count of 1365 from counter U19/U29/U28 (TP9) is applied through differentiator C131/R98 to form a spike. The spike is inverted by U27-11 and U17-12 and applied to pin 3 of phase comparator U9. The other input to the phase comparator pin 1 is playback gated sync (-) from the Video Input PWA. The sync, inverted by U5-3 and gated through U10-6, inverted by U10-11 and U17-4 is differentiated by C11/R38 to fire one-shot U11-12. The sync from U11-12 is gated through U10-8, inverted by U7-11 and is applied as the second input to phase comparator U9. The comparator operates on the negative-going edges of both signals. The dc signal comparator outputs are fed to dual four-line data selector multiplexer U3 which is used as a digital switch. The RC time constant one-shot U11 causes the oscillators to slow up faster in frequency than they slow down. Both sections of U2 and U8 prevent half-frequency lockup of the VCO.

he output of charge pump U9 pins 5 and 10 is a dc voltage used to charge up or discharge capacitors C18/C20 and C14/C12 in the following two VCO integrator circuits U80-6 and U4-6 that feed up-oscillator U81-7 and-down oscillator U81-10, respectively. Up-frequency one-shot U83-4 and down-frequency one-shot U83-12 provide for noise immunity.

9-5 Horizontal Sync—Video Field

During video field time (line 20 to 262), if in normal operation with color present, the burst crossing signal (pin 25) from the Tape H Comparator is selected to drive circuits associated with H-rate timing. Through a series of delay one-shots, the signal is phased to create a flywheel sync pulse at video H-sync time. The delayed H-pulse is applied to one input of a digital phase comparator. A counter, driven by the 6Fsc oscillator, generates the normal flywheel sync pulse (1201 counts of the 6Fsc oscillator) and a measured interval later generates a counter reset pulse (1365 counts) which is also the other input to the digital phase comparator. The output of the comparator is integrated and applied as an analog dc voltage to a varactor in the 6Fsc oscillator circuit. Thus, an accurate phase relationship between the burst crossing signal and the 6Fsc oscillator is maintained.

The integrated output of the digital phase comparator is also sent to a window voltage comparator. The normal output of the integrator is 4V; the window limits are +4.5V and +2.5V. If the integrator output falls outside these limits, an eight-field delay counter is enabled. The carry output triggers a 1.2s one-shot which provides the search positive (+) and negative (-) signals. The search signal is activated in shuttle operation of the playback mechanism when the incoming H-rate is too high (fast shuttle forward) or too low (fast shuttle reversal).

When the TBC-3 is in search mode the following conditions are established:

- Up or down search oscillator is enabled.
- Field rate input to the 256 vertical delay counter is switched from playback vertical to tape vertical.
- Search half-line used instead of normal half-line to 256 vertical delay, normal VCO write pulse flip-flop, search VCO write flip/flop, and flywheel sync flip/flop.
- Search 1.65 MHz used instead of normal to the frequency discriminator U34-8.
- Search flywheel sync used instead of normal to the flywheel sync one-shot U41-6.
- Search 6Fsc (U25-10) used instead of normal to pin 13.
- Search VCO write pulse (U40-6) used instead of normal to pin 23.
- VCO lock to pin 71 is inhibited.
- Search (-) is gated to pin 72.

The H-sync signal, whether from burst crossing (pin 25) or tape H-sync (pin 60), is delayed approximately 0.6 μ s by the H-reset and qualify-delay one-shot. Q drives the digital phase comparator; Q provides the tape pulse to the qualify H-pulse circuit. The count 1352 of the 6Fsc oscillator (46.65 ns prior to the next predicted delay H-pulse) provides a 586-ns gate to qualify a 104-ns pulse triggered by the H-reset and qualify delay one-shot. If coincidence occurs, a flip/flop will be reset by the qualified H-pulse and clocked set by the VCO comparator range one-shot approximately 31 μ s later. Thus, the VCO comparator is enabled 0.6 μ s before the predicted time of the delayed H-pulse and is inhibited 32 μ s later. This operation is referred to as line-by-line qualification. If coincidence does not occur (not qualified), the phase comparator is not enabled for the succeeding line. The signal used to enable/inhibit the digital phase comparator is gated out to pin 56 as the clamp pulse to the color processor. The qualified H-pulse is also used to trigger a 1.5-ms one-shot which is gated out to pin 71 as VCO lock to the video input. If the H-pulse is not qualified the VCO lock one-shot is inhibited.

9-6 Horizontal Sync—Vertical Blanking Interval

The vertical inhibit signal is reclocked with half line (+), and with the reset qualify signal generated in the vertical delay circuits is used during the vertical blanking interval to inhibit the digital phase comparator (see Figure 9-9, waveform K).

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Thus, during the period when the VTR's playback head enters and leaves the tape, the oscillator will not be skewed by absent or distorted timing signals. In addition, a switch signal beginning with line 2 (start of head switch vertical dropout) and ending at the end of line 9 (trailing edge of playback vertical) replaces burst crossing with tape H-sync to drive the horizontal sync circuits. Vertical inhibit is also gated out to the tape H comparator (pin 24) and to the video input and color processor (pin 55).

9-7 Heterodyne Operation

Sync head process (pin 73) (VPR) and head switch vertical dropout (pin 69) (VPR) are inhibited, therefore end of vertical delay—the trailing edge—clocks one reset qualify pulse.

9-8 Normal Operation—Vertical Delay

If not in search, heterodyne, or slow-motion mode, playback vertical (pin 33) or tape vertical (pin 57) may trigger the 256-count vertical delay circuit. If present, playback vertical is always used. If play vertical is not present, then tape vertical is used (standalone application). If in search mode, tape vertical only is used. If in slow motion (and not search), playback vertical only is used.

At leading edge of playback vertical (or tape vertical) if in normal mode, the 256-count vertical delay is loaded to zero and clocked by half-line (+) pulses. At the 256 count the carry pulse triggers a one-shot which forms the vertical inhibit signals (pin 24 and 55). These outputs are used to inhibit various circuits during the helical scan dropout interval.

9-9 Normal Operation—Reset Qualify

If the sync head is in use, sync head process (pin 73) is low, enabling head switch vertical dropout (leading and trailing edges) and playback vertical (trailing edge) to produce three reset qualify pulses during the vertical blanking interval (see Figure 9-9, waveform C). If the sync head is not in use, sync head process goes high, inhibiting sync-head process gating so that only the trailing edge of the head switch vertical dropout produces a reset qualify pulse. The reset qualify pulse is started as previously described. It may be ended after a 2H delay if a qualified H-pulse is received from the tape H pulse qualify circuits. If no qualified H-pulse is received, the reset qualify pulse will continue for a total of up to 15H, at which time it will be arbitrarily terminated.

The reset qualify signal provides an inhibit of the error control of the normal 6Fsc oscillator and prevents disqualification of the VCO lock signal during the vertical blanking interval. In addition, it provides insurance against a loss of flywheel sync. The flywheel sync generator is enabled at 1/2-line time (507 count). If for any reason the decoded 1201 count does not trip the flywheel sync one-shot, and thereby latch it shut until the next half-line time, 4 μ s later a tape H pulse will be enabled into the OR gate by reset qualify. If that pulse fails, a comp timing (burst crossing) pulse (see Figure 9-9, waveform E) reclocked by 6Fsc and the eight-count of the divide-by-13 counter will be gated into the OR gate. If that one fails, a last attempt will be made by the 1365 count pulse. The reason for providing the

redundant circuits to develop a flywheel sync is that every line of the field must be written into memory in its exact sequence, otherwise the write-read-sequence of memory would be impaired.

9-10 MAINTENANCE

See Figures 9-5 through 9-10 in this section for the simplified schematics, waveforms, test-point, and adjustable component summaries called out in these procedures.

Before undertaking any adjustments to the Tape VCO review the alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-5 for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the Tape VCO and interactive functions between it and other PWAs before making adjustments. Pay particular attention to the Tape H Comparator and Video Input PWAs. Adjustment to or replacement of the Tape VCO PWA may require complementary adjustment to Tape H Comparator PWA 5.

9-11 VCO Frequency and Error Discriminator Alignment

STEP 1 Use tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

STEP 2 Normal mode VCO alignment:

- a. With power off, remove Tape VCO PWA 5. Connect a digital voltmeter to TP1 and ground. With digital voltmeter still connected to TP1, reinsert PWA into frame.
- b. Switch power on and allow a 2-min warmup of TBC.
- c. Verify a $+4 \pm 0.1$ Vdc level at TP1. Adjust L1 (normal 6Fsc oscillator), if necessary, using a nonmetallic tuning tool.

STEP 3 6Fsc oscillator adjustments:

- a. Place VPR in ~~rewind~~ ^{Forward} mode. Adjust R26 (up oscillator control) for minimum hooking at top of picture as observed on TV monitor.
- b. Place VPR in fast ~~forward~~ ^{Rewind} mode. Adjust R19 (down oscillator control) for minimum hooking at top of picture as observed on TV monitor.
- c. Connect oscilloscope to jumper J14 pin A (up oscillator error voltage). Place VPR in rewind mode and adjust C117 (up search oscillator) so that for all rewind speeds error voltage is more than 0.6 Vdc and less than 4.5 Vdc.
- d. Connect oscilloscope to jumper J13 pin A (down oscillator error voltage). Place VPR in fast forward mode and adjust C121 (down search oscillator) so for all fast forward speeds the error voltage is more than 0.6 Vdc and less than 4.5 Vdc.

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STEP 4 Frequency error discriminator calibrations:

- a. With power off, remove PWA and connect a miniature clip lead or solder a wire to connector end of R120 (1K 5% 1/8W resistor—see component locator). This end of resistor is electrically at edge connector pin 79, 80. Connect wire to a digital voltmeter and reinsert PWA into frame. Allow a 2-min warmup of the TBC and then read dc level at connector end of R120. It should be $6.5V \pm 0.05V$.
- b. Adjust L2 (frequency error), if necessary, using nonmetallic tuning tool. It may be necessary to alternately adjust and reinsert PWA more than once to obtain desired reading.

Note

If adjustments are to be made to Tape H PWA, leave clip lead attached for later test.

STEP 5 Tape H reset and qualify delay adjustment:

- a. Connect oscilloscope as follows: CH1—TP1 (VCO dc error). Trigger on PWA pin 57 (tape vertical).
- b. Adjust R45 (tape H reset and qualify delay) through its range and note the presence of vertical rate pulses. Set R45 so that the vertical pulses are at minimum amplitude (nominally 50 mV).
- c. Connect oscilloscope as follows: CH1—TP5 (gated tape H reset). Trigger on PWA pin 25 (Tape H comparator timing).
- d. Adjust R50 (VCO phase comparator range) for a 50% duty cycle. Waveform 4(B) shows a typical adjustment. The 50% duty cycle sets up a symmetry for the error signal at TP1 for clipping on both positive and negative peaks.

STEP 6 Go to PWA-level Tape H Comparator adjustment section and verify normal operation of burst/sync phasing (paragraph 8-7).

9-12 Vertical Delay

Vertical delay control establishes vertical inhibit timing of format dropout and is used for heterodyne or other VTRs without a sync head. It may be adjusted any time, but should be done before line velocity compensation adjustment.

- STEP 1 Use tape/reference test loop setup with a 75% color-bar signal to TAPE VIDEO IN.**
- STEP 2 Connect oscilloscope: CH1—TP10 (vertical inhibit); CH2—PWA 2 TP1. Trigger from CH1.**
- STEP 3 Adjust R88 (vertical delay) so that trailing edge of inhibit ends after rf recovery and one line prior to active video. Waveform 25(Y) shows a typical setting at line 16 for a VPR without a sync head. For VPRs with a sync head inhibit is coincident with start of line 10.**

9-13 Shuttle Mode Verification with the VPR

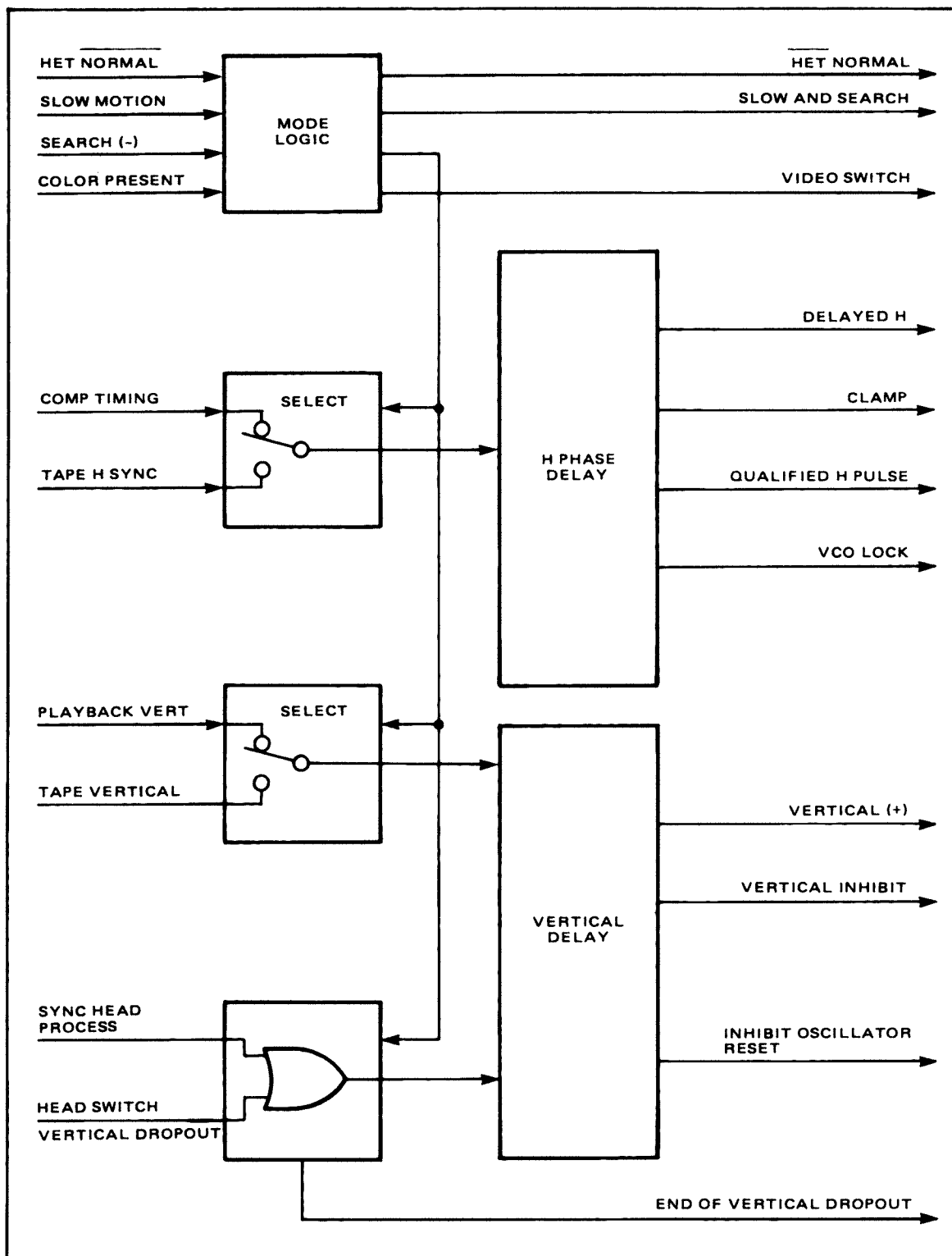
This verification requires normal VPR/TBC configuration with both units fully operational and properly phased to system reference (RS170A sync/burst phase or facility standard reference).

- STEP 1 Make a 10-minute color-bar recording.
- STEP 2 With power off extend tape VCO.
- STEP 3 Connect an oscilloscope to pin 30 (gated sync). Trigger on internal.
- STEP 4 Set VPR TAPE/EE switch to TAPE.

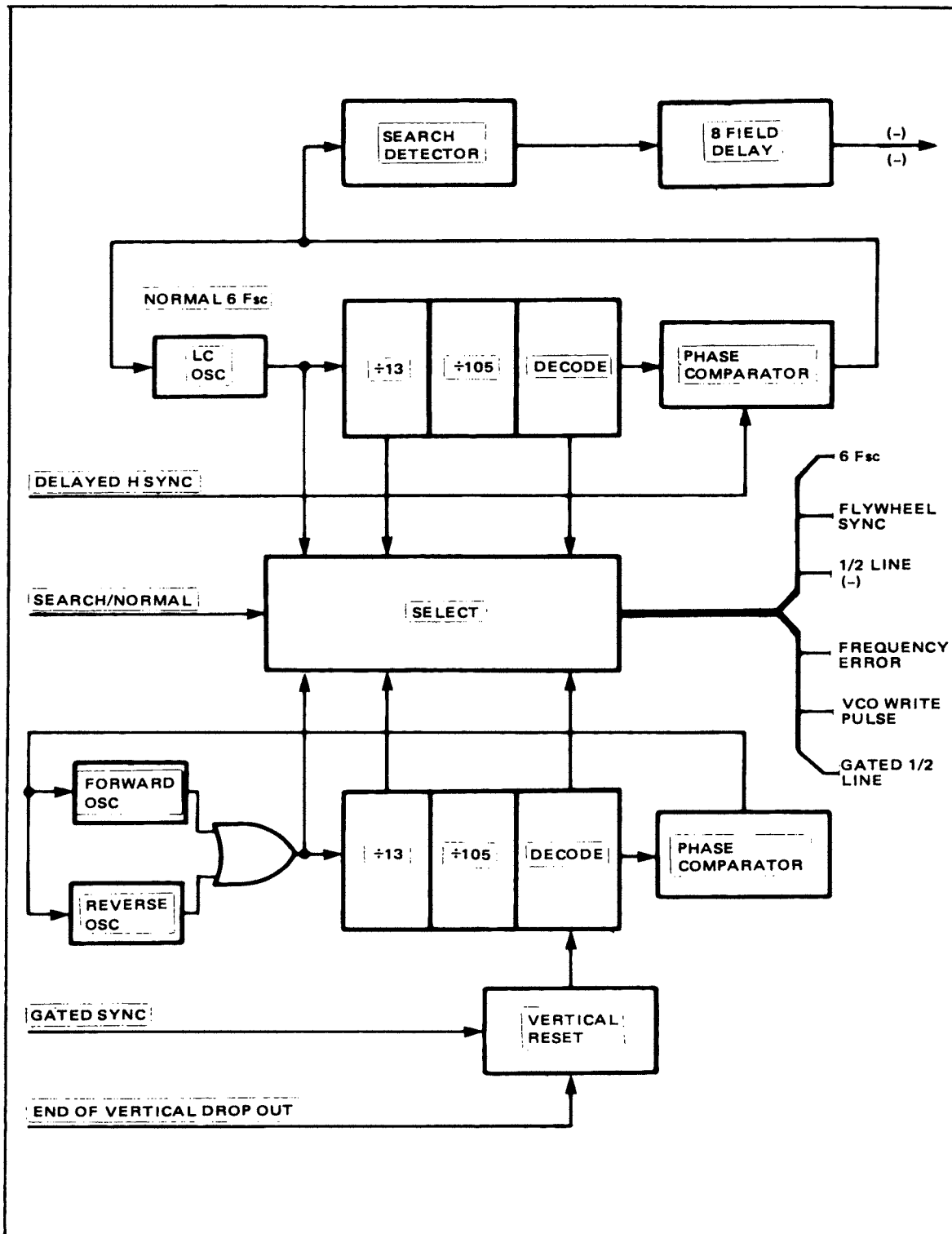
Note

If VPR has a sync head perform steps 5—9 below for sync head both on and off.

- STEP 5 Shuttle recording (rewind) and verify a stable monochrome picture with normal, random narrow black streaks across it.
- STEP 6 Verify that SEARCH indicator (PWA edge, red LED) is on.
- STEP 7 Verify that a stable monochrome picture still exists when period of gated sync is 93 μ s.
- STEP 8 Shuttle recording forward. Verify stable monochrome picture with black streaks and that SEARCH indicator is on.
- STEP 9 Verify stable picture for a gated sync period of 43 μ s.
- STEP 10 With power off return PWA to cage.



**Figure 9-1. Horizontal and Vertical Input Delay Circuits
Simplified Block Diagram, Tape VCO PWA 5**



**Figure 9-2. Normal and Search Oscillator Circuits
Simplified Block Diagram, Tape VCO PWA 5**

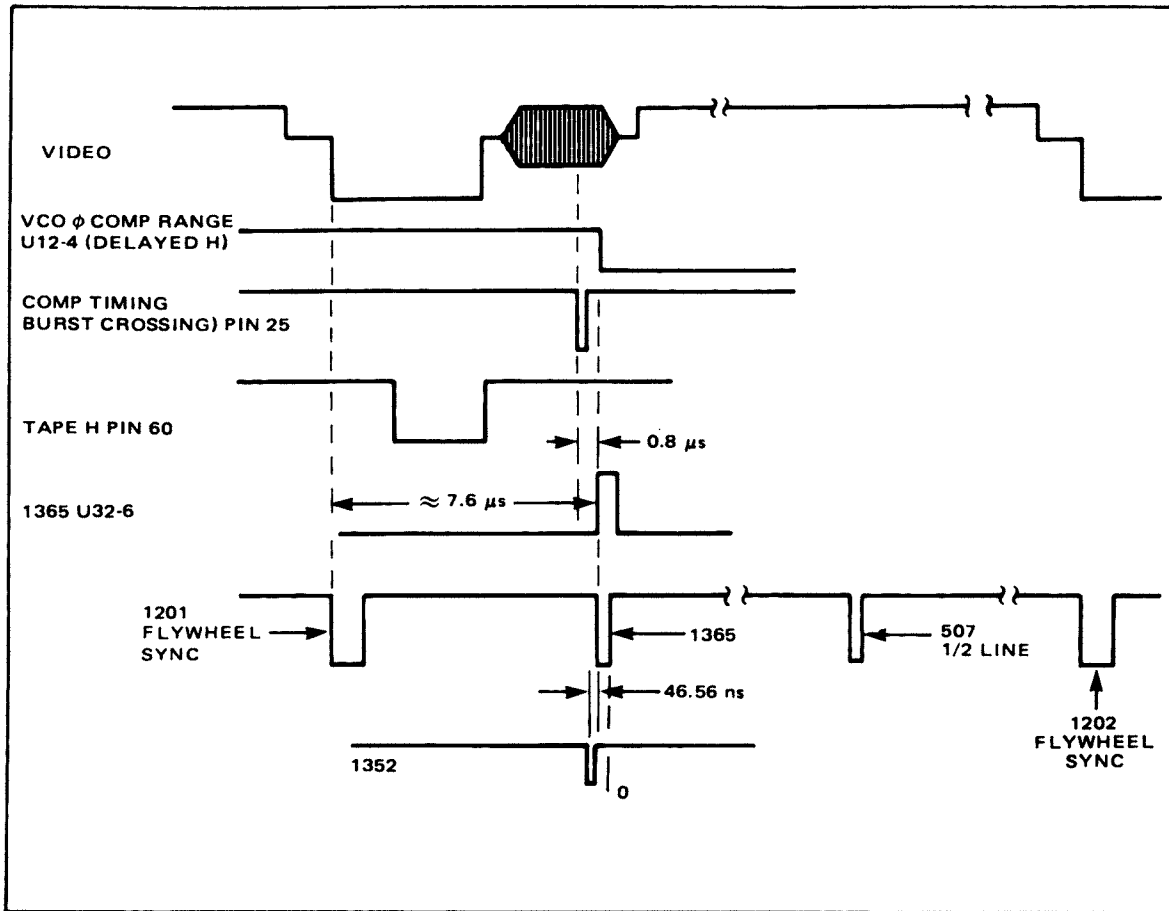


Figure 9-3. Counter Decode Timing Relationship, Tape VCO PWA 5

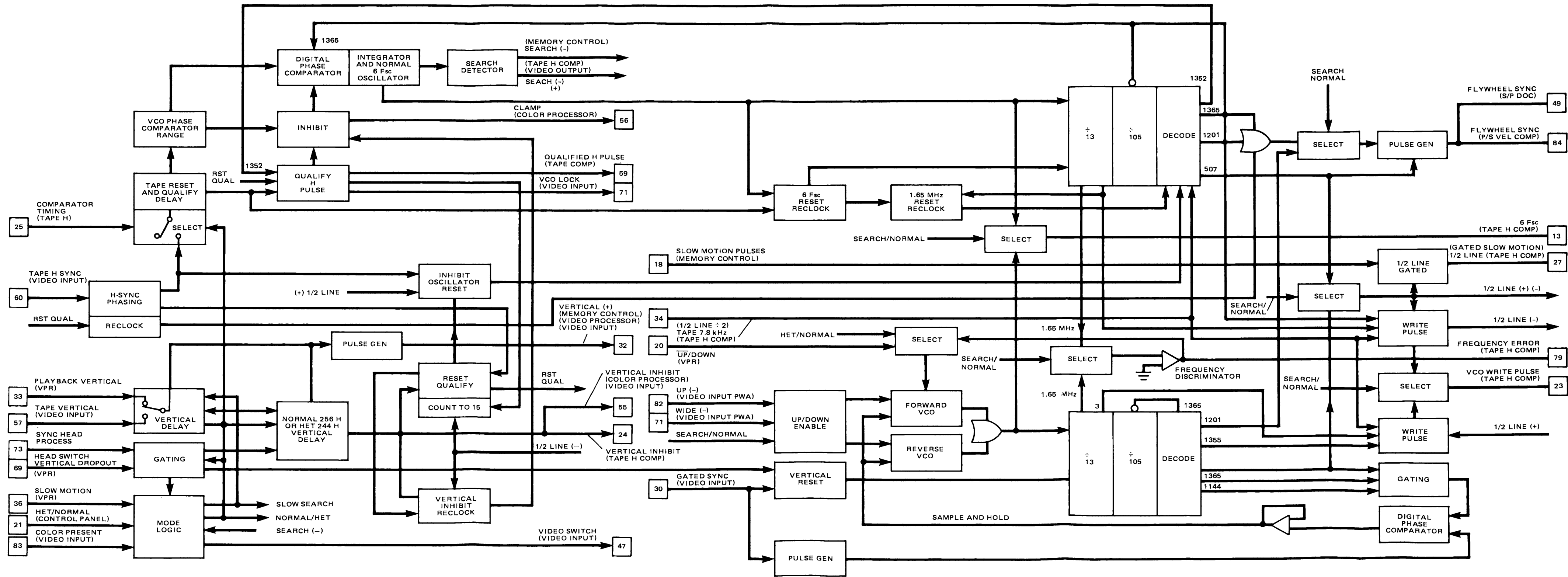


Figure 9-4.
Tape VCO PWA 5 Block Diagram

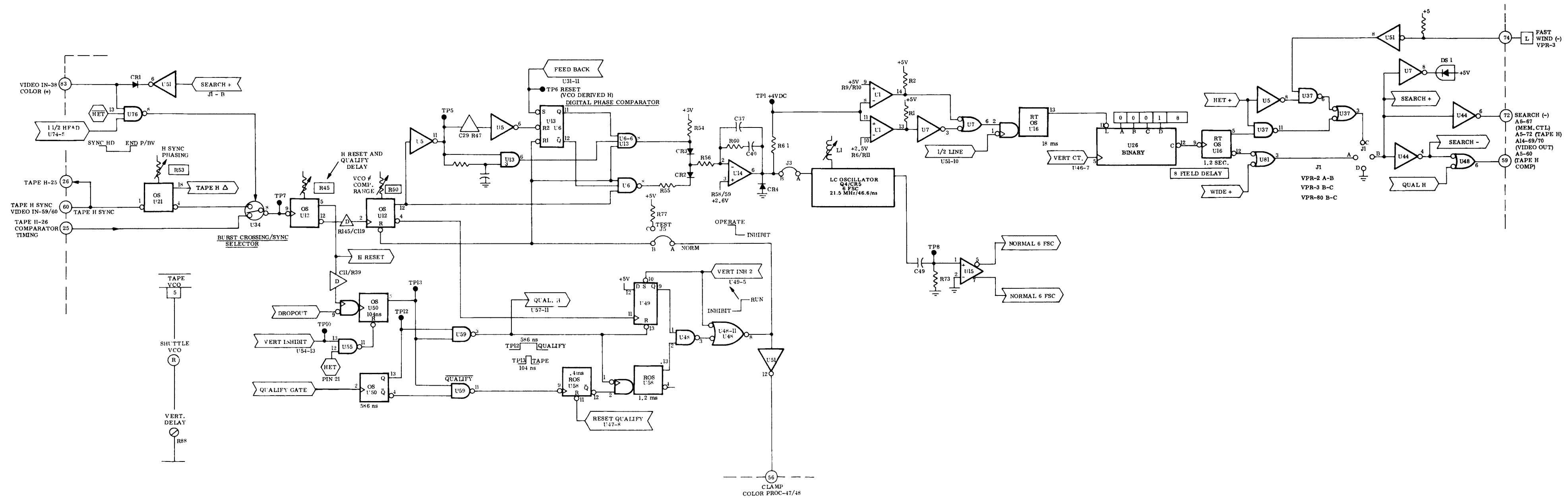


Figure 9-5.
Normal Speed VCO Simplified Schematic,
Tape VCO PWA 5

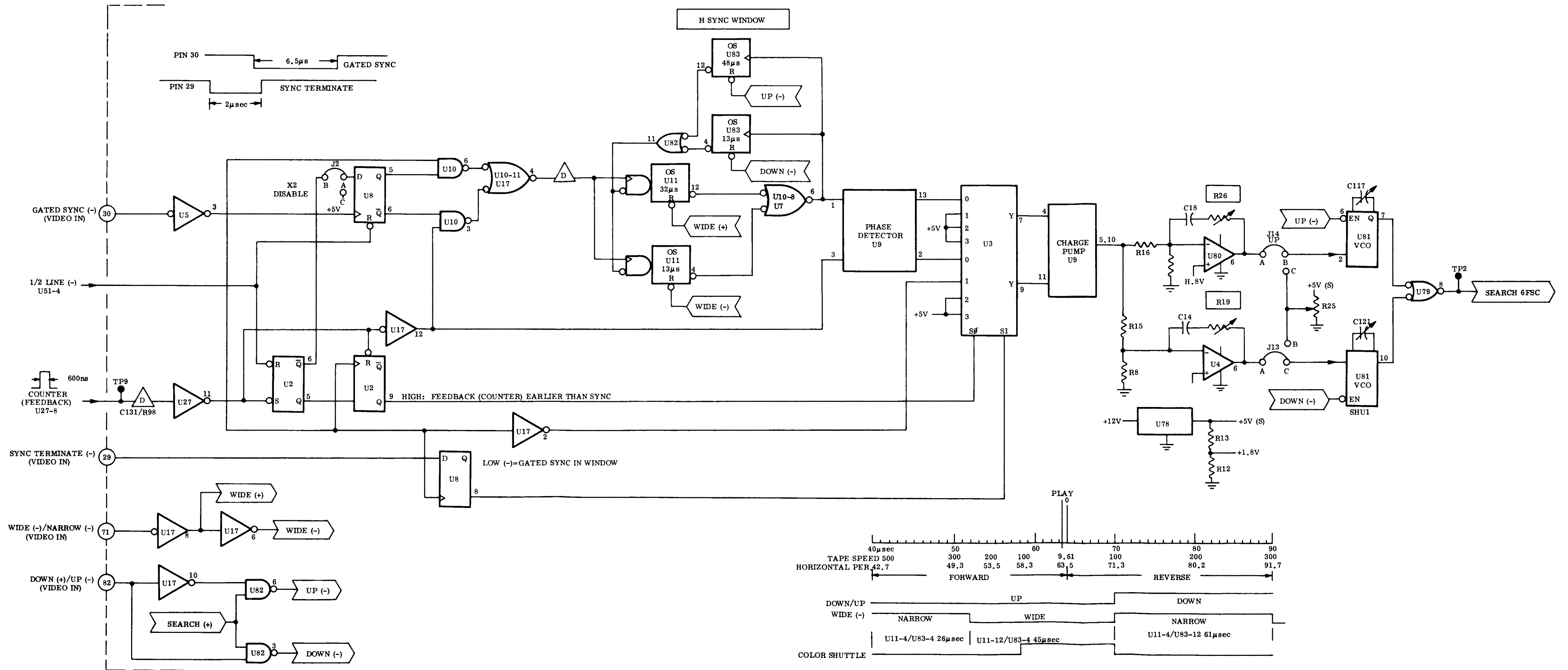


Figure 9-6.
Shuttle Speed VCO Simplified Schematic,
Tape VCO PWA 5

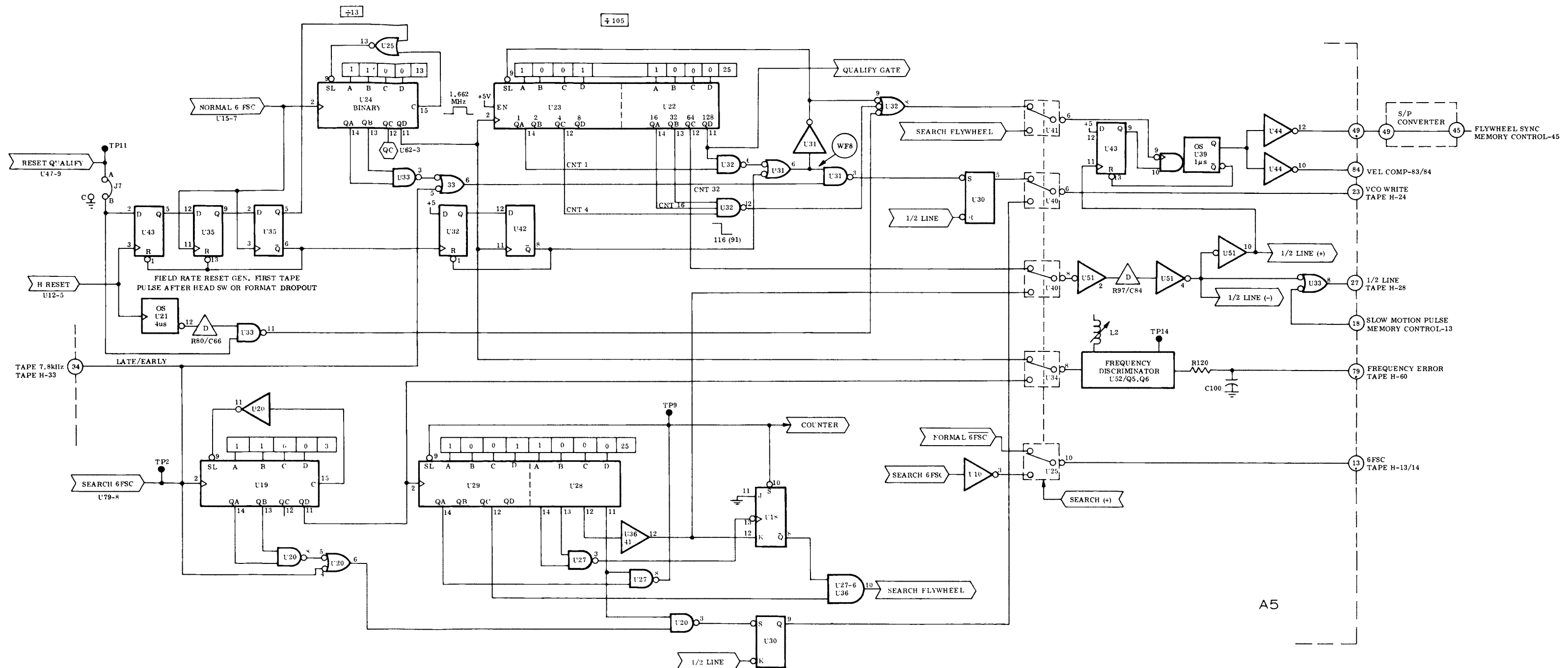


Figure 9-7.
6Fsc Counters Simplified Schematic,
Tape VCO PWA 5

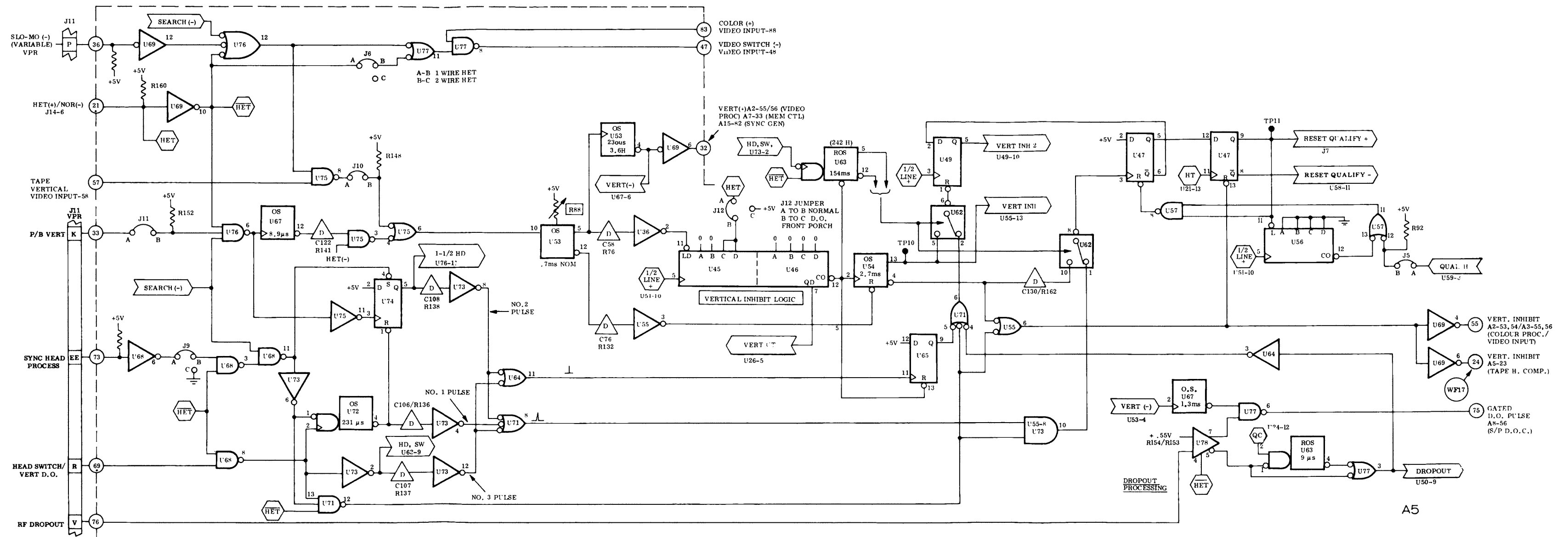


Figure 9-8.
Vertical and Dropout Logic Simplified Schematic,
Tape VCO PWA 5

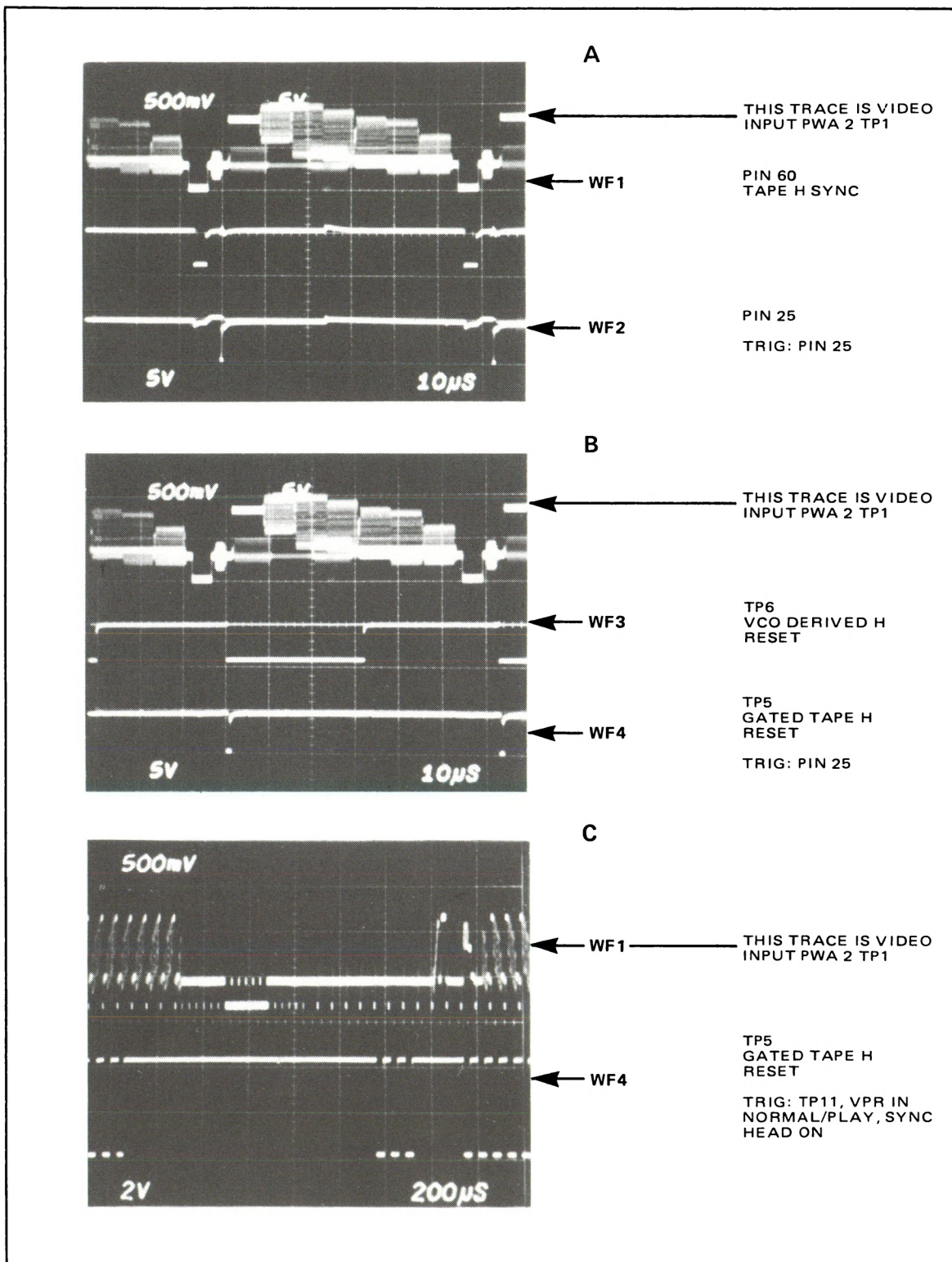


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 1 of 7)

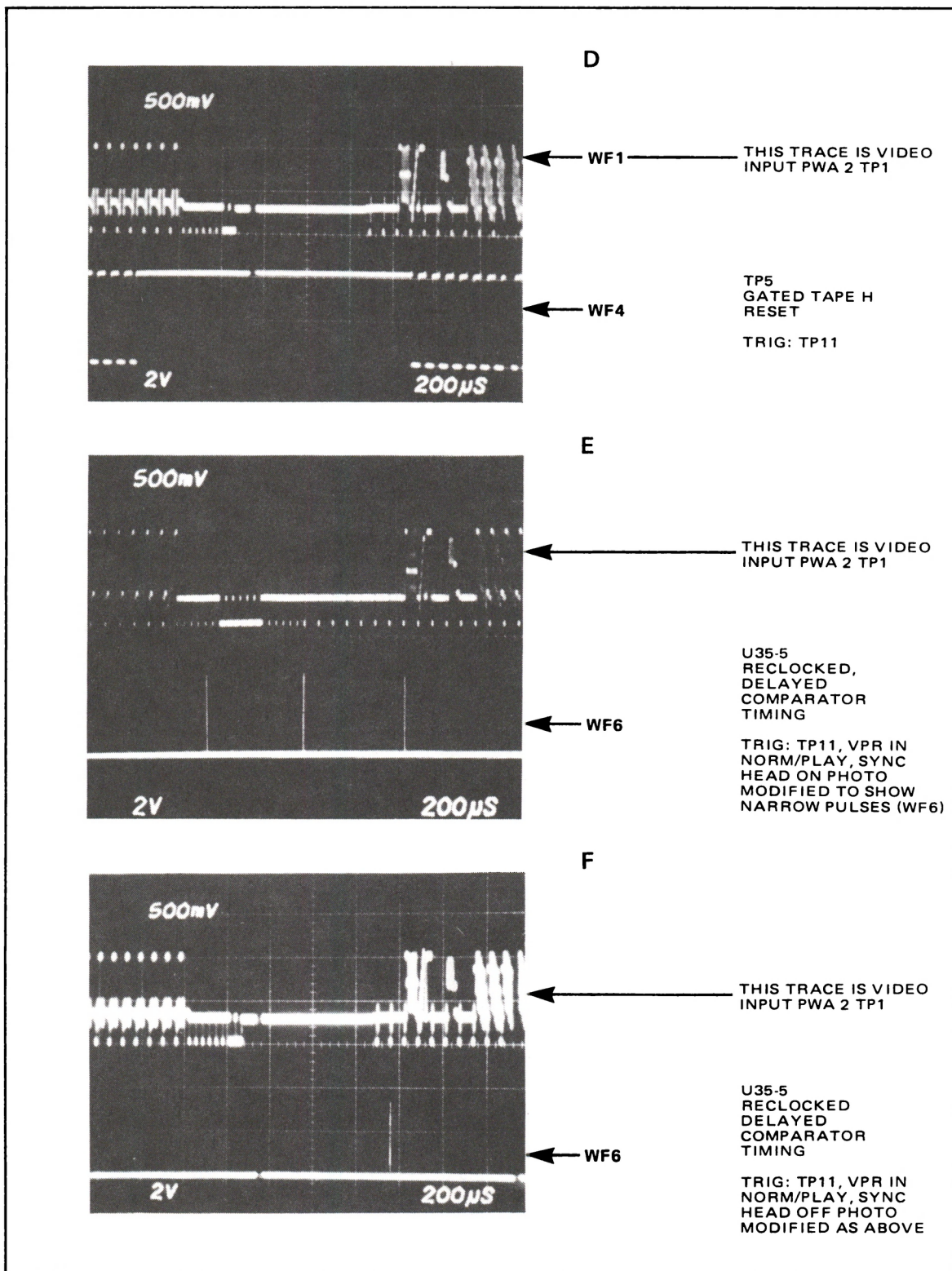


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 2 of 7)

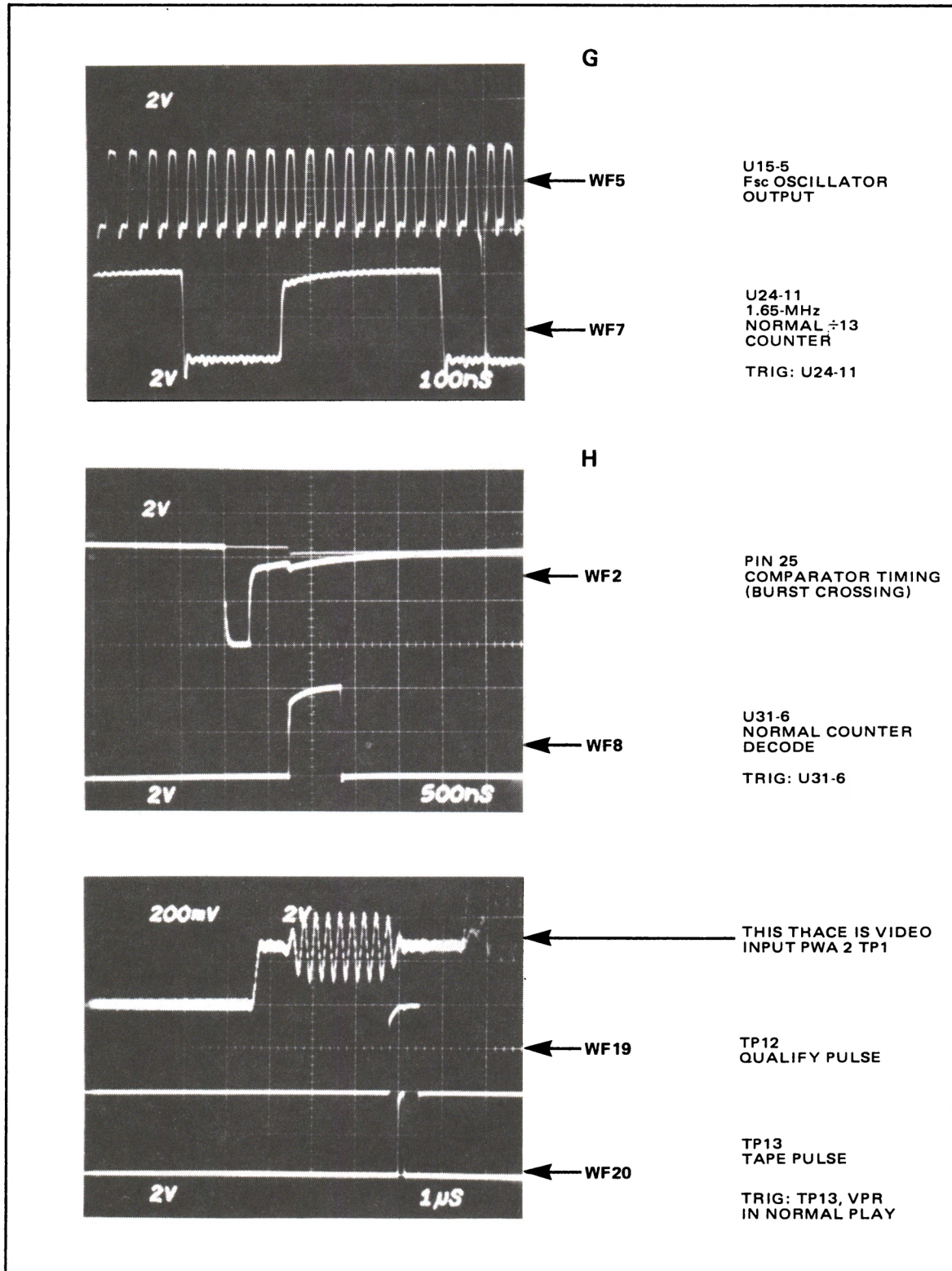


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 3 of 7)

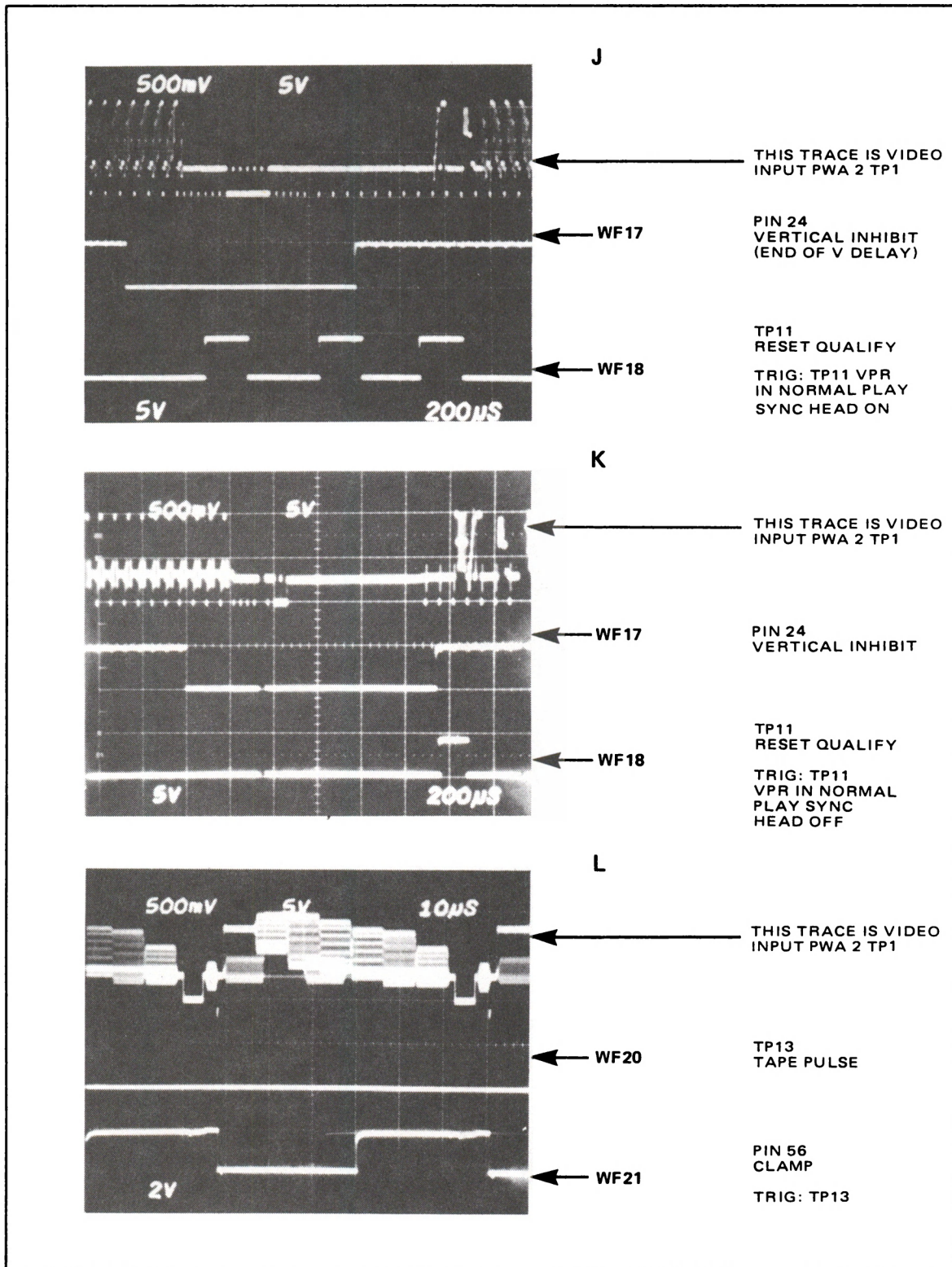


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 4 of 7)

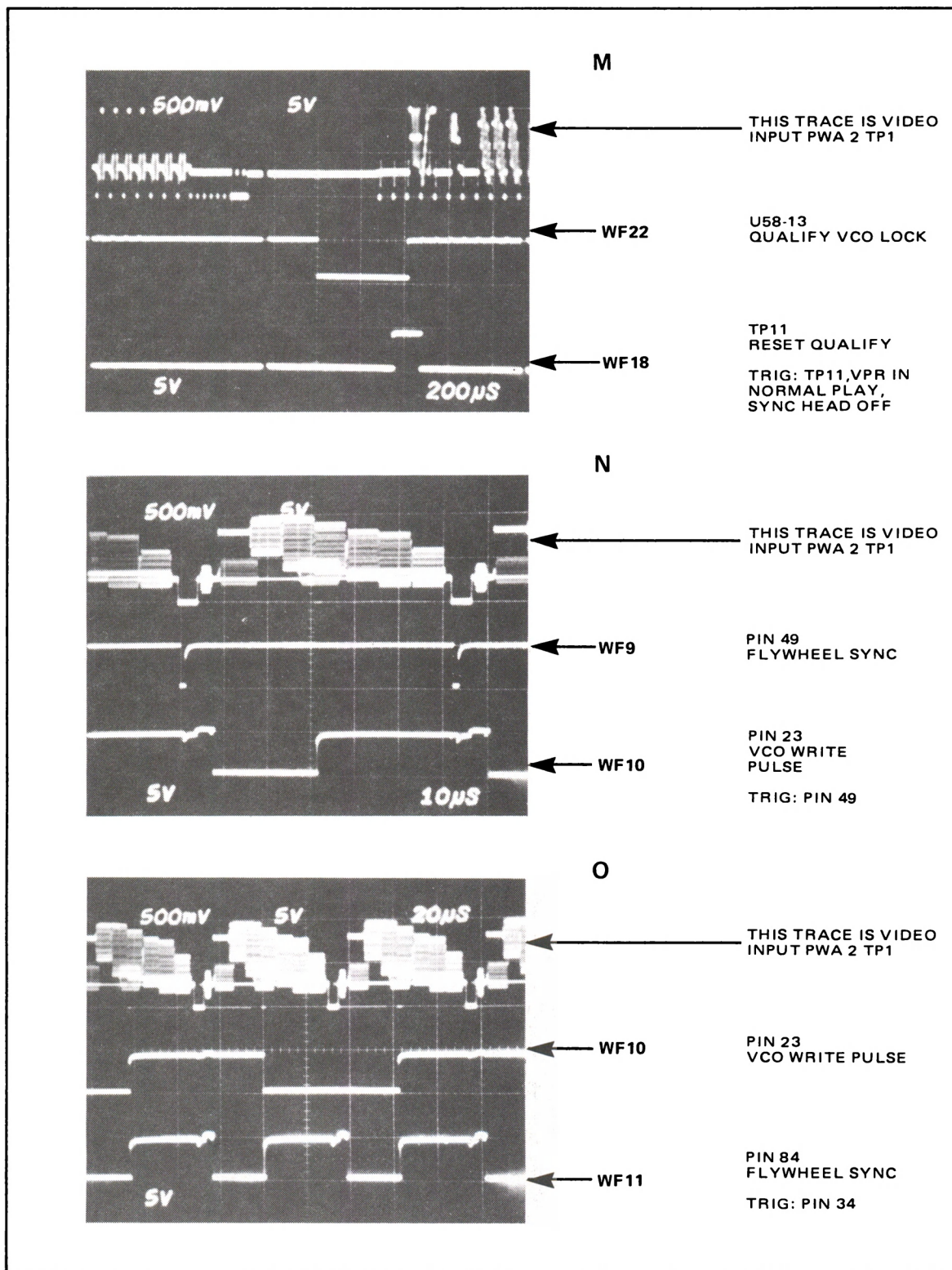


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 5 of 7)

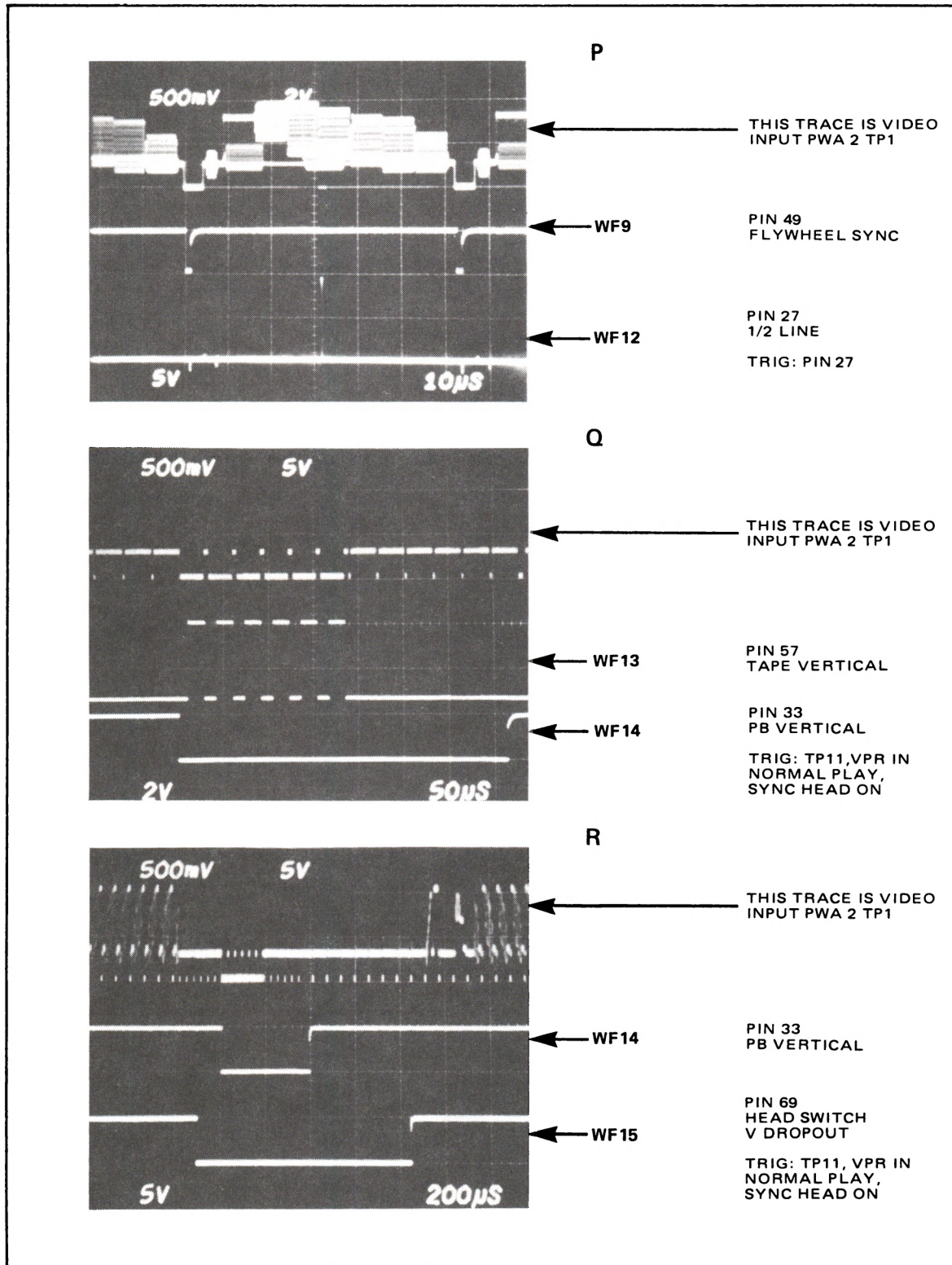


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 6 of 7)

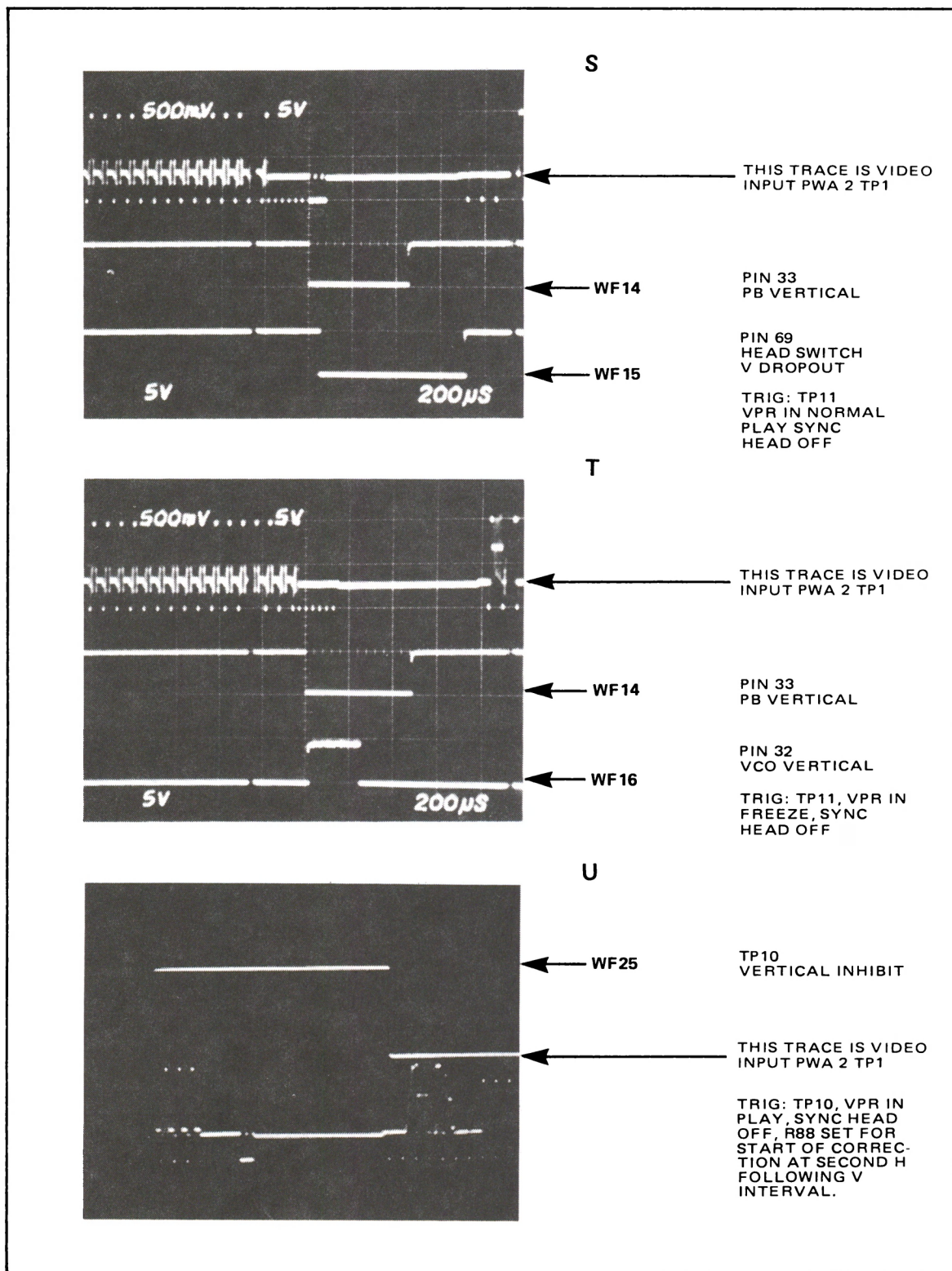


Figure 9-9. Tape VCO PWA 5 Waveforms (Sheet 7 of 7)

PWA 5 Jumpers

Jumper	Position	Function
J1	A-B	Normal/Search
	B-C	Internal Search (VPR-2B)
	B-C	External Search (VPR-3)
	B-D	Forces normal oscillator (test)
J2	B-C	Counter Disable
	A-B	Normal
	A-B	x2 disable
J3	A-B	VCO Test
	A-B	Normal
	Removed	Removes error to oscillator
J5	A-B	Factory Test
	A-B	Normal
	B-C	Test
J6	A-B	Two-Wire/Single Wire
	A-B	Single-wire heterodyne operation
	B-C	Two-wire heterodyne operation
J7	A-B	Factory Test
	A-B	Normal
	B-C	Test-defeats H-reset
J8	A-B	Factory Test
	A-B	Normal
	Removed	Test-verifies reset qualify counter
J9	A-B	Sync Head Video Processing
	A-B	Normal
	B-C	Disabled
J10	A-B	Factory Test
	A-B	Normal
	Removed	Disables tape vertical-to-vertical display
J11	A-B	Factory Test
	A-B	Normal
	Removed	Disables VTR vertical-to-vertical delay
J12	A-B	VTR Type Select
	A-B	Normal; vertical dropout
	B-C	Front porch vertical dropout
J13	A-B	Down Search VCO
	A-B	Normal
	B-C	Test
J14	A-B	Up Search VCO
	A-B	Normal
	B-C	Test

PWA 5 Test Points

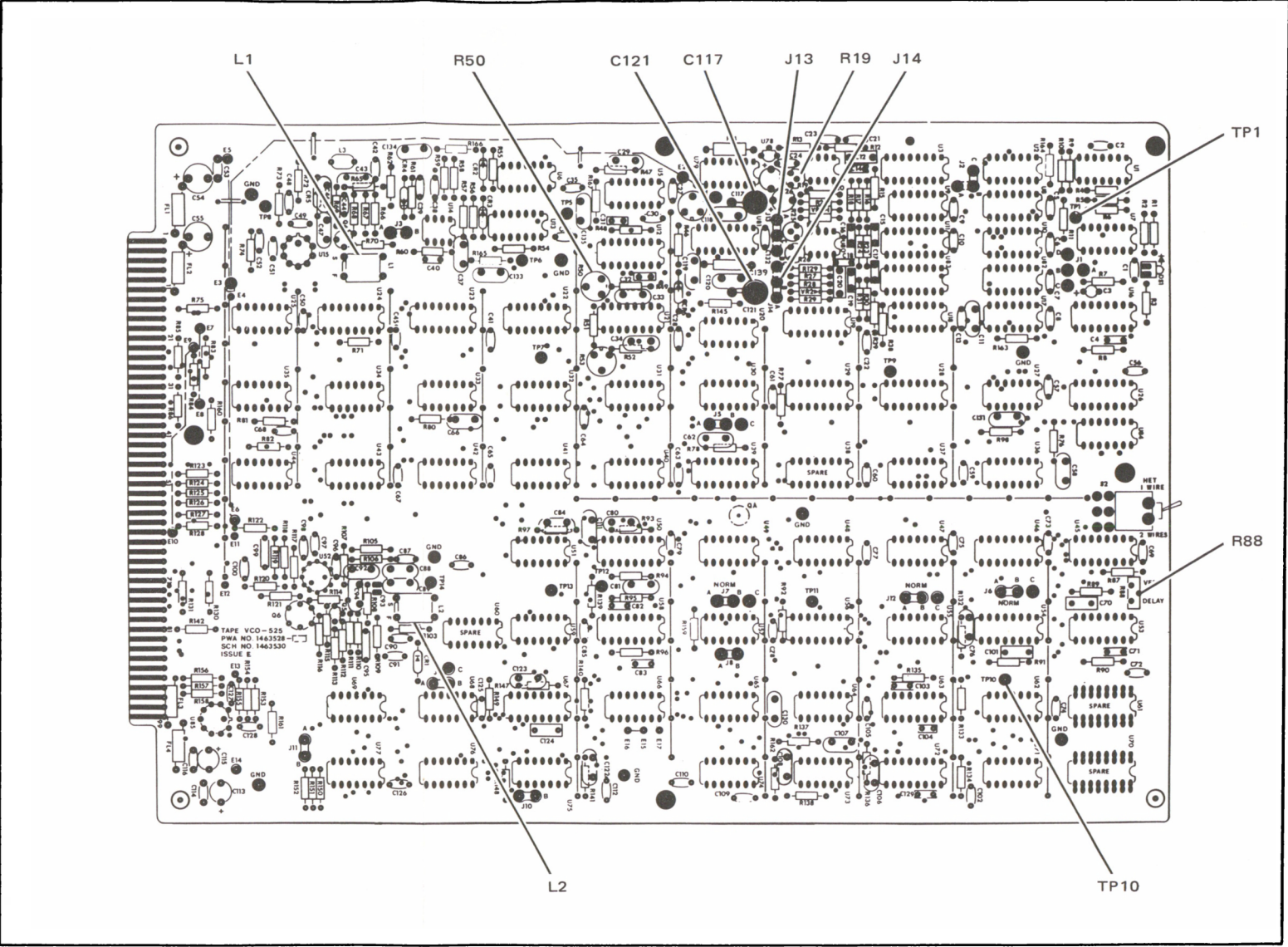
Test Point	Function
TP1	+ 4V VCO error voltage
TP2	Search oscillator output
TP5	Gated tape H reset
TP6	H-rate reset
TP7	Tape H
TP8	6-Fsc normal oscillator
TP9	Search reset-1365
TP10	Vertical inhibit
TP11	Vertical reset qualify
TP12	Qualified gate timing pulse
TP13	Tape pulse
TP14	1/2 subcarrier oscillator

PWA 5 Adjustable Components

Component	Function
C117	Up search oscillator
C121	Down search oscillator
L1	Normal 6-Fsc oscillator
L2	Frequency error
R19	Down oscillator control
R21*	Search oscillator test
R26	Up oscillator control
R45	Tape-H reset and qualify delay
R50**	VCO phase comparator range
R88	Vertical delay
R143*	Down VCO range
C20*	Up VCO trim

* Factory adjust only.

** R50 is adjusted for a 50% duty cycle at U12-13 with a 10-12V random error input (an active factor only when VCO is accessing new video).



PWA 5 Component Locator

Figure 9-10.
Test Points, Jumpers, Adjustable Components,
Component Locator, Tape VCO PWA 5

PART II

SECTION 10

MEMORY CONTROL PWA 6

DESCRIPTION AND MAINTENANCE

10-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463556 (12-line), 1463537 (16-line)
Schematic No. 1409096 (12-line), 1463539 (16-line)

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 10-3, overall block diagram
- Figures 10-4 to 10-13, simplified schematics
- Figure 10-14, waveforms
- Figure 10-15, maintenance data

Memory Control PWA 6 function summary:

- Write control is synchronous to tape 3.58-MHz timing and provides:
 - a. Memory board address and line select addressing for main memory and velocity compensator line error store.
 - b. Separate two-phase write clocks for main and dropout memory.
 - c. Three phases of 10.7 MHz for 8-to-24-bit serial-to-parallel conversion on PWA 7
- Read control is synchronous to reference video 3.58-MHz clock (modulated by velocity compensator) and provides:
 - a. Memory board address and line select addresses for main memory and velocity compensator line error store.
 - b. Two-phase memory read clocks (modulated by velocity compensator).
 - c. Three phases of 10.7 MHz for 24-to-8-bit parallel-to-serial conversion on PWA 13.
 - d. Reference 10.7-MHz clock for D/A conversion on PWA 14.
- Memory centering and overload logic maintain the relationship of read-to-write addressing within the center of the correction range.
 - a. A write overload condition (tape slow compared to reference) enables the dual load which advances write address two lines and simultaneously loads the skipped line (resulting in two lines of video repeated).

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- b. A read overload condition (tape fast compared to reference) inhibits the write address counter from incrementing for two lines and inhibits writing for two lines (two lines of video are dropped).

10-2 DESCRIPTION

Note

This discussion pertains to the 12 and 16-line version of the Memory Control PWAs. Where there are differences, information pertaining to the 16-line version is immediately shown in parenthesis.

Memory Control PWA 6 generates control signals that regulate the flow of digitized video through the TBC. Write control signals are clocked by $3F_{sc}$ (10.7 MHz) which is phase-locked to the tape burst crossing and the leading edge of tape H sync. As illustrated in Figure 10-1, the write function is initiated by the write pulse, from the Tape H Comparator PWA, which occurs just after the color burst on the back porch of horizontal blanking. Read control signals are clocked by reference H-drive from the Sync Generator PWA, which is in phase with the reference F_{sc} . Because these signals are timed to broadcast standards, digitized video read out of memory will be time-base corrected for any errors due to the tape or the playback process.

Memory Control PWA 6 is divided into three general circuit areas: write timing, read timing, and line and field registration, as shown on the memory control block diagram, Figure 10-3.

As illustrated in Figure 10-1, the data flow block diagram, memory control may be regarded as the center of a control system that moves digitized 8-bit data representing input video from the A/D Converter PWA at $3F_{sc}$ rate into the Serial/Parallel Converter PWA. There it is assembled in a 24-bit register and shifted at F_{sc} rate into the memory. As data is written into a given line of memory, a previously written line is read out at reference F_{sc} rate into the Parallel/Serial Converter PWA. There it is latched and read out to the Video Output PWA at reference $3F_{sc}$ rate. During the process of moving data from Memory to the Video Output PWA, the Sync Generator PWA further refines time-base correction by providing a modulating reference $3F_{sc}$ to correct for errors introduced by the tape head crossing the vertical dropout gap.

Line and field registration circuits perform three primary functions:

- To servo the relationship between the line being written into memory at a given time and the line being read out of memory to a six-line difference (eight-line difference). That is, read-line 1 paired with write-line 6 (write-line 8). (See Figure 10-2.)
- To servo the video frame into registration with the top of the television screen, while maintaining the six-line (eight-line) read/write difference; the vertical centering function can be selected by a switch at the front edge of the Memory Control PWA.
- To allow the picture display on the monitor during shuttle operation of the playback mechanism by use of search mode.

10-3 Write Timing

Write timing circuits perform two primary functions:

- Timing of data from the A/D converter into the serial-to-parallel converter.
- Timing of data from the serial-to-parallel converter into memory.

They also provide signals for the slow-motion function during editing, and a signal to invert the phase of the chroma at the frame/2 (color frame) rate. Write timing may be modified by vertical centering of the field, memory centering of data in storage, and correction required during editing.

Write-pulse reclocking flip/flops serve to ensure that the 3Fsc pulse that clocks the serial-to-parallel shift register, write shift pulse clock, and reset counters, is synchronous with the write pulse. The reclocked write pulse initiates action in these circuits at the start of the data line by presetting serial-to-parallel shift registers to WCB3. The next 3Fsc pulse shifts the circuit to WCB1; reset counters are enabled and write shift clock pulses are initiated.

10-4 Memory Write Control

The principal clock for the line address counters (WA0, WA1) is the delayed flywheel sync. See Figures 10-3, 10-5, and 10-14 (waveforms O, P, Q). WA0 and WA1, with the appropriate board select signal WMA, WMB, WMC, (WMD), will enable the write gates of each of 12 (16) lines of memory in sequence. WA1 is also used as the clock for the shift register which generates the WMA, WMB, WMC (WMD) intervals. W01 and W02 are two phase clock pulses used by the memory to shift data into storage at the tape Fsc rate. Write clock reset is used by the Memory PWA to reset the write shift enable latch at the end of each line of data. Reset counters are started by the delayed write pulse at the end of the horizontal blanking period. At this time the WM board select output gates are enabled. The reset counters permit 199 words of data to be entered into a given line of memory. At the end of this event the output gates are inhibited, thus closing the write gates in memory. Shift pulses continue to a count of 255, resulting in a shift of 55 words of zero value bits into the memory line behind the data. A total of 254 shifts have been made. The memory line is 256 words in length, therefore the two forward registers at the output end are also zero-value words. Since all memory lines on a given board are wire-ORed at the outputs, the two extra zero-value words serve to prevent mixing of data from two or more lines.

10-5 Serial-to-Parallel Converter Write Control

The serial-to-parallel shift registers generate the WCB1, WCB2, and WCB3 intervals. See Figure 10-3, waveforms L and M. This signal controls the loading of data into Serial/Parallel Converter PWA 7 in 8-bit groups (luminance video level sample) and transfers them into a 24-bit word in the output latch. For dropout compensation, control signals WMA, WMB, WMC-WA0, WA1-DCΦ1, DCΦ2—and terminate clock are used.

10-6 Read Timing

Reference subcarrier (chroma phase component) from the sync generator is the source of read timing. Velocity-compensated read Fsc at pin 82 from PWA 13

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becomes the basic source timing for memory read, P/S conversion, and the D/A conversion on the Video Output PWA. This read Fsc is a 3.58-MHz pulse train which varies in phase as a function of the velocity line error. Reference H drive at pin 72, which is the source for the read stop/start timing for each line in memory, is reclocked by read Fsc to establish the registration of the left picture edge. The read start of the picture data is adjusted in 140-ns increments by the horizontal phasing digital switch on the Memory Control PWA edge. The read timing can be followed on the simplified schematic of Figure 10-4 (12-line) or Figure 10-9 (16-line) and the read control waveforms of Figure 10-14, A-K.

10-7 P/S Converter Read Timing

Velocity compensator circuits on PWA 13 require the same line-by-line read timing as the memories so that the read Fsc output of PWA 13 is synchronous with the line being read out of memory. The clock circuits reclock the delayed H-phase pulse to synchronize with the 3-Fsc rate. The reclocked pulse resets the parallel-to-serial shift register to RCB3 and enables the 224-bit counter. The next WCB1 signal triggers the pulse generator starting the count and the R ϕ 1, R ϕ 2 shift pulse clock. After 224 read shift pulses, the carry output of the counter resets the enable flip/flop and the circuits wait for the next reference H-drive pulse. RCB1 and RCB2 operate the 24-bit latch and multiplexer of Parallel/Serial Converter PWA 13.

10-8 Memory Read Control

Line address counters are reset by the 7.8-kHz reference V/2 color frame one-shot and clocked by H-drive to develop RA0. RA1 clocks the RM board select shift registers. R ϕ 1 and R ϕ 2 shift data from the memory to the Parallel/Serial Converter. RMC, RA1 and RA0 are also used by the velocity compensator in the Parallel/Serial Converter PWA.

The reference 7.8 kHz is the D-input to the color frame rate counter. Reference V/2, which occurs at video frame rate, clocks the counter at the end of the first sequence of F/4 counts. A pulse is generated which presets the line address counter to line 3 and the RM board select shift register to RMA. At 2,100 lines or four frames later, the pulse at TP3 is repeated. Since the 12 lines of memory are evenly divisible into 2,100, all pulses after the first one should find the preset condition already present. F/4 and F/2 with ADV V/2 are sent to the line and field registration circuitry to generate vertical strobe.

10-9 Write/Read Registration Decode

See Figures 10-7 and 10-8 (12-line) or Figures 10-12 and 10-13 (16-line) for simplified schematics and waveform callouts for the memory centering circuitry. The write/read registration decode is used in two modes, search and centering. In the vertical centering or memory centering mode, search inhibits the read/address to the multiplexers. The multiplexer then becomes a write address decode. The clock signal from the latch clock generator, although encoded with RA1-RMC, actually occurs at the beginning of RA1-RMA (line 1) due to calculated delays in the delayed flywheel sync. Thus, whatever line of memory is being written into at that time will be latched for 12 (16) lines of operation. The latched write address is

decoded to the specific line in the two-line to four-line multiplexers U14/U27. The 1 line of 12 (16) selected will go low and the appropriate LED will light up. The green LED, DS7 (DS8), is the target light of the system. Illumination of a red light is an indication of a read/write registration error, which causes the registration error decode to advance or retard the write clock plus-or-minus two lines to bring the system back into registration.

10-10 Registration Error Decode

Lines 1-5 (1-7) and 7-12 (9-16) of the write/read registration decode are inputs to the error decode gates. Lines 1, 2 OR lines 11, 12 (line 1 OR 16) will, if one goes low, preset the error delay counter to 14 and only one pulse will be required for the carry signal to clock the error signal from the error decode gates into the appropriate sample-and-hold JK flip/flop. Lines 1-5 (1-7) are decoded as an error signal to the read digital sample-and-hold flip/flop U5-9. Lines 7-12 (9-16) are decoded as an error signal to the write sample-and-hold flip/flop U5-5. However, if the error is confined to the 2-4 and 8-11 (2-6 and 10-14) line area, the counter will not be preloaded and the counter must count to 15 or 60 lines before the error is clocked into the sample-and-hold flip/flop.

The decode clock produces a signal which is in phase with, but approximately 1 μ s in advance of WA1. When ADV WA1 goes high (end of line 2), the clock is advanced. When the carry is generated, the error is clocked into the sample-and-hold flip/flop. When ADV WA1 goes low, a 1.5- μ s delay triggers the appropriate one-shot to produce either a plus-two-line signal or a minus-four-line signal and a plus-two-line signal. Lines 1, 2, 3, and 4 from the registration decode are designated as read error signals and will produce a plus-two-line pulse (advance two lines) and a dual load. Dual load will load identical data into lines 3 and 1, and lines 4 and 2 (or two lines of memory in the 16-line system). Lines 8-12 (9-16) are designated as write-error signals and will produce a minus four-line signal and a plus-two-line signal (retard two lines).

When the plus-two-line pulse is generated, WA1 is preset to the lines 3 and 4 condition. Thus, lines 1 and 2 of the sequence following the advance two-lines signal are deleted, and the empty lines 1 and 2 are written with pseudo video contents of lines 3 and 4 by the dual load to provide two lines of video.

When the minus-four-line pulse is generated, the WA1 clock to the Memory PWA select shift register is blocked, holding the shift register in its mode of the moment. The plus-two-line pulse operates as previously described, with a resultant retard of two lines. This could be regarded as an instruction to "rewrite lines 3 and 4 with current data."

If the tape H rate is such that the write address sampled by the registration decode latch falls within the read error area lines 1-5 (2-7), a plus-two pulse and dual load is generated to advance the write address toward a six-line (eight-line) read/write address difference. Because the write address is sampled at read line 1 address time, the target of the write address is write address 6 (8). After 12 (16) successive lines of memory read, the write address is sampled again, and if error is found, the write address is advanced two more lines. This process continues until the write address falls within the write 5, 6, or 7 (7, 8, or 9) address area.

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If the write address falls within the write error area lines 8-12 (10-15) the minus-four and plus-two pulses will retard the write address two lines. This action will continue, in 12 (16) memory read line intervals, until the write address falls within the write 5, 6, or 7 (7, 8, or 9) address area. The write/read registration decode, registration error decode, latch clock generator, and write address circuitry comprise a digital servo system.

10-11 Vertical Strobe Generator

At the start of every fourth frame the read address is preset to line 3-RMA. If a six-line read/write address difference is maintained, the write address is line 8 (line 4-RMB). Tape vertical sync is offset in respect to the start of the vertical interval so that at the 10th line (start of the back porch of the vertical interval) the address is read line 1, write line 6. The function of the vertical strobe generator is to enforce this condition, and thereby align the top edge of the picture on the screen.

If the vertical/memory centering switch is in the vertical position, the vertical strobe generator is enabled. While the counter in the strobe generator circuitry is counting (4.9 ms) the latch clock generator is disabled.

In the eighth field of the F/4 signal, F/2, F/4, and ADV V/2 are ANDed to preset a JK flip/flop and \bar{Q} goes low. The first flywheel sync pulse at tape vertical clocks the JK and \bar{Q} goes high. Since the preset was made by a combination of signals from reference V/2 and reference 7.8 kHz, and the reset was established by signals from the tape, the width of the pulse at \bar{Q} is a measure of the phase difference between the two vertical rates. When \bar{Q} goes high the counter is enabled and is clocked by flywheel sync. After 13 counts the 64-bit is high and remains for 64 more counts (total 77). After the 77 count the carry pulse locks the vertical strobe circuits until another F/4-field VIII pulse presets the JK to start the process again.

The leading edge of the vertical strobe clocks the latch of the write/read registration decode. The latched write address is held for the duration of the vertical strobe. If an error is decoded the write address is servoed toward the line 5, 6, 7 area. When a line 5 or 7 error is decoded, a secondary circuit latches the error on the trailing edge of the vertical strobe. Another counter is enabled and is clocked by the trailing edge of the vertical strobe. After eight counts (32 frames) a slow centering pulse is OR-gated into the WA0 counter advancing the write address to one line. The write address is therefore servoed to line 6.

Because the read address is preset to line 3 at the beginning of the frame and becomes line 1 at the 10th line of the vertical interval and the write address is servoed to line 6 (8) during the vertical interval, the correct read/write relationship is established at the beginning of the frame.

When the vertical strobe generator is locked out at the end of the strobe, the latch clock generator is enabled and centering continues to enforce the servo condition.

10-12 Search Mode

When in search mode (shuttle of the playback mechanism) the read addresses to the multiplexer in the write/read registration decode are enabled. The circuit then

begins to commute. Search also removes RMC as a condition for the latch clock and latch clock pulses are generated at each RA1-delayed flywheel sync interval. Therefore, the sampling rate is increased from 1-of-12 lines to 1-of-4 lines. Commutation of the address decode produces the following pattern:

Memory/Vertical Centering	Read Address	Search		
		RMA	RMB	RMC
Mux 1-A	Mux 1	A	B	C
Mux 2-B	Mux 2	B	C	A
Mux 3-C	Mux 3	C	A	B

The pattern produced by commutation generates artificial error signals at a rate proportionate to tape speed multiplied by the increased sampling rate. The error signals thus produced add or delete lines to maintain the correct number of lines of data loaded into memory. Although some lines may be deleted, or some may be loaded with false data, enough recognizable picture information is available to allow the operator to recognize the particular area of tape for which he is searching.

10-13 Interlace Select

During slow-motion editing by the playback mechanism, 1% (two and one-half lines) of video information is lost in each field due to mechanical considerations. To compensate for this, the STEP BACK signal from the playback mechanism deletes alternately two or three lines from successive fields (average two and one-half). Also, during this process the phase of the 3.58-MHz Fsc in Color Processor PWA 2 must be reversed at the correct time in the color field. See Figure 1-14, waveforms V through AA.

To delete the lost lines, two (or three) delayed flywheel sync pulses are OR-gated into the line address counters at reference vertical time. Thus, these lines are deleted before the field begins.

At tape vertical time the even/odd comparator U7/U21/U33/U36/U90/U91 in the interlace select circuitry checks the relative position of delayed flywheel sync pulses and ADV V/2 to determine if the following field will be an even or odd number in the color field. During the time the lost lines are deleted, the even/odd signal is gated to the color processor.

10-14 MAINTENANCE

See Figure 10-15 for component locator diagrams and jumper, test point, and adjustable component summaries.

Before undertaking any adjustments to the Memory Control PWA, review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-6 for a general understanding of the scope of these field adjustments.

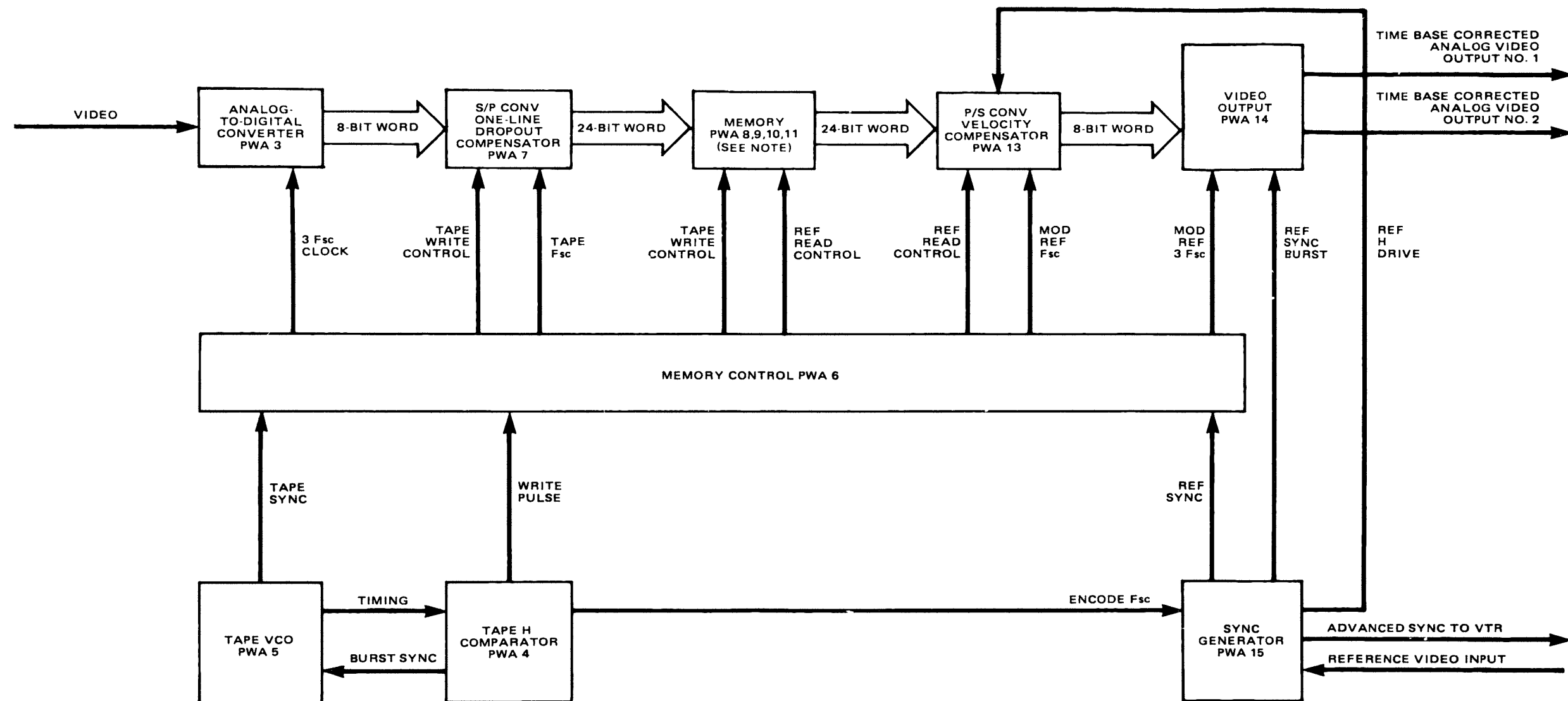
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Consult the waveforms and interconnect data on the simplified schematics to confirm normal operation of the Memory Control PWA and interactive functions between it and other PWAs before making any adjustments.

There are two adjustments on the Memory Control PWA. The first, S2 (H-video position), is described in the system level tape-H/sync-to-video timing adjustment (paragraph 3-14, step 10).

The velocity-compensated reference subcarrier (read Fsc) is tripled and becomes the source for read clock timing of the Memory, P/S Converter, and Video Out PWAs. The adjustment ensures a symmetrical reference 3Fsc signal, and is accomplished as follows:

- STEP 1 Use the tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.
- STEP 2 Connect oscilloscope to U93-13; trigger on internal.
- STEP 3 Adjust R81 for a 50% duty cycle.
- STEP 4 Connect oscilloscope to TP10 (3X subcarrier); trigger on internal.
- STEP 5 Adjust L1 (3Fsc peaker) and L2 (3Fsc filter) for maximum 3Fsc—ranging between 1.5 and 4.0 Vp-p.



NOTE: MEMORY PWA 11 IS ADDED TO SYSTEM FOR 16-LINE VERSIONS OF THE TBC-3.

Figure 10-1.
TBC-3 Data Flow Block Diagram

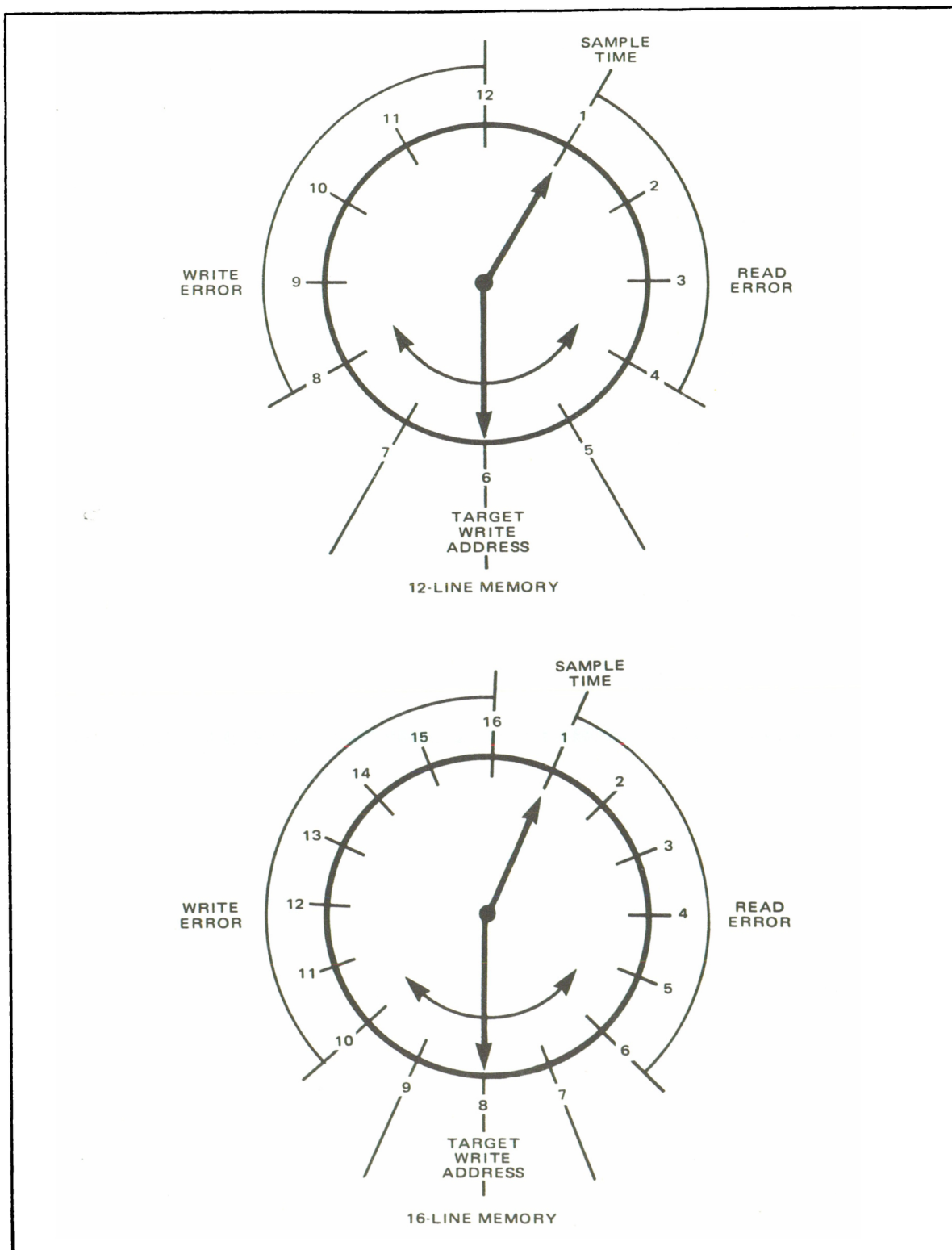


Figure 10-2. Read/Write Time Relationship, Memory Control PWA 6

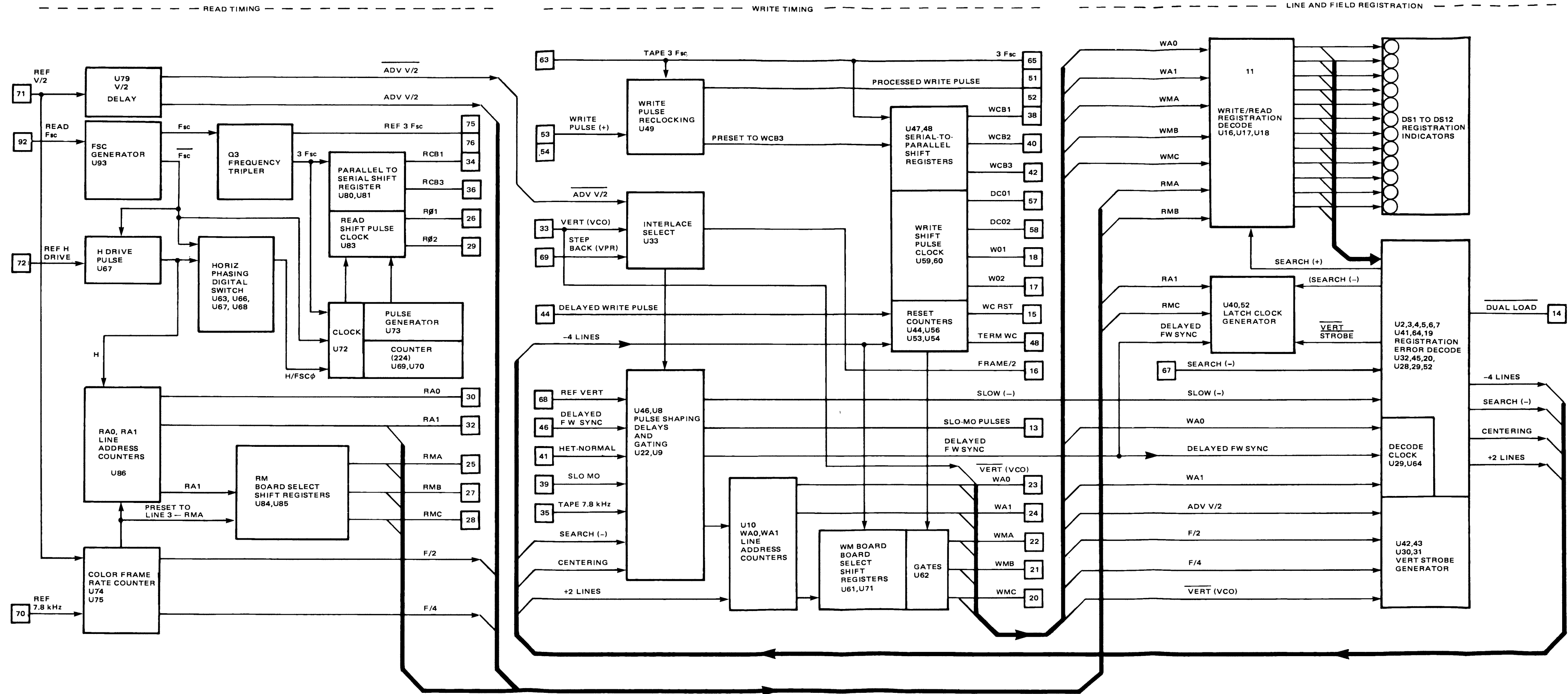


Figure 10-3.
Memory Control PWA 6 Block Diagram (12-line)

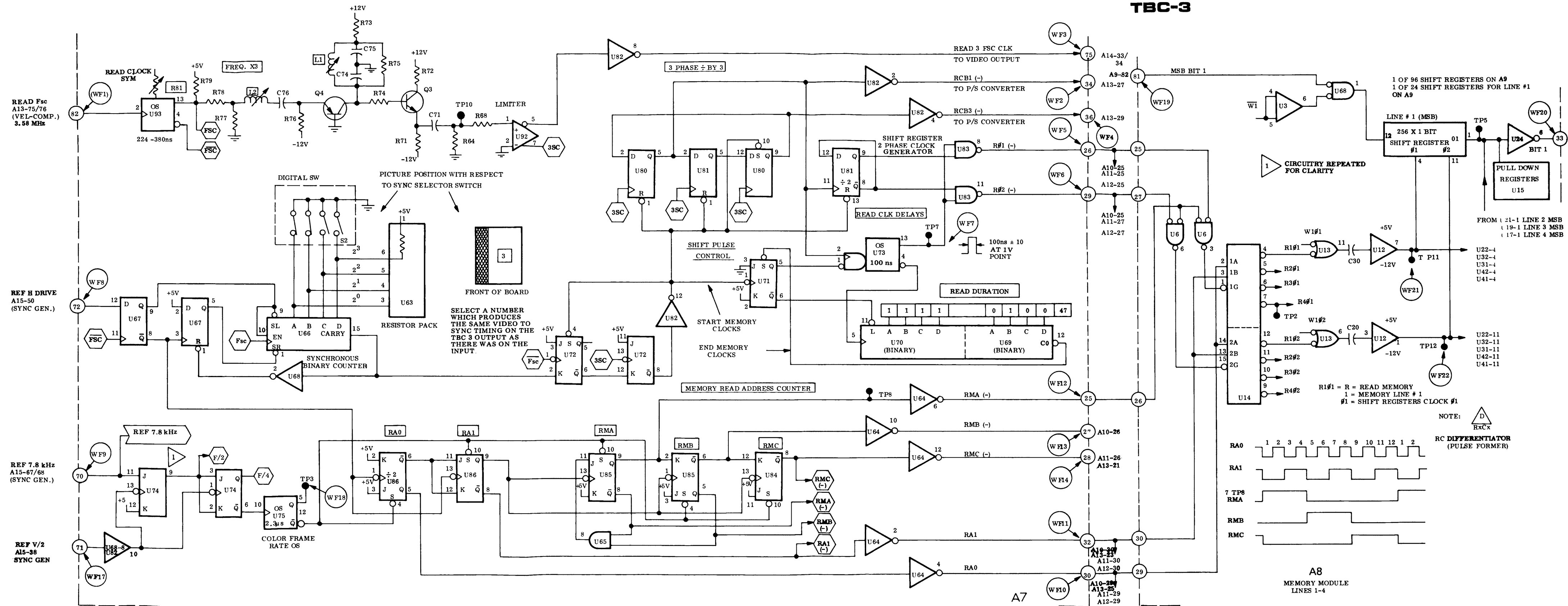


Figure 10-4.
Read Control Simplified Schematic,
Memory Control PWA 6 (12-line)

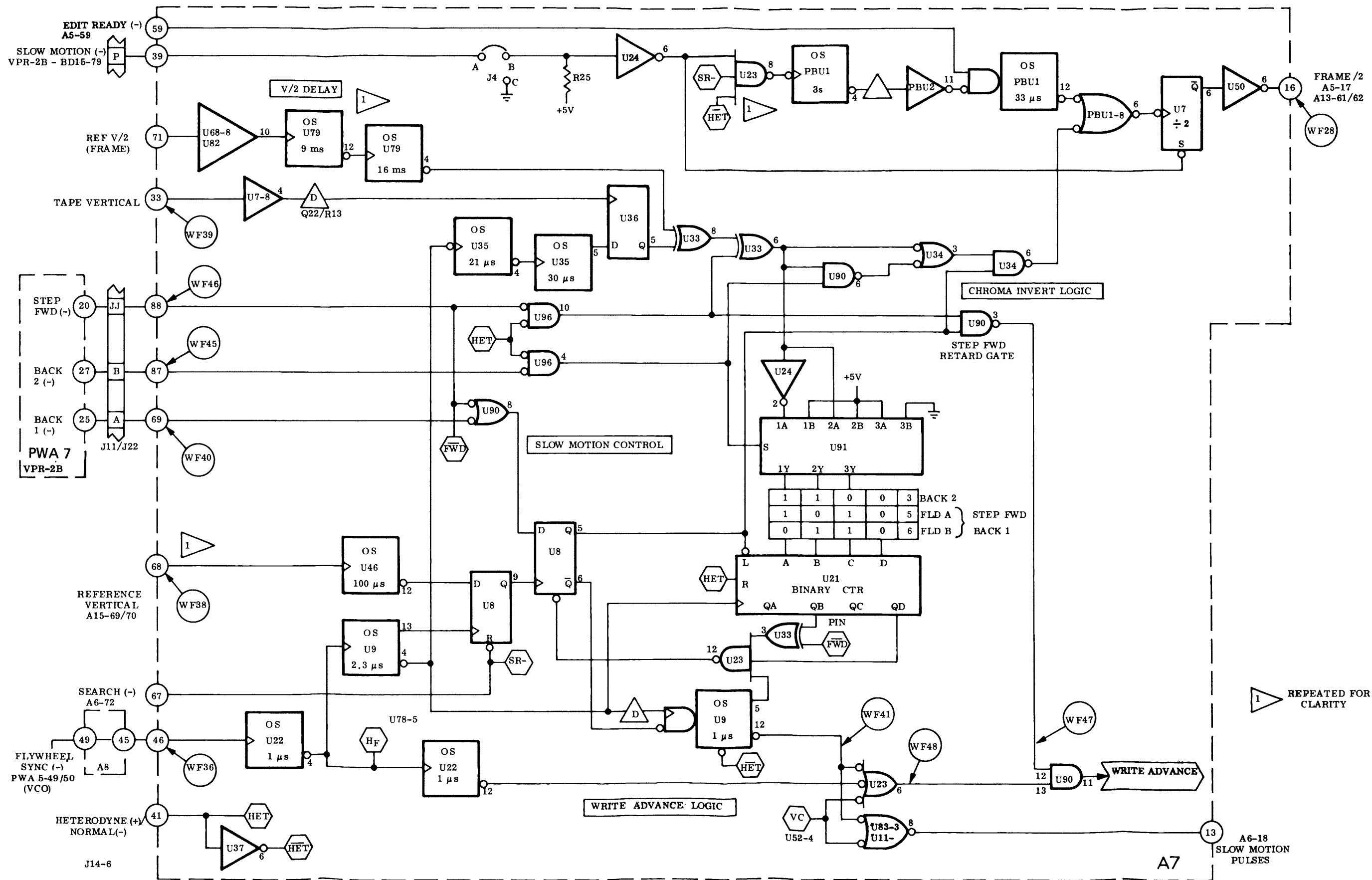
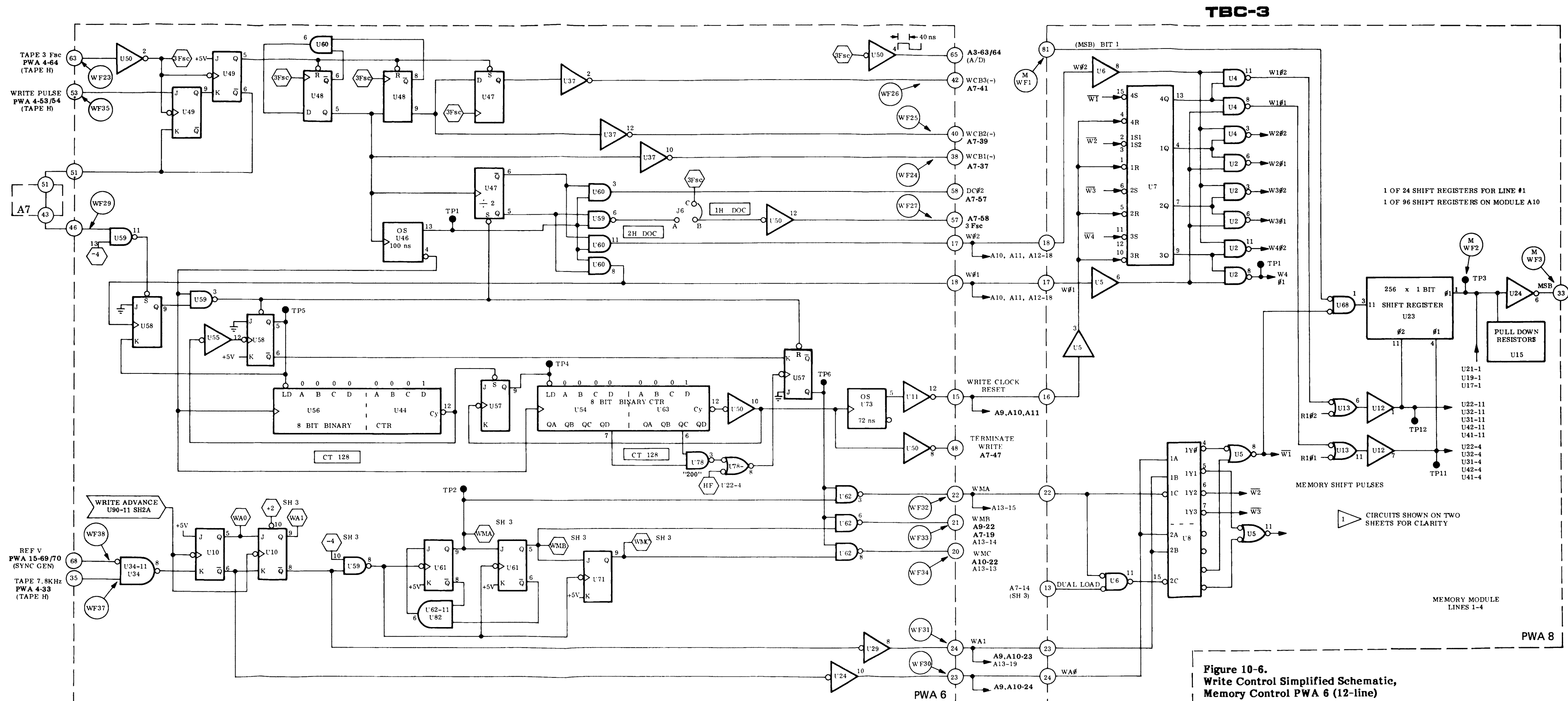


Figure 10-5.
Write Control Logic Simplified Schematic,
Memory Control PWA 6 (12-line)



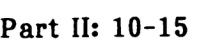


Figure 10-7.
Memory Overload Sense and Memory Centering,
Simplified Schematic, Memory Control PWA 6 (12-line)

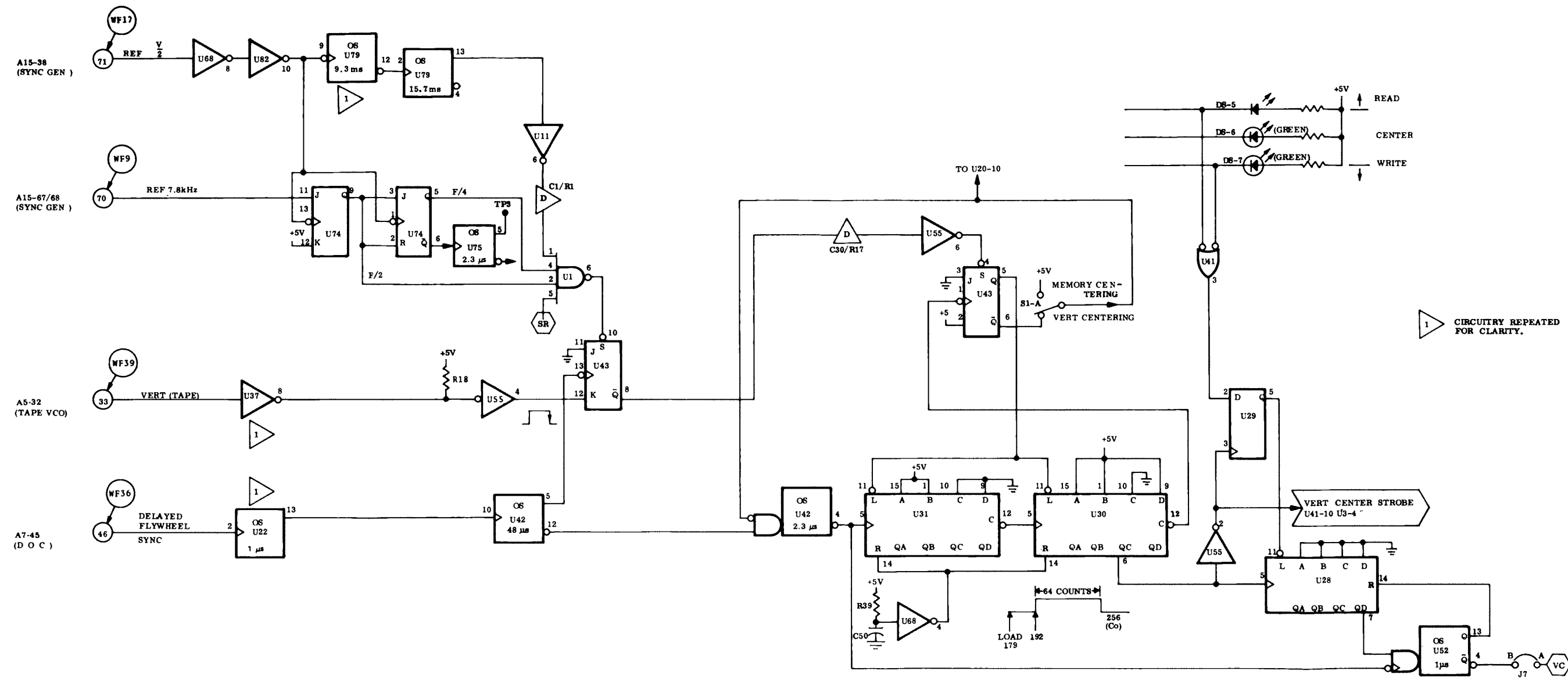


Figure 10-8.
Memory Overload and Vertic Centering Simplified Schematic,
Memory Control PWA 6 (12-line)

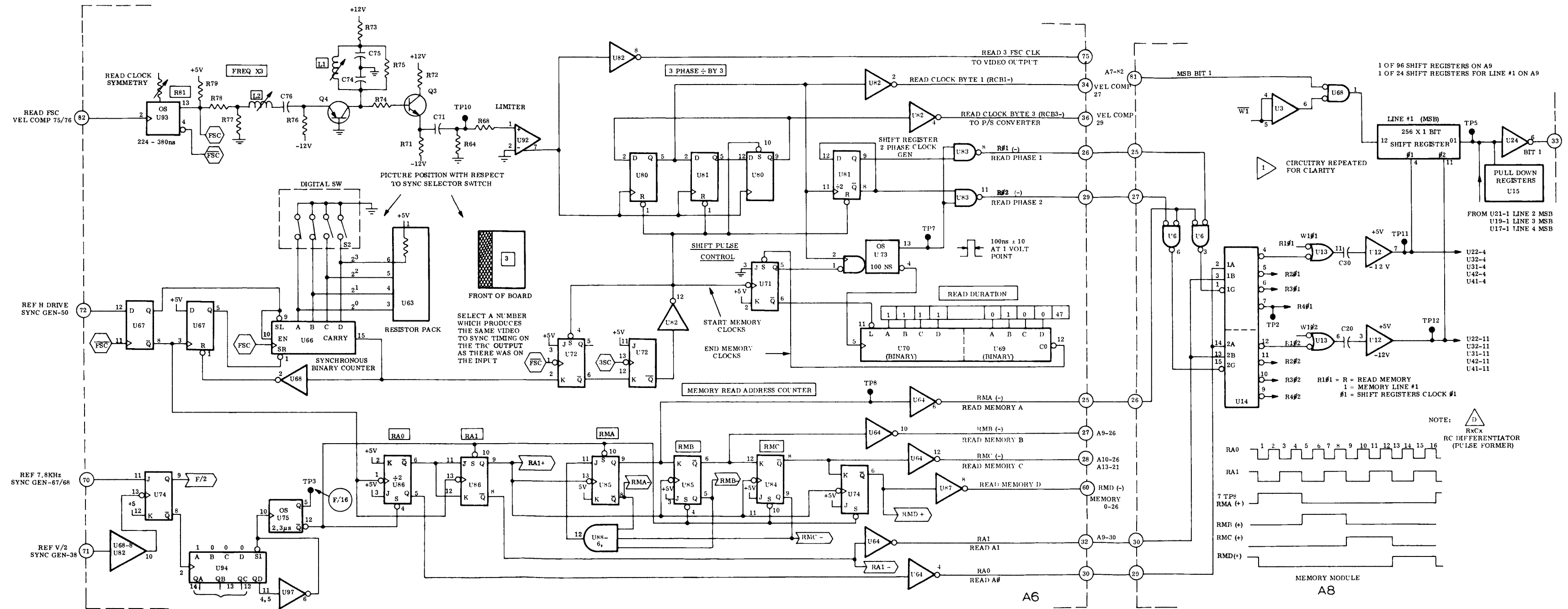


Figure 10-9.
Read Control Simplified Schematic,
Memory Control PWA 6 (16-line)

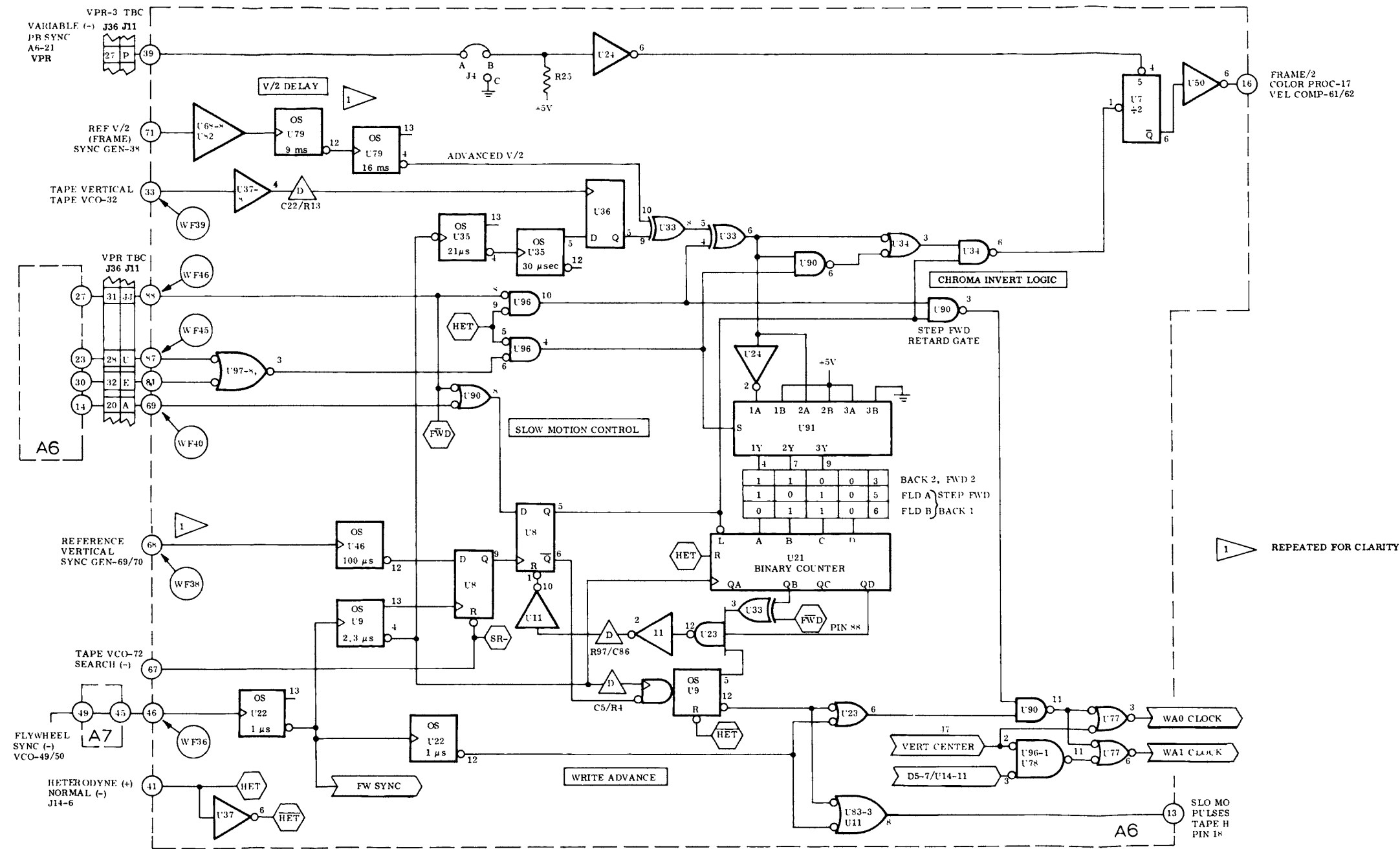


Figure 10-10.
Write Control Logic Simplified Schematic,
Memory Control PWA 6 (16-line)

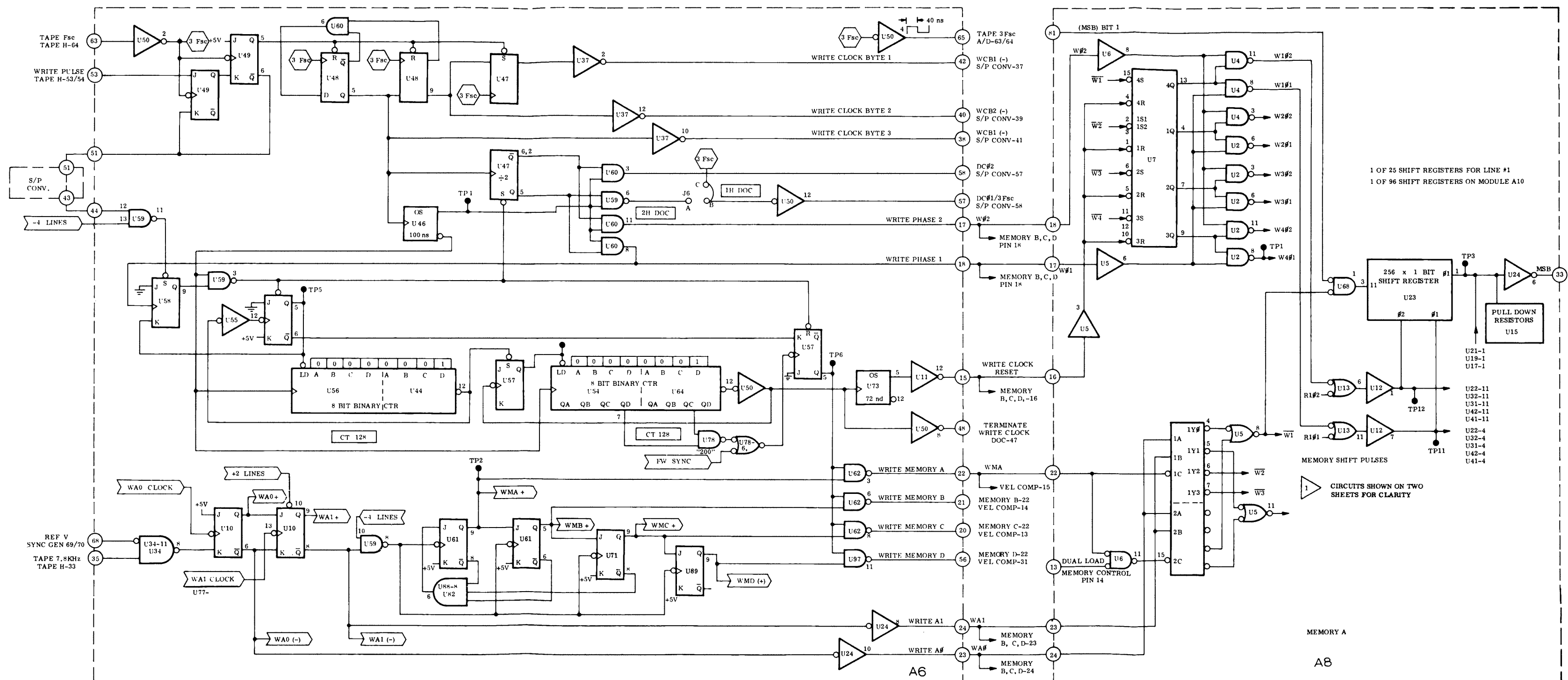


Figure 10-11.
Write Control Simplified Schematic,
Memory Control PWA 6 (16-line)

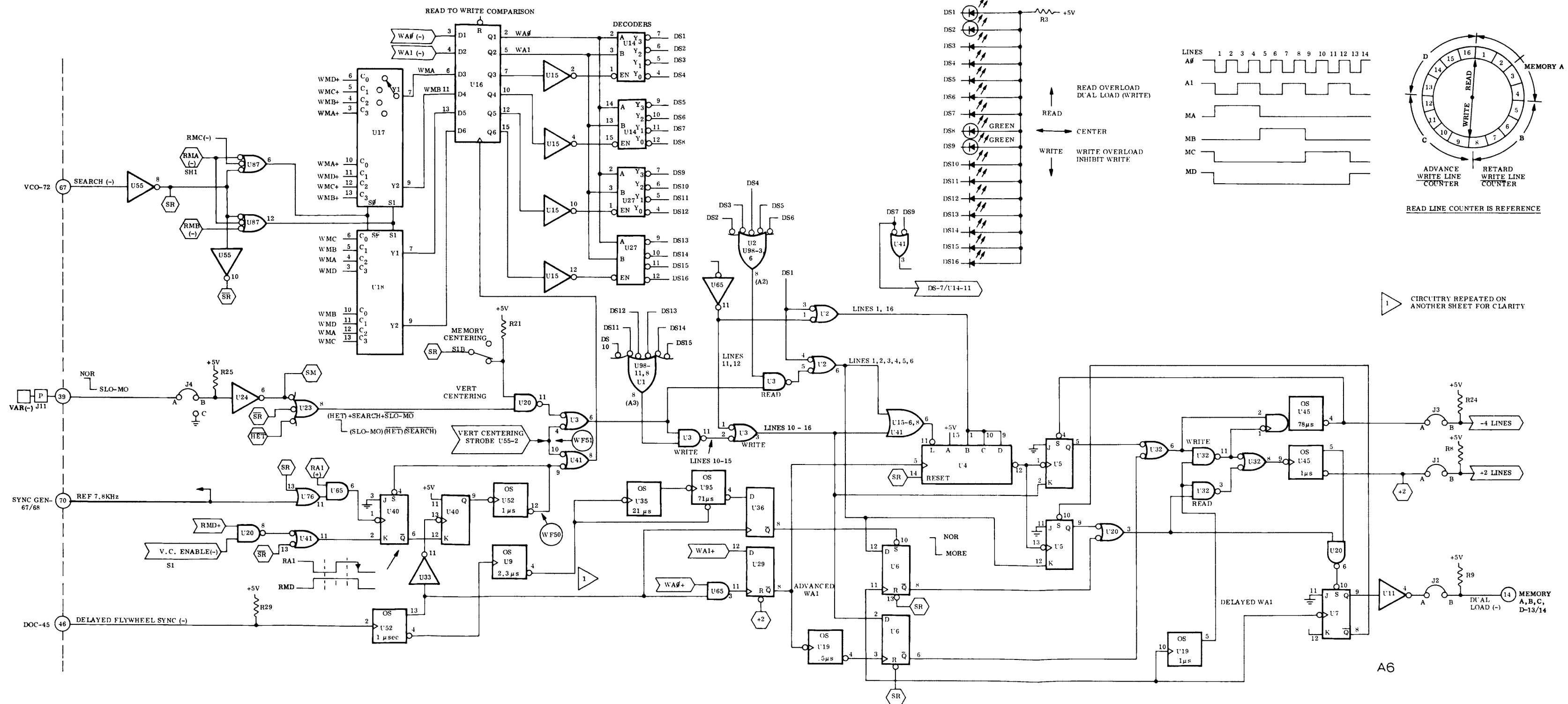


Figure 10-12.
Memory Overload Sense and Memory Centering Simplified
Schematic, Memory Control PWA 6 (16-line)

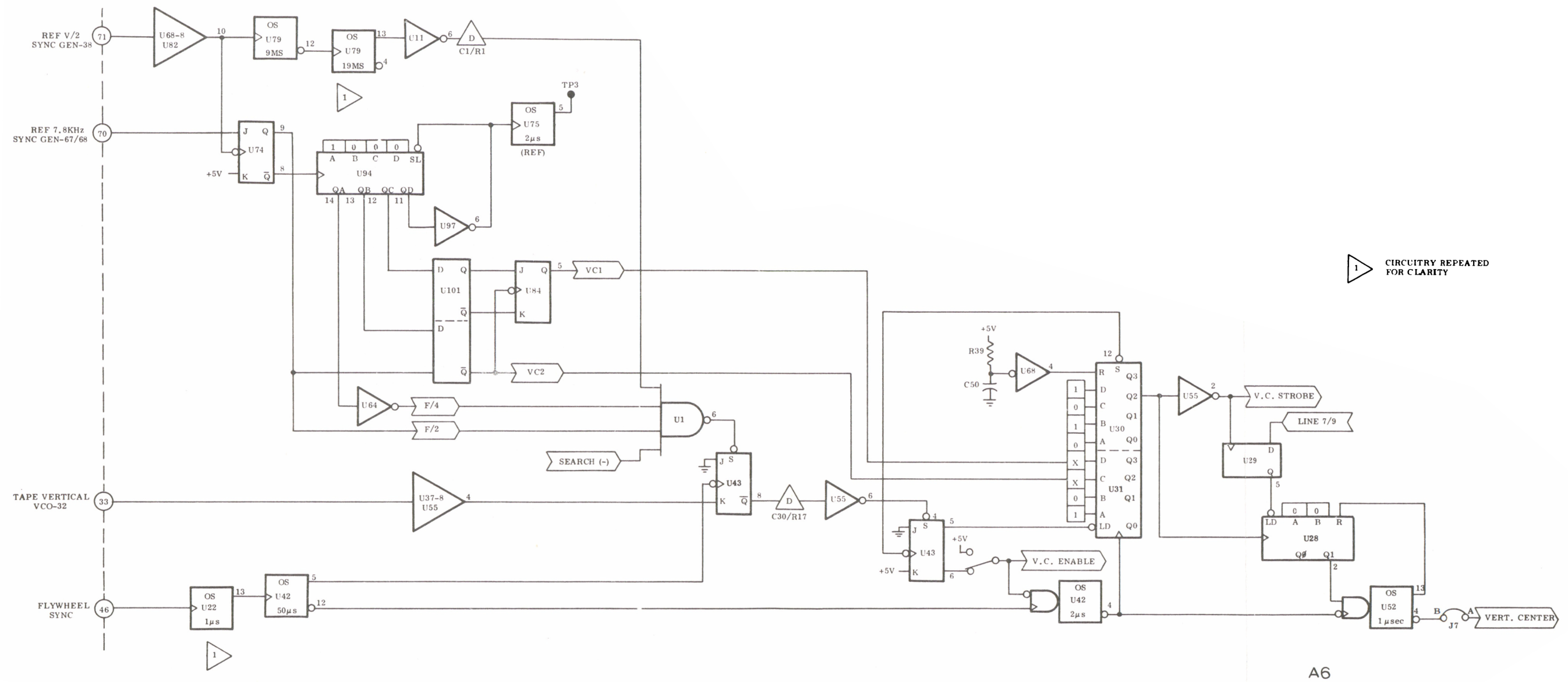


Figure 10-13.
Memory Overload and Vertical Centering Simplified
Schematic, Memory Control PWA 6 (16 line)

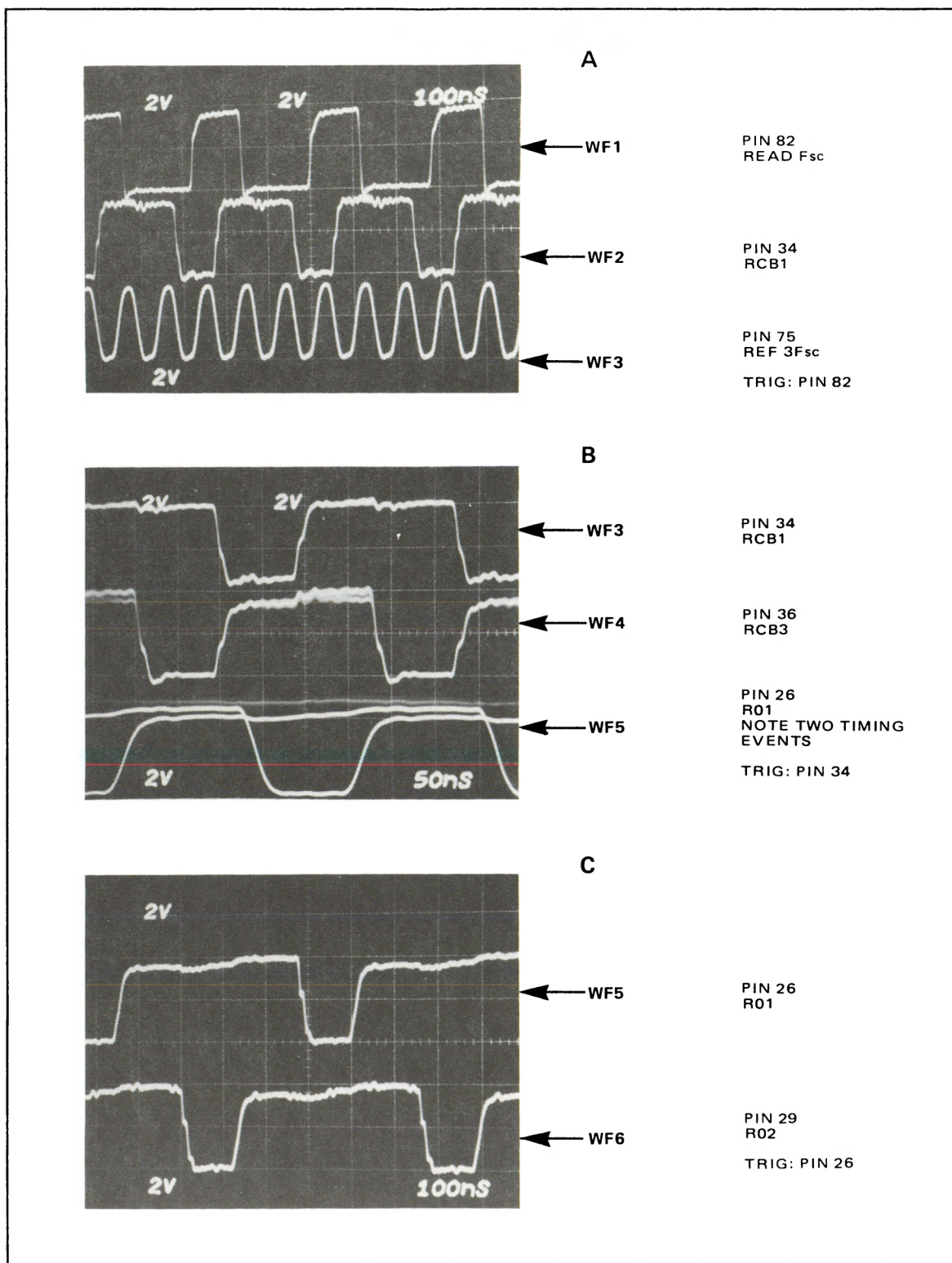


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 1 of 10)

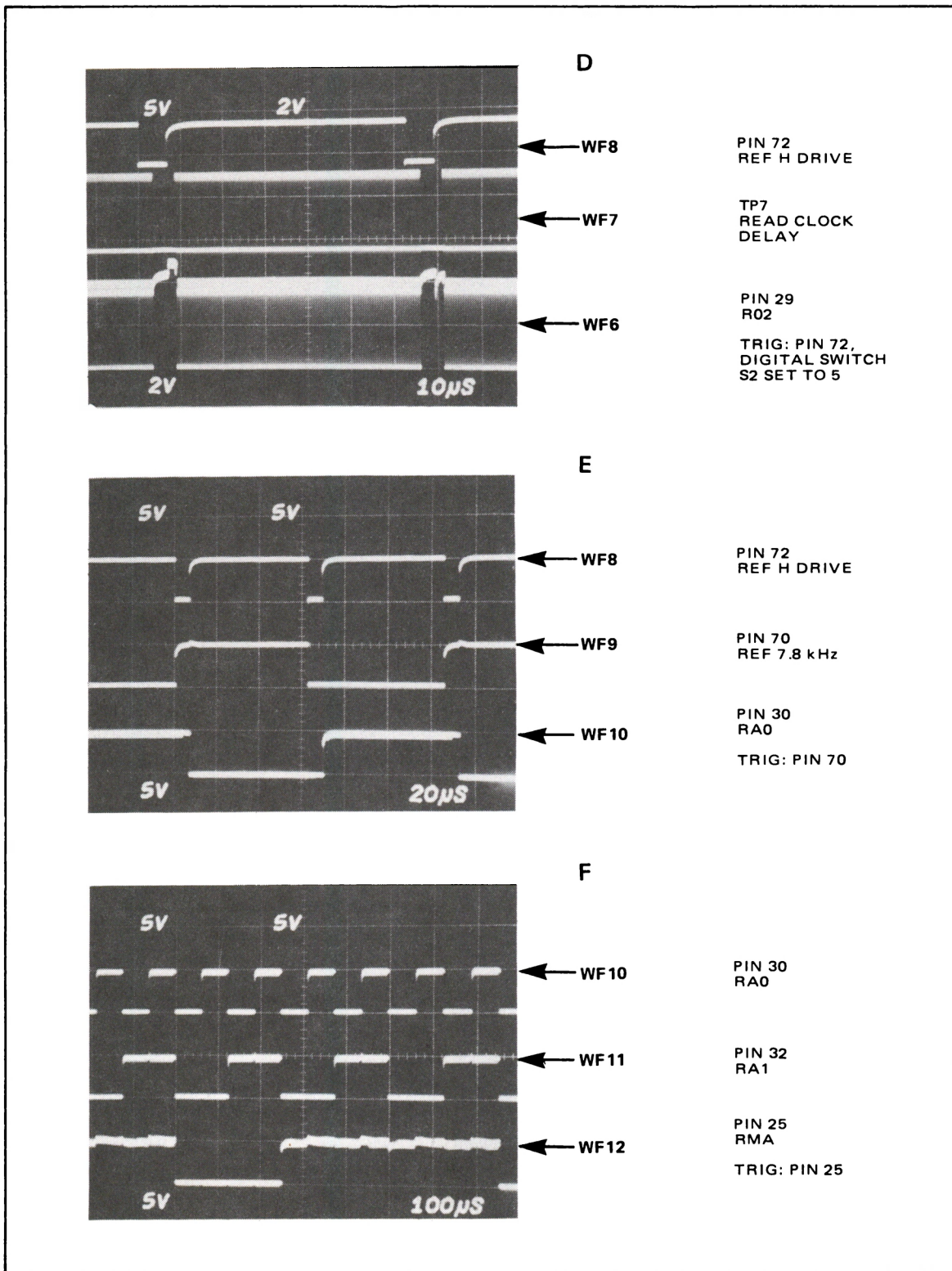


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 2 of 10)

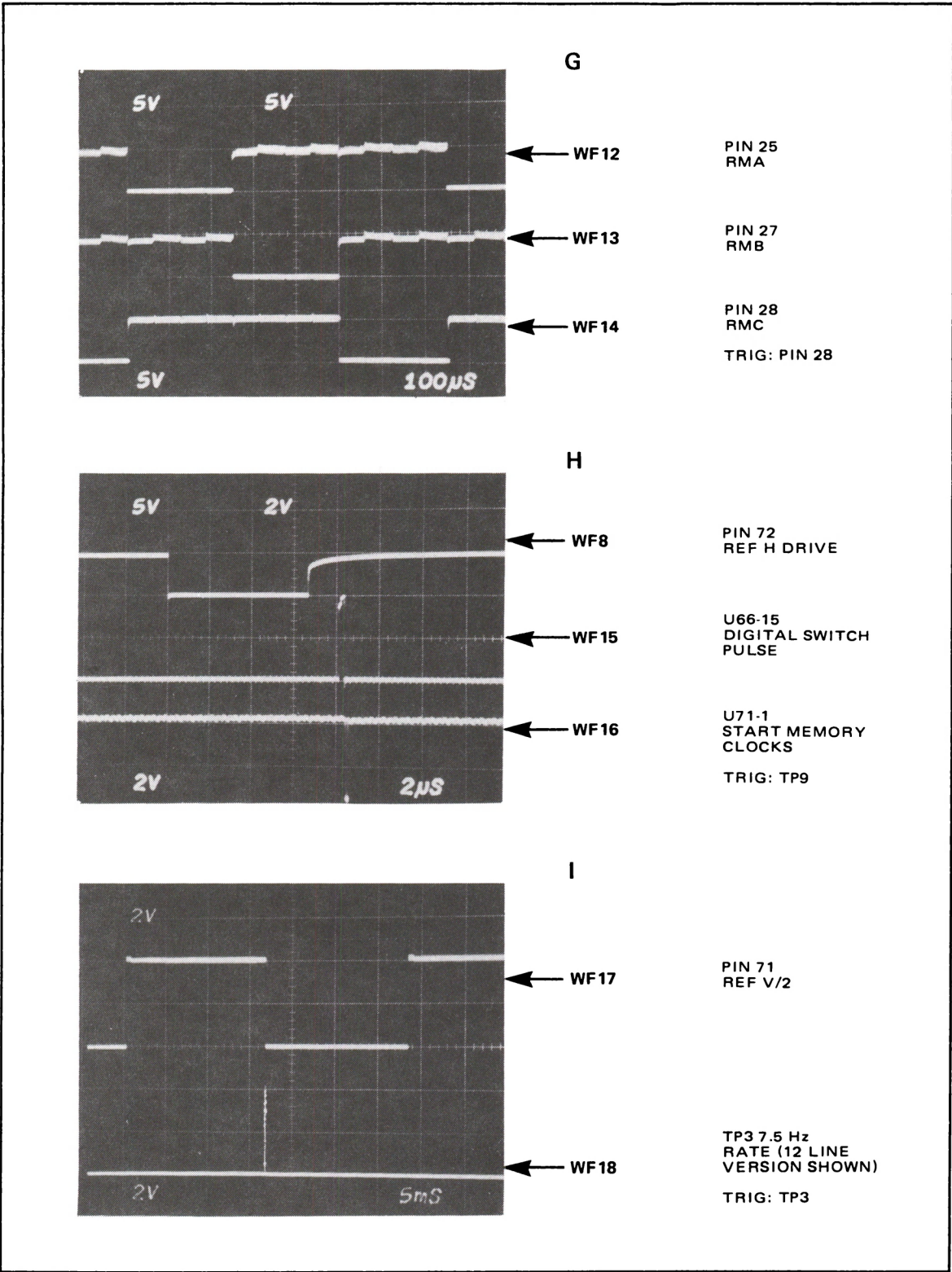


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 3 of 10)

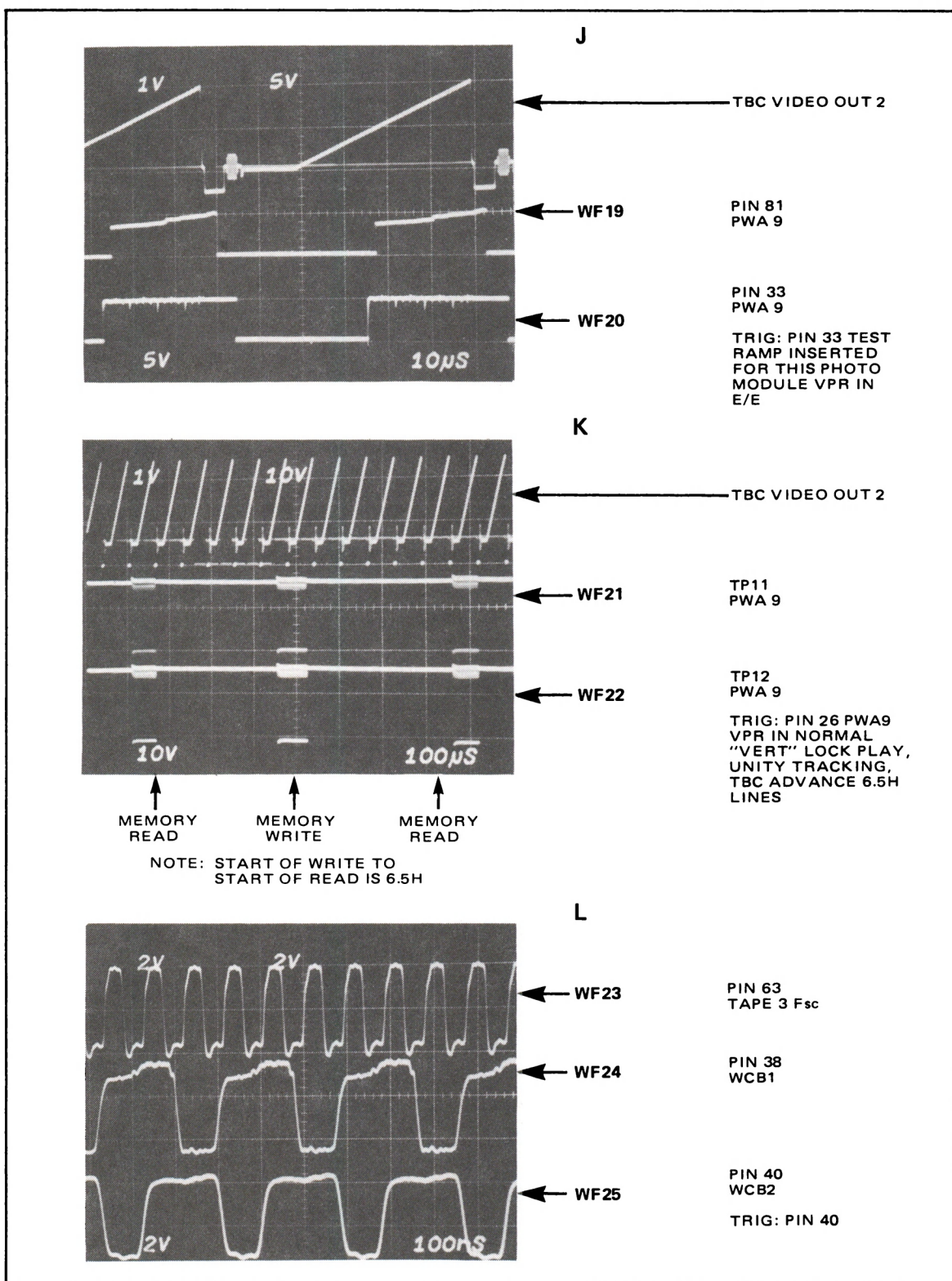


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 4 of 10)

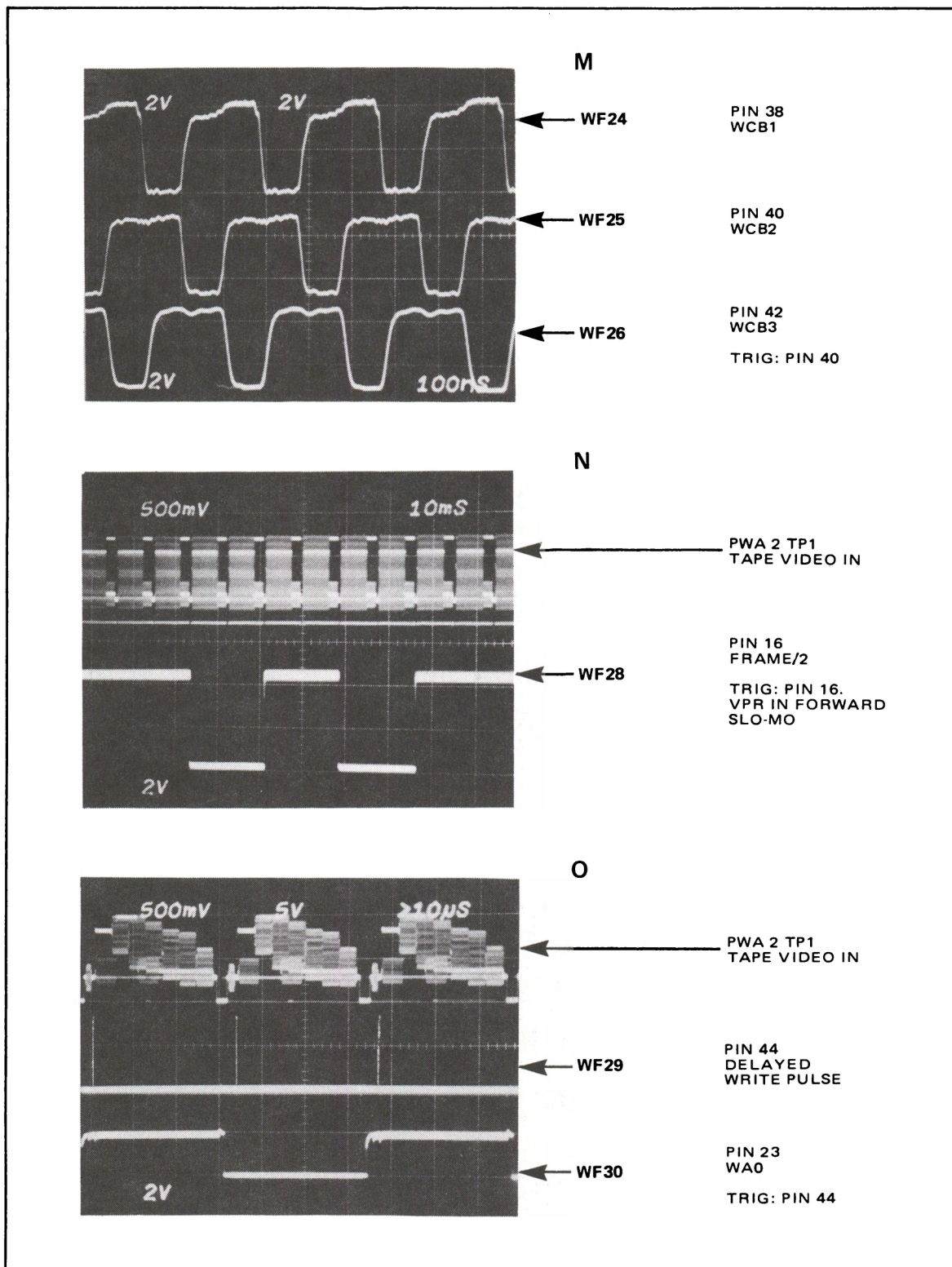


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 5 of 10)

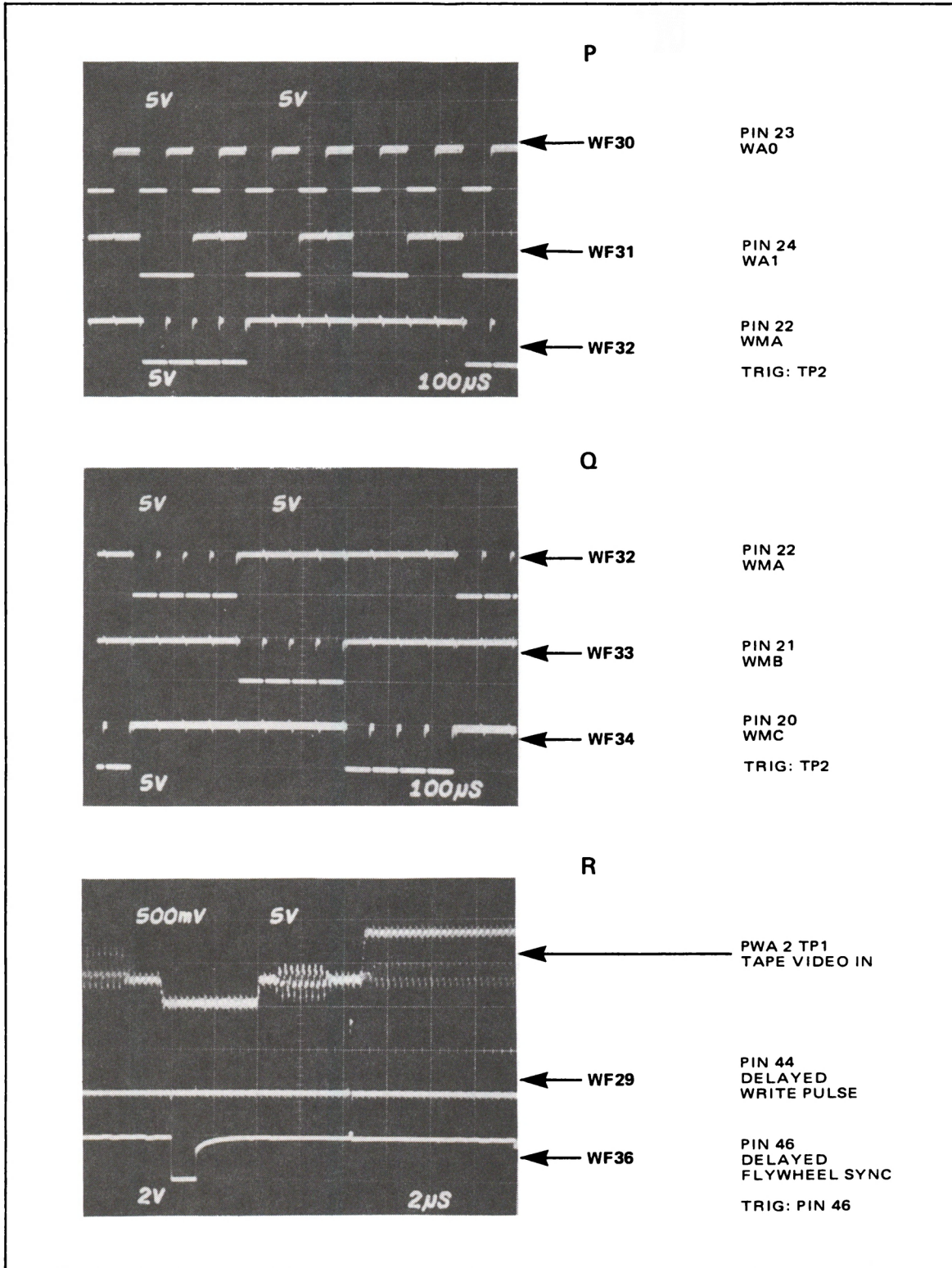


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 6 of 10)

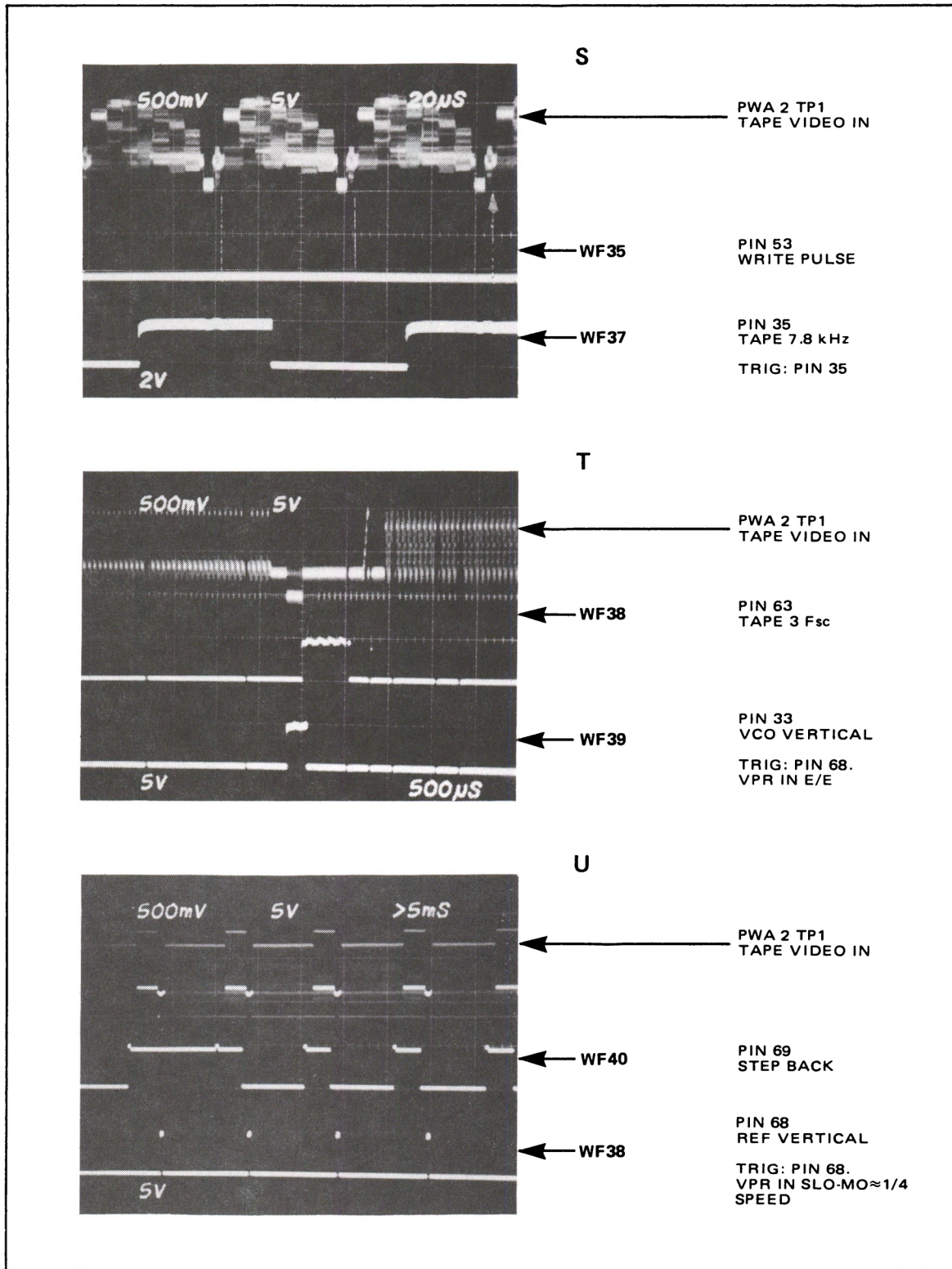


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 7 of 10)

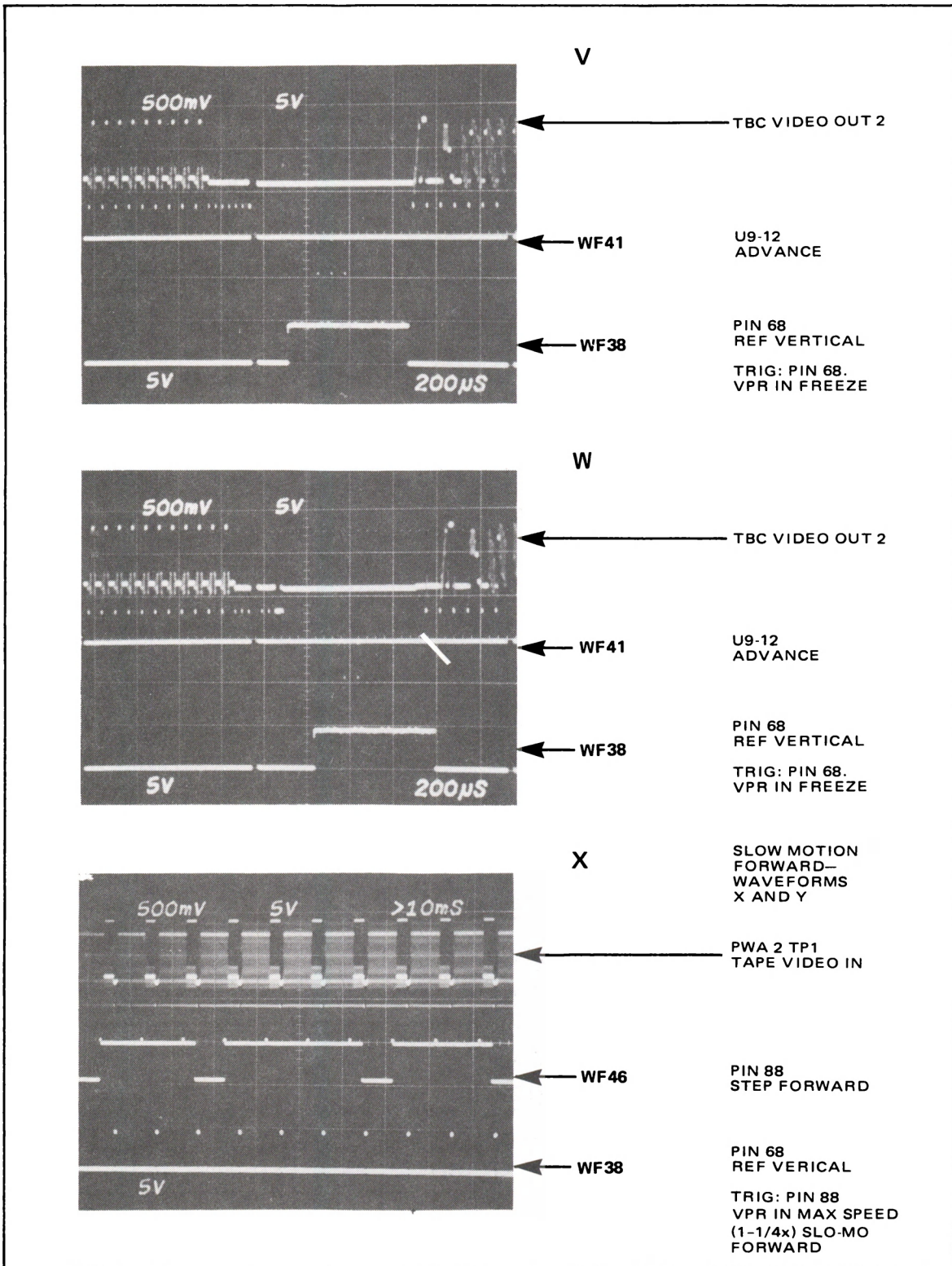


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 8 of 10)

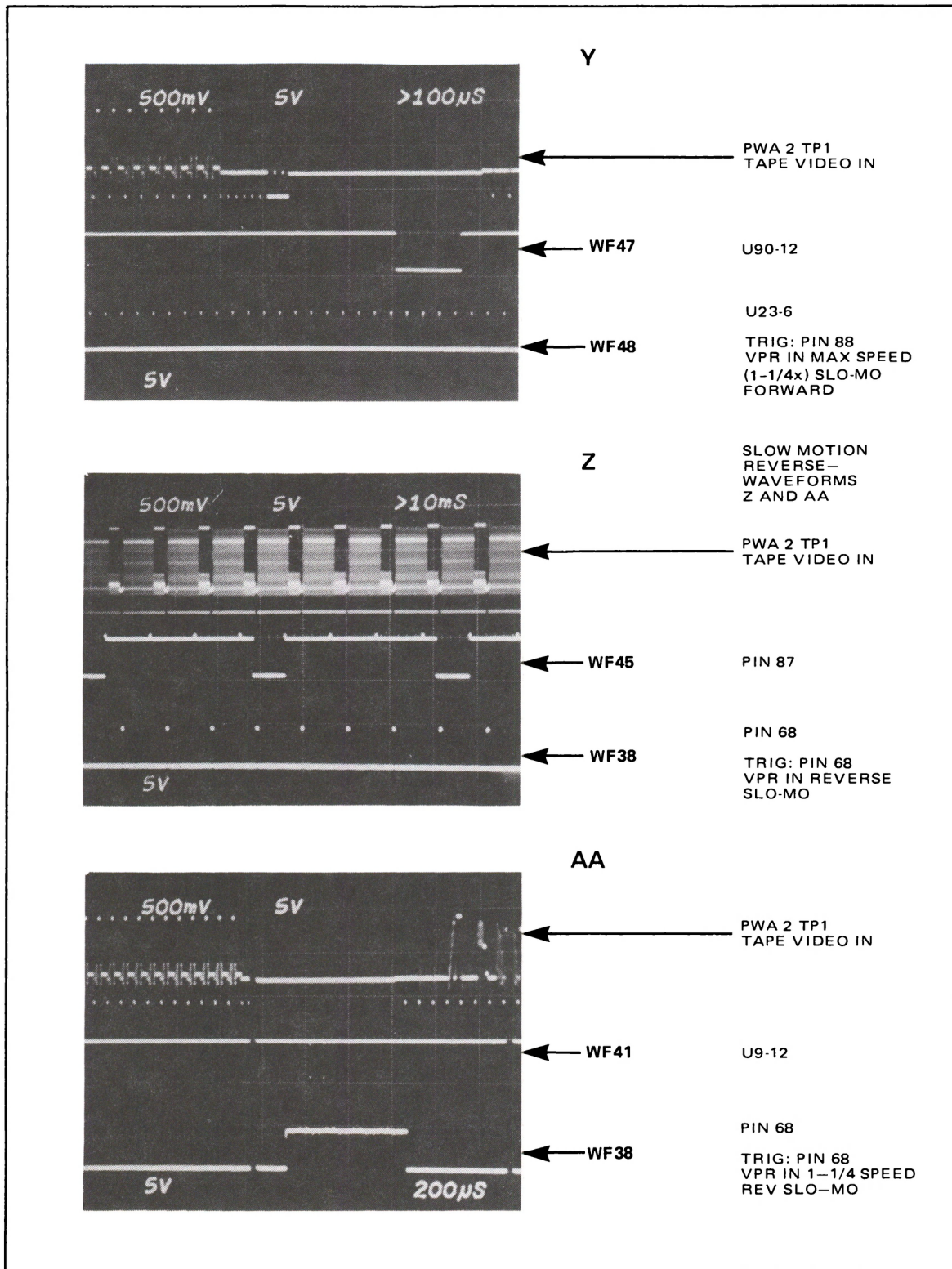


Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 9 of 10)

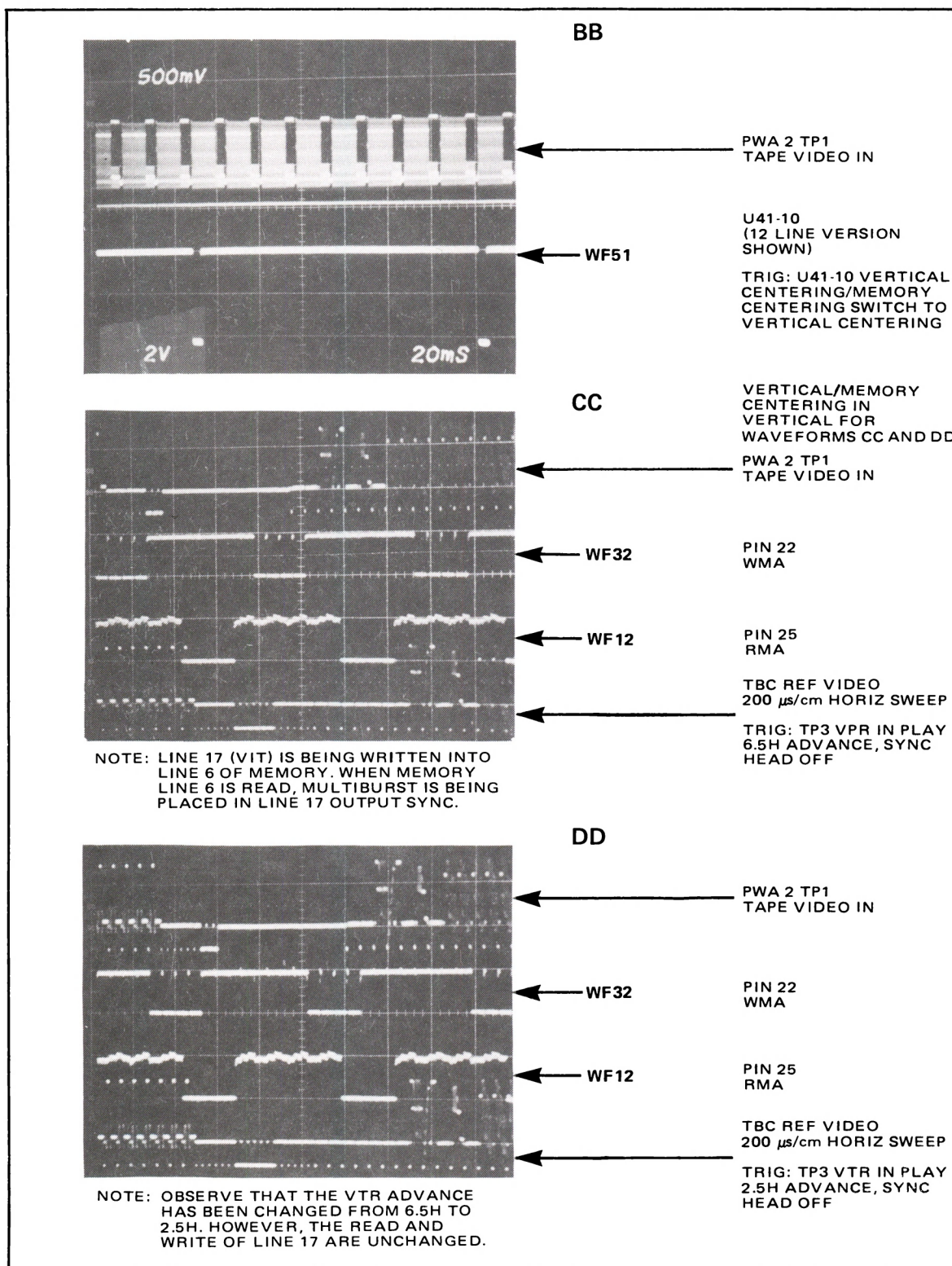


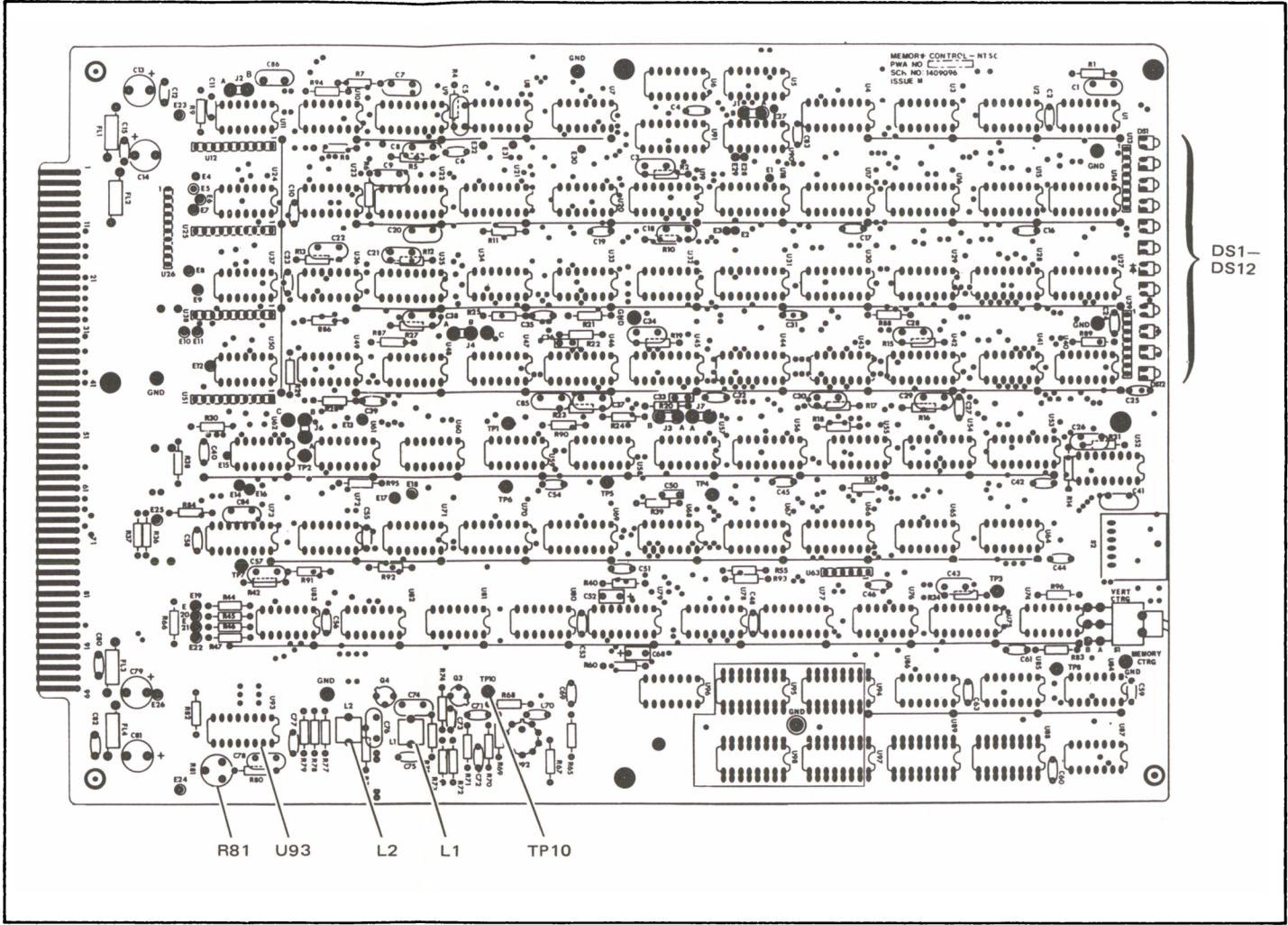
Figure 10-14. Memory Control PWA 6 Waveforms (Sheet 10 of 10)

PWA 6 Jumpers

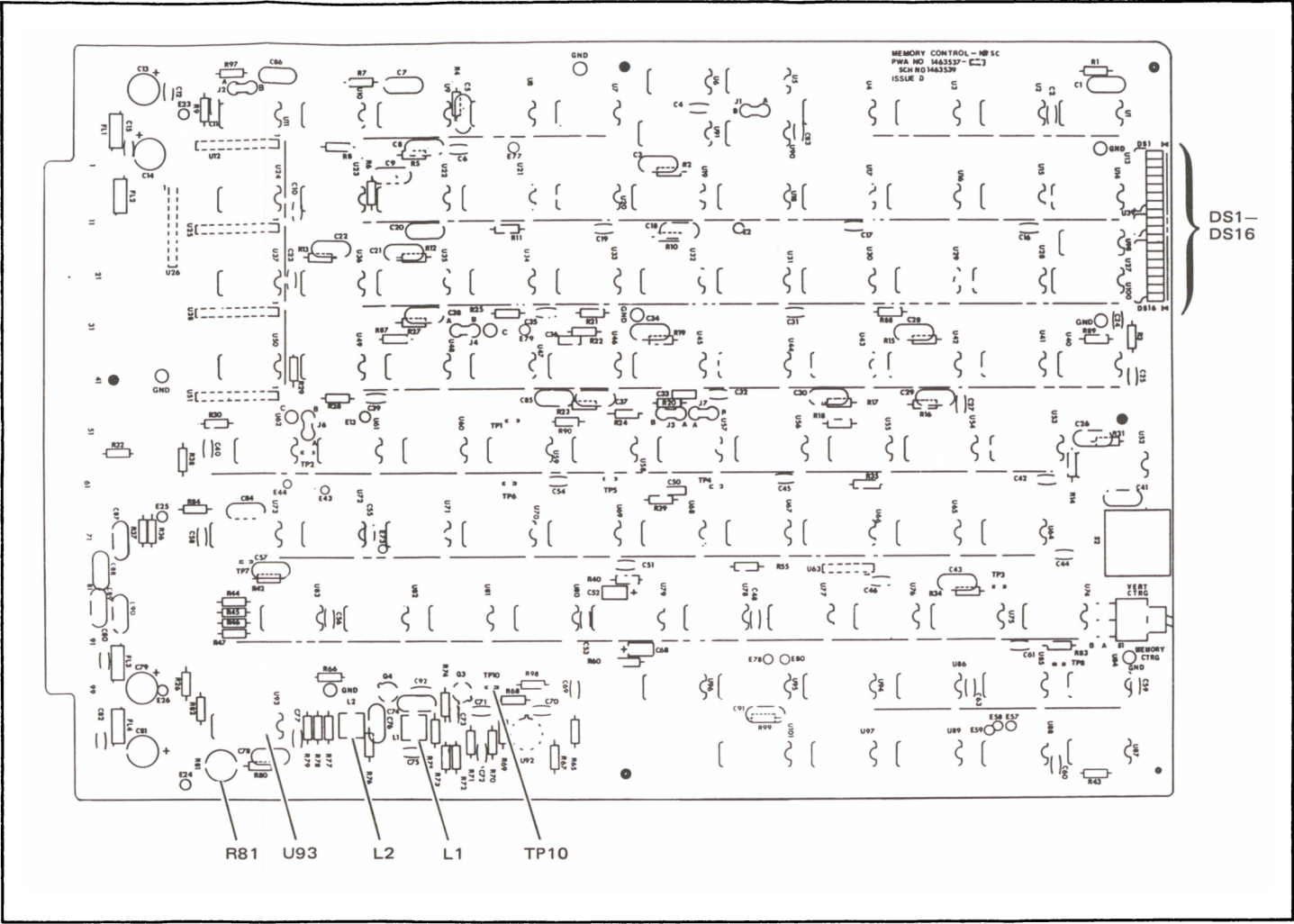
Jumper	Position	Function
J1	A-B Removed	+ 2 lines Normal Test; disables + 2 line signal
J2	A-B Removed	Dual Load Normal Disables dual load signal
J3	A-B Removed	-4 lines Normal Test; disables -4 line signal
J4	A-B B-C	Slo-Mo Normal Test; forces slow motion
J6	A-B B-C	Dropout Select Two-line DOC (PAL/SECAM) One-line DOC (NTSC)
J7	A-B Removed	Centering Normal Factory Test only

PWA 6 Adjustable Components

Component	Function
L1	3x subcarrier peaker
L2	3x subcarrier filter
R81	Read clock symmetry
S2	H/Video position
S1	Memory/Vertical Centering



PWA 6 Component Locator-12 Line



PWA 6 Component Locator-16 Line

PWA 6 Test Points

Test Point	Function
TP1	100 ns pulse Fsc
TP2	Write memory A
TP3	F/4 (12-line), F/16 (16-line)
TP4	H rate
TP5	H rate
TP6	Write enable
TP7	120 ns pulse at Fsc
TP8	Read memory A
TP9	(not used)
TP10	3x subcarrier

Figure 10-15.
Test Points, Jumpers, Adjustable Components,
Component Locator, Memory Control PWA 6

PART II

SECTION 11

SERIAL/PARALLEL ONE-LINE DOC PWA 7 DESCRIPTION AND MAINTENANCE

11-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1409140
Schematic No. 1405132

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section:

- Figure 11-5, detailed block diagram
- Figures 11-6 to 11-9, simplified schematic
- Figure 11-10, waveforms
- Figure 11-11, maintenance data

S/P One-Line DOC PWA 7 function summary:

- Converts 10.7-MHz rate 8-bit data from A/D Converter PWA to 24-bit bytes at 3.58-MHz rate for entry into memory.
- From the flow of data, the dropout compensator (DOC) continuously stores processed luminance from one line previous and chrominance from two lines previous. This stored data is inserted into the data stream when a dropout is detected by the DOC control logic.

11-2 DESCRIPTION

A short section of a recorded signal that is severely attenuated or missing is known as a dropout. Fortunately, in video there is redundancy in the signal that can be used to disguise dropouts when they occur.

The TBC one-line DOC uses the substitution technique. In order to substitute information from the past, it must be stored in memory as it arrives from the tape. The TBC DOC processes the video as luminance and chroma components, then reassembles these as composite video. Chroma is derived from two lines past and luminance from one line past. The simplified block diagram of Figure 11-1 illustrates the signal flow in the one-line compensation circuits. Note that the circuit blocks call out the appropriate simplified schematics from reference data at the end of this section.

11-3 Functional Description

See Figure 11-1 and Figure 11-5. Video information from the A/D Converter PWA is latched by the input multiplexer and is designated as A-data to the digital luminance filter. Luminance is extracted by taking the average of three adjacent 10.7-MHz samples. The resulting luminance (\bar{L}) is subtracted from a delayed composite video word (V-data) which is the middle word of the three samples to obtain the chroma component, D-data. A complete line of D-data words is stored for a period of one horizontal line in the RAM chroma memory. Data is read out of memory as C-data. C-data is added to L-data which has been delayed by two clock pulses to match the processing delay of the C-data. The L+C multiplexer checks the resulting composite video word for an overload condition. If an overload is detected for a given word, a corrected word will be substituted in the multiplexer latch. The output of the latch, F-data, is stored in the one-line video memory for a one horizontal line period. Data is read out of the one-line video memory into the M-latch. Addressing of the data out of the memory is advanced by nine words to match the total processing delay of the data. Thus the M-data is in step with the data from the A/D Converter PWA. If a dropout is detected, data from the A/D Converter is blocked and M-data is substituted by the input multiplexer. Substitute data is sent to the serial-to-parallel converter circuit as A-data. If a multiline dropout condition occurs, data stored in the dropout compensation memory is recirculated until dropout condition terminates. In normal operation, incoming digital video data from the A/D is passed directly to the serial-to-parallel converter circuit and then to Memory PWAs 8, 9, 10, and 11 (if used).

Recirculated data of a multi-line digital dropout compensation will deteriorate in quality on each iteration of a line. This is similar to the result obtained with analog delay lines. Contemporary high-quality tapes tend to have dropouts of one-third line or less in length; therefore, this effect is not usually noticeable.

The deterioration of quality in digital dropout compensation is primarily due to round-off of the digital numbers in the processing of luminance and chroma data and the cumulative error resulting from recirculation of the data.

The output of the input multiplexer latch is designated as the A-data bus. The A-data bus serves

- the serial-to-parallel converter,
- the B-latch, and
- the digital luminance filter.

In the digital luminance filter, three successive samples of video data are added and divided by three to obtain the luminance value. Luminance level is centered on the positive and negative peaks of the chroma signal; or conversely, chroma is centered on luminance.

11-4 Digital Luminance Filter

See Figure 11-6. The luminance filter adds the three samples of video and divides the value by four. Further processing adds incrementally decreasing values until the final result is equivalent to a divide-by-three. The entire operation is a series

of add—shift right, add—shift right, add, etc. operations. The sequence of events is as follows:

1. Sum samples A and B. Carry in is 0 (U75/84).
2. Divide result by 2, enter carry as MSB (U57/50).
3. Divide sample C by 2 and add to $\frac{A+B}{2}$. 1-8 bit of C is carry in (U58/67).
4. Divide result by 2 and enter carry as MSB (U49/50).
5. Result is S value. $S = \frac{A+B+C}{4}$. (U49/50).
6. Divide S by 4 and add to S. S-7 bit is carry in (U39/48).
7. Result is P value (U40/14).
8. $P = (A + B + C) + (1/4 + 1/16)$
9. Divide P by 16 and add to P. Carry-in is 0 (U32/23).
10. Result is L value, or luminance (U31/22).
11. $L = (A + B + C) + (1/4 + 1/16 + 1/64 + 1/256) = (A + B + C) + (85/256) = (A + B + C/3)$ to 8-bit accuracy.
12. L-bar is the one's complement of L (U31/22).

All operations are hard-wired. Divide-by-two (U58/U67) is accomplished by a hard-wired shift right one bit. Divide-by-four (U39/U48) is accomplished by a hard-wired shift right two bits. Divide-by-16 (U32/U22) is accomplished by a hard-wired shift right four bits.

For the purpose of analysis of the digital one-line dropout compensator, the chroma signal of the following example is considered to have the same phase as subcarrier (10.7-MHz clock). It is assumed that clocking occurs as indicated in Figure 11-1. The serial stream of 8-bit words from the A/D Converter PWA is latched into the input multiplexer by the 10.7-MHz clock. Sample A is the output of the B-latch. Sample B is the concurrent data on the A-bus. Sample C is the data on the A-bus on the following clock pulse. The three samples are shown in Figure 11-2.

The example in Figure 11-2 uses an arbitrary chroma positive peak value of 250, a chroma negative peak at 50, and a luminance value of 200. The average value of luminance is thus 150. Sampling occurs at $+60^\circ$, 0° , and -60° . ($\sin 60 = 0.866$ ($0.866 \times 100 = 87$), or 87 bits. Therefore sample A = $150 + 87 = 237$, sample B = 150, and sample C = $150 - 87 = 63$.

$A + B = (236 + 150) = 386$. 386 is an overflow condition. The sum at the output is 130 plus a carry-out of one (next highest bit). A hard-wired shift right is equivalent to a divide-by-two. Placing the carry in the most significant bit (MSB) of the latch carries forward the 256-bit of the sum, down-shifted to 128. The value 131 becomes 65.

$$\frac{A+B}{2} = 128 + 65 = 193$$

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$C/2 = 65/2 = 32$. The C sample is hard-wired shift right one bit (divide-by-two)

$$\frac{A+B}{2} + \frac{C}{2} = (193 + 32) = 225$$

The output of the second adder is hard-wired shift right one bit (divide-by-two). The carry out to the MSB of the latch is 0 in this example. Therefore, the latch output is $225/2 = 112 = S$ value.

$$\frac{\frac{A+B}{2} + \frac{C}{2}}{2} = \frac{A+B+C}{4} = 112 = S$$

$$S/4 + S = P = (112/4 + 112) = (28 + 112) = 140$$

$$P/16 + P = L = (140/16 + 140) = (8 + 140) = 148 = L$$

$$L = \frac{A+B+C}{4} = 148$$

$$L\text{-bar} = \text{one's-complement-of-}L = 256/148 = 108$$

11-5 Chrominance Subtractor

See Figure 11-7. V-data is B-data delayed by three clock cycles to establish the comparison of luminance (average of three samples of video) with the value of the second sample of that group. V-data is applied to one set of inputs of the U-30/21 adder. L-bar data is applied to the other input with a carry in of one, making the L-bar data the two's complement of L. Thus the operation is a binary subtraction. With luminance subtracted from luminance-and-chrominance (video) the result is chrominance.

11-6 Chroma Memory

See Figure 11-7. Chroma is latched into the D-latch and forwarded to the chroma memory. When the write pulse starts the chroma address register the D-data is loaded into the memory and the previously stored line of data is read out to the C-latch.

L-data from the digital luminance filter is delayed by two clock cycles to match the processing delay of the chrominance subtractor. L-data and C-data are added to produce data representing the composite video signal. The result is routed to the L + C multiplexer/latch as shown in Figure 11-1.

In any group of three sequential samples, four clock pulses are required to derive the values of L and L-bar. Referring to Figure 11-3, at C' time the luminance value for samples A, B, and C is derived. The V-value which is added to L-bar in the chrominance adder is sample B. The next group of samples are labeled A', B', and C'. The luminance value for this group is derived at time C', and the sample to which it is added is sample B'. Thus a sequence of three sample groups, each advanced in time by one clock pulse, is compared with a continuous series of video samples to derive the values of chroma. Although three samples of video are

required to produce a value for luminance, this value is valid only for one specific sample of video. The delayed video which is applied to the chroma adder is a first-in-first-out circuit; therefore, the video sample B is available at time C'.

11-7 Luminance Filter—Low-Pass Characteristic

The digital luminance filter is a band-reject filter and exhibits some of the characteristics of an analog low-pass filter. At the boundary of a sharp transition in values (a gross change occurring between two samples of data) the summation of a group of three samples of video is distorted, and may result in a distortion of the processing chain. One example would be if the transition were from a black color bar to a saturated white color bar. Figure 8-3 illustrates the effect of the low frequency characteristic.

11-8 L + C Overload Limiting. See Figure 11-8. If, as in color bars or split field color bars, a video signal of sharp transition and large change of scalar values is encountered, a high frequency transient is produced which could cause the transition to ring in the bandpass filter of the Video Output PWA.

A worst case example of the error condition and the correction applied by the error detection logic is a transition during a vertical split field. If chroma (two lines past) and luminance (one line past) cross the boundary of a color bar and a white bar, the chroma of the color bar and the luminance of the white bar would be added in the L + C adder. The addition of the two radically different video signals will result in an erroneous digital signal containing black spikes instead of the normal negative excursion of the chroma sine wave.

The L + C multiplexer control logic will provide a limit of all one's for the erroneous addition, and thereby prevent any unsuitable condition in the Video Output PWA. The L + C multiplexer logic and decodes are illustrated in Figure 11-4.

11-9 Chroma and L + C Memories

See Figures 11-7 and 11-8. Nine clock cycles are required to process video data through the dropout compensator circuits. Without this compensation, a horizontal shift of video would occur when stored dropout data is substituted for off-tape video. To correct for this condition, data from the M-latch must be advanced by nine clock cycles toward the write pulse. In addition, the half-cycle subcarrier shift on alternate lines must be reconciled to provide the DOC output M data with the previous line luminance plus chroma of two lines past. The memories and the memory address counters are the same for both the chroma and L + C memories, but the line length counters provide the data manipulation necessary for the delay and alternate line offset.

11-10 Memory Organization and Address Counters. One line of NTSC data (64 μ s) would require 686 8-bit words. The picture video portion of the line, however, uses only 636 words. The chroma and L + C one-line memories use 256 x 4 bit RAM memory integrated circuits (ICs) organized as four 8 x 256-bit partitions. While one line of video needs only three partitions (768 words), the simultaneous write/read serial addressing scheme uses a fourth partition.

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Compare the two memories with their address counters on Figures 11-7 and 11-8. Note that the L + C memory address counter (U72/U63/U54/U44/U43 on Figure 11-8) and the chroma memory address counters (U19 through U37 on Figure 11-7) are exactly the same. Ignoring the line length start and terminate signals for the moment, it can be seen that as long as the 10.7-MHz clock is present the address counters continuously supply a sequence of addresses which advance the partition sequence counter (U36 for the chroma address counter) at the end of each 255 binary address count. The two-bit output of this counter is decoded as OE1, OE2, OE3, and OE4. The partition access code, when applied to a write enable input (pin 20) on the RAMs, provides access to write into the memory in the addressed sequence; when applied to the read enable input (pin 18), it provides access to read data out to the 8-bit C-data latch. The write/read sequence shown in Tables 11-1 and 11-2 for the chroma and L + C memory partition addressing also illustrates how the fourth partition is used for the simultaneous write/read process. The line is read out of memory one partition behind the partition into which data is written.

Table 11-1. Chroma Memory Partition Sequence

Write Enable	Read Partition	Enable	Partition
OE1	U2/U1	OE1	U27/J26
OE2	U27/U26	OE2	U18/U17
OE3	U18/U17	OE3	U10/U9
OE4	U10/U9	OE4	U2/U1

Table 11-2. L + C Memory Partition Sequence

Write Enable	Read Partition	Enable	Partition
WE1	U80/U79	WE1	U71/U70
WE2	U71/U70	WE2	U62/U61
WE3	U62/U61	WE3	U53/U52
WE4	U53/U52	WE4	U80/U79

The picture video line requires only 636 words of the possible 768 words of three partitions. By loading the address counters with a binary 44, each partition advance occurs after 212 address counts. This maintains the write/read partition sequencing but it should be noted in the case of the L + C line length counter that the start of the video line data need not occur with the first memory address (binary 44). The line length counters control the start and termination of the address counter clocks, and the start of the consecutive partition address of the video line in memory may position the data anywhere in the memory.

11-11 Chroma Line Length Counter. See Figure 11-7. The chroma line length counter uses the carry from the two stages of the address counter to advance

another counter (U11) three counts. This produces a line length of 212 counts times three, or 636 clock cycles. At startup the line length carry from U11 will be clocked through the terminate flip/flop U4, to inhibit the address counter clock. This will bring the line count in sync with the address count when the processed write pulse enables the next line. Thus, the chroma line data will always reside in memory across any three partitions with the start of the line always at binary address 44.

The M data consists of chroma from two lines previous and luminance from the previous line. The chroma line length counter is used to manipulate the data to reconcile the subcarrier phase displacement relative to the start of the line initiated by the processed write pulse from the Memory Control PWA. On alternate lines, WA0 (7.8 kHz) is used to preload counter U12 to a 12 or 13 count. The address counter clock from U5-8 is thus inhibited for the 3- or 2-clock cycle period needed to lock the U12 carry output high. This re-times the chroma processing to make the previous line chroma phase consistent with the current line luminance.

11-12 L + C Memory Line Length Counter. See Figure 11-8. The L + C line length counter is used to advance the M data read toward the processed write pulse to compensate for the nine-cycle delay through the dropout compensator processing. Also, the output M data must be consistent in chroma phase relative to the write pulse on alternate lines to reproduce the half-cycle subcarrier shift.

The processed write pulse from U6-5 initiates the L + C line counter (U59, U68, U78, and U85). The line counter operates independently of the address counter and the start/terminate output at U85-9 merely inhibits or enables the address counter clock. Thus the start of the data line is not coincident with any particular memory address and will advance across partition boundaries as the line length counter manipulates the data. The address counter of the L + C memory stops at the termination of the line length counter, but is not reset. At the start of the following line the address count is continued until the line terminates again. By this means, the last address of the L + C line is advanced nine words past the number of words stored in the memory, and data read-out is advanced by nine clock cycles. Thus data from the M-latch is matched to A/D input data in reference to the write pulse, and there is no horizontal offset of substitute data during a dropout condition.

Note that the line length counter is loaded to binary 3451 by the processed write pulse start. At the final carry from U78 at binary 4096 the counter will have been counting a total of 645 clock periods. This means that the address counter has produced the normal line 636 addresses plus nine. The address counter of the L + C memory stops at the termination of the line length counter, but is not reset. At the start of the following line the address count is continued until the line terminates again. By this means, the last address of the L + C line is advanced nine words past the number of words stored in the memory, and data read out is advanced by nine clock cycles. Thus data from the M-latch is matched to A/D input data in reference to the write pulse, and there is no horizontal offset of substitute data during a dropout condition.

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In the main TBC memory the hue of the video data does not shift because the phase of chroma relative to burst is entered into memory intact. However, the half-cycle of subcarrier phase shift per line must be accounted for in the manipulation of the processed dropout data to avoid a sawtooth effect at the edge of the screen during multiline dropouts. To accommodate the alternate line subcarrier phase shift the line length counter preload is shifted from 3451 to 3453 by the 7.8-kHz WA0 signal. This advances the L + C line by two clock cycles, so that as the L + C data is read out the subcarrier shift and the processor delay both will be reconciled.

11-13 Dropout Detector Circuit

See Figure 11-9. The dropout detector circuit receives information from three sources:

- Gated dropout pulse from the Tape VCO PWA
- Rf in from a heterodyne VTR
- Head switch dropout from the VPR which inhibits dropout operating during the vertical interval.

The high HET/NORMAL signal from the mode switch in heterodyne mode inhibits the gated dropout pulse signal and enables the rf detector. It also inhibits the head switch dropout gate in heterodyne mode. When the mode switch is in the normal position the reverse of these conditions is true. Jumper J2 is also used to enable or inhibit the PWA dropout detector. Jumper position A-B inhibits the PWA dropout detector and enables the VPR-2B or VPR-3 originated gated dropout entering the PWA at pin 56. For use with VTRs that do not supply a dropout pulse, jumper J2 is placed in position A-C. This places a high on pin 12 of gate U25-11 thereby enabling the rf detector and also disabling the gated dropout pulse.

The pulse stretcher extends the dropout signal for the input multiplexer by an additional 10 μ s after the end of a dropout detection. The quality of the off-tape video is not fully restored immediately after the end of the dropout. The stretched pulse is, therefore, required to extend to the replacement period.

11-14 MAINTENANCE

See Figure 11-11 in this section for the component locator diagram, jumper, test-point, and adjustable components summaries, and the waveforms called out in these procedures.

Before undertaking any adjustments to the S/P Converter PWA review the system alignment procedures of Table 3-2 and the tape/reference test loop discussion of paragraph 3-6, Part I, for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the S/P Converter PWA and interactive functions between it and other PWAs before making any adjustments.

11-15 Dropout Test—VTRs with TTL Dropout Pulse

This test requires a dropout test tape (See Table 3-1).

- STEP 1** Verify operation of dropout compensator option in normal speed playback.
- Switch DOC option off with the DOC ON/OFF switch on front edge of S/P Converter PWA 7.
 - Play back special dropout tape. A dropout will appear in the picture.
 - Switch DOC on (DOC ON/OFF PWA 7). The dropout noted in step 1b should be removed.

Note

Some marks around the dropout area may show—this is normal.

- STEP 2** Play back tape in STILL FRAME and SLOW MOTION. Repeat observations of step 1c.

Note

Special dropout tapes are intended only for use in the procedure given above. Use of this tape for other purposes is not recommended.

11-16 Rf Dropout Level Adjustment

The rf dropout detector is used for the Ampex VPR-20, heterodyne, and other VTRs which do not supply a TTL dropout pulse. The rf dropout detector is calibrated at the factory for optimum dropout recovery and only the level may need adjustment for particular VTRs. More elaborate adjustment is given in the next paragraph. This procedure uses the programmed dropout test tape listed in Table 3-1.

Note

If a dropout test tape is not available, a 20-dB pad inserted in the line to the RF IN jack may be used to simulate a typical dropout level.

Adjust R24 during normal playback of color bars for disturbance in the picture with pad installed, then remove pad and verify a normal picture.

- STEP 1** Verify that jumper J2 is in A-C position (rf dropout enable).
- STEP 2** Switch dropout compensator (DOC) off (S1, PWA edge).
- STEP 3** Play dropout tape at normal speed and observe two small dropouts near the top and bottom of the picture and a large dropout in the center.
- STEP 4** Switch DOC on. Dropouts observed above should be removed.

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STEP 5 If dropouts are not removed or other picture disturbance indicates an incorrect dropout level, adjust R24 (rf DO level—PWA edge) for a stable picture.

11-17 Rf Dropout Detector Adjustment

This procedure may be used in lieu of a programmed dropout test tape.

Note

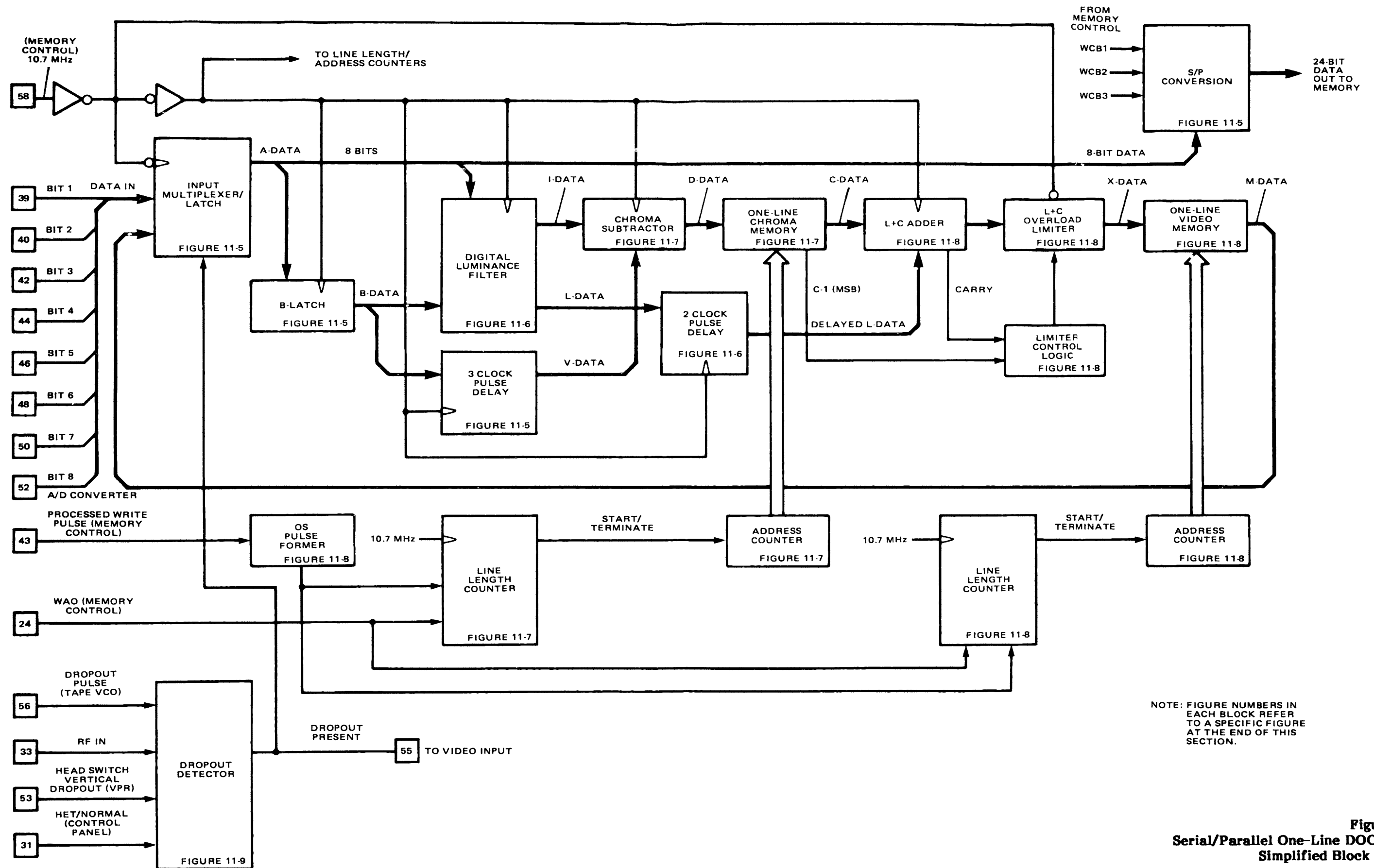
Because of noise and crosstalk with the PWA on the extender, adjustment results here should be rechecked with the PWA in the card rack.

STEP 1 Rf threshold and amplifier gain adjustment:

- a. Verify that jumper J2 is in the A-C position (rf dropout enable).
- b. Connect oscilloscope as follows: CH1—PWA 2, TP1 (tape video input); CH2—PWA 7, U7-7 (rf comparator output). Trigger on internal.
- c. Disconnect TAPE VIDEO IN on back panel to remove the rf source.
- d. With video input disconnected, adjust R24 (AGC level) for a transition from low to high. Signal should remain high. Signal at TP5 should be less than the dc voltage at the junction of R13 and R4 (threshold level).
- e. Connect oscilloscope as follows: CH1—PWA 2, TP5 (tape video input). CH2: PWA 7—TP5 (rf amplifier output). Trigger on PWA 7 pin 24 (WA0).
- f. Connect a tape video source to TAPE VIDEO IN connector.
- g. Adjust oscilloscope time base to view horizontal sync time period. (Rf is lowest in frequency at this period.)
- h. Adjust R44 for 500 mV of rf at TP5. The signal is very noisy. See Figure 11-10, waveform 56 (S).
- i. Connect oscilloscope as follows: CH1—PWA 2, TP1 (tape video input). CH2—PWA 7, U24-12 (rf detector one-shot). Trigger, PWA 7 pin 24 (WA0).
- j. With video input connected, view horizontal sync time period. Adjust R25 until pulses appear. Readjust until pulses disappear and signal on U24-12 is a continuous low. The object is to make time-out of the retriggerable one-shot slightly longer than the period of 1 Hz of the lowest frequency of rf.

STEP 2 Pulse stretcher adjustment:

- a. Connect oscilloscope as follows: Channel A—U24-4 (pulse stretcher one-shot). Trigger on PWA 7 pin 24 (WA0).
- b. Adjust R29 (pulse stretcher adjustment) for a negative-going pulse of 9.0 to 9.2 μ s.



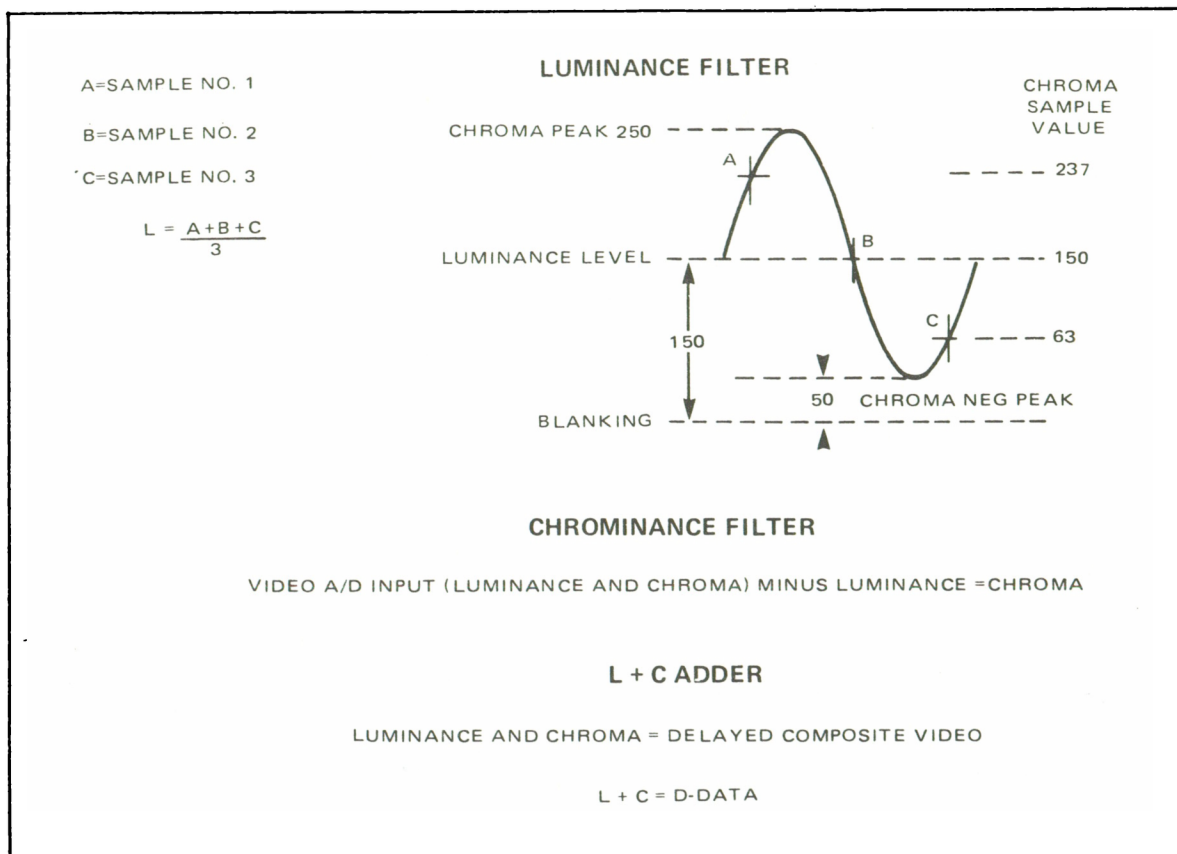


Figure 11-2. Digital One-Line Delay Equations

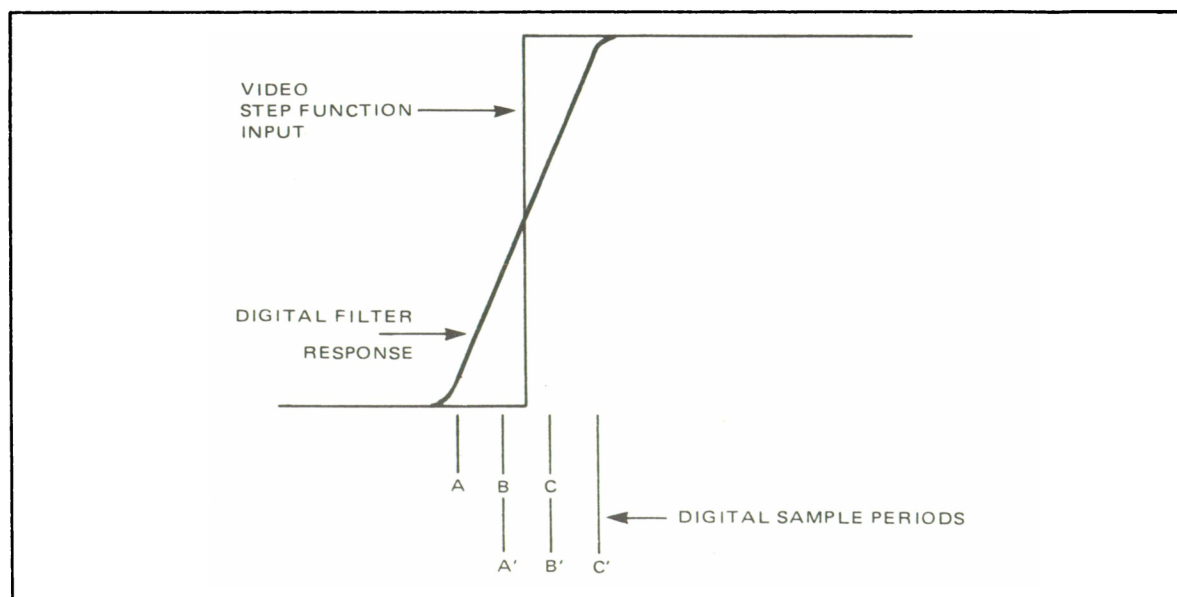


Figure 11-3. Digital Luminance Filter Sample Timing and Transient Response

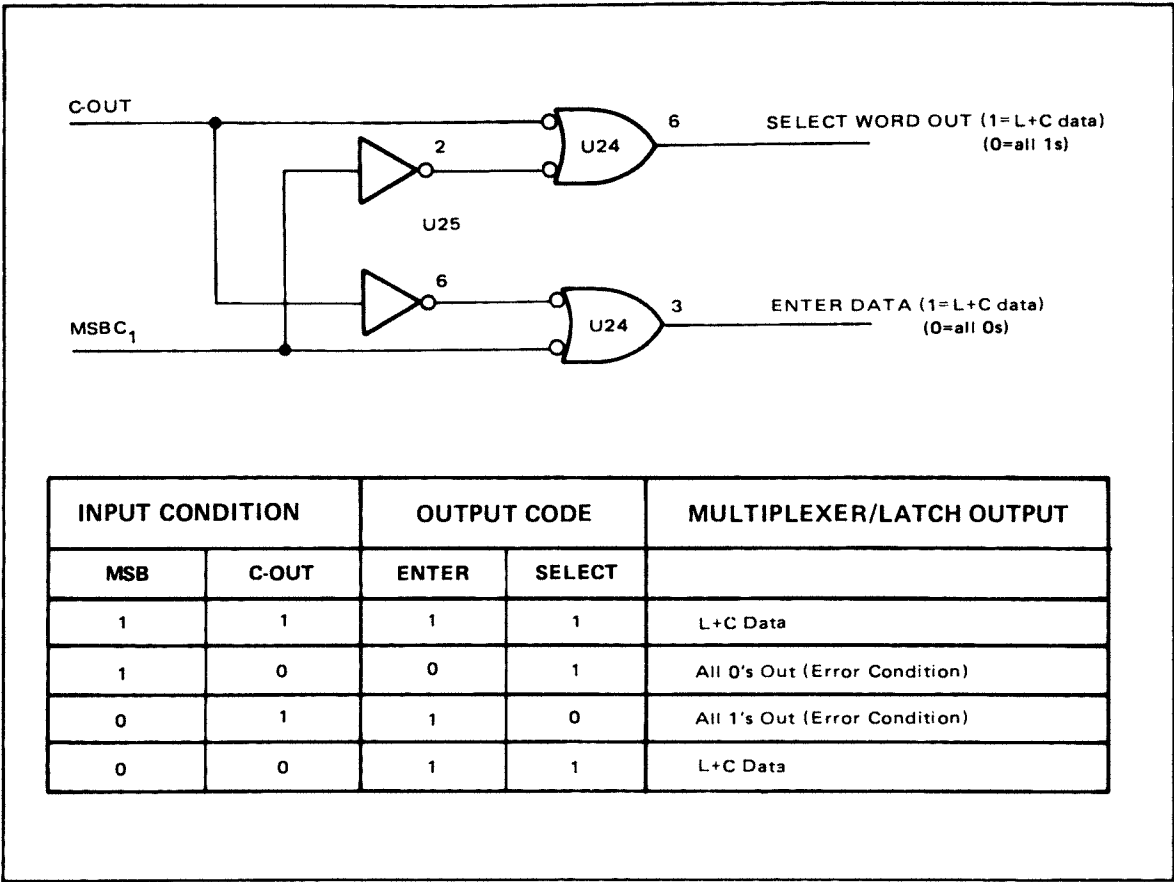


Figure 11-4. Multiplexer Control

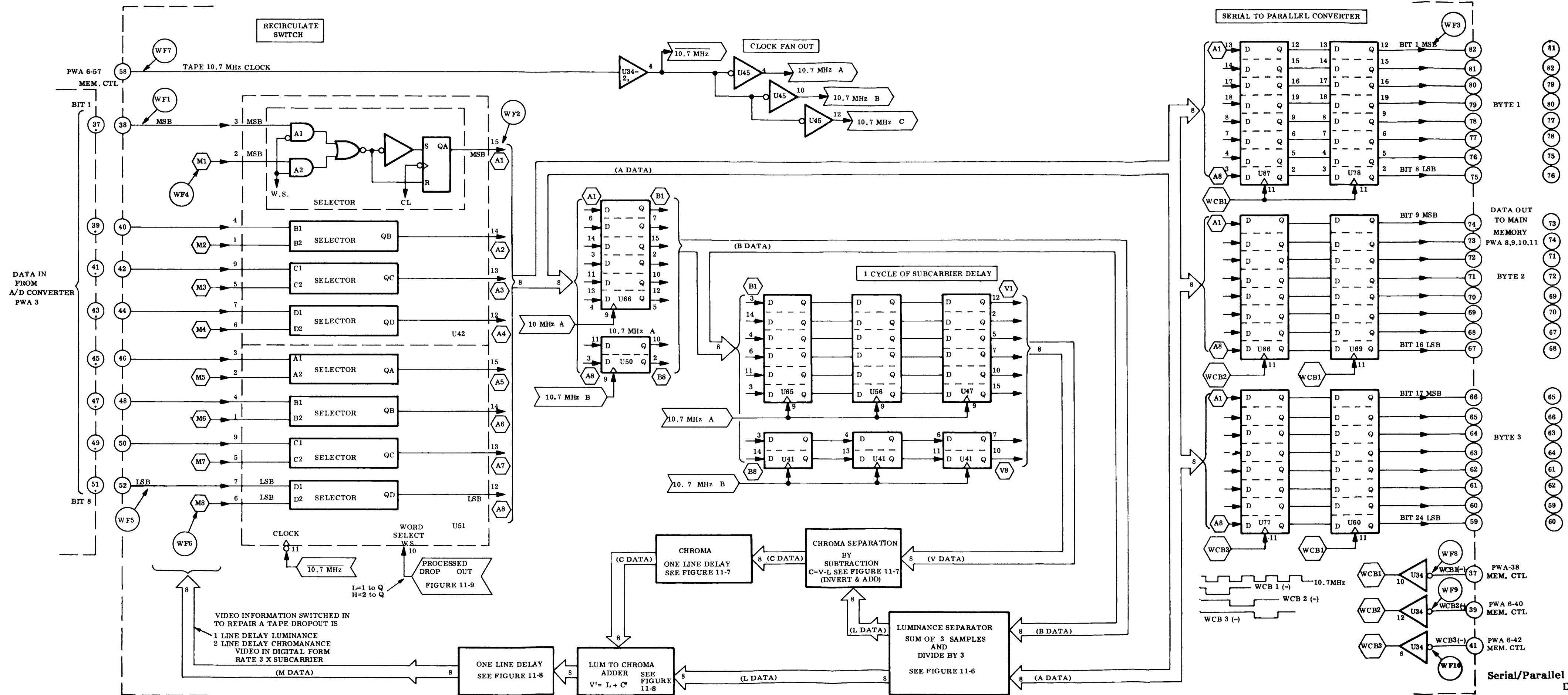


Figure 11-5.
Serial/Parallel One-Line DOC PWA 7,
Detailed Block Diagram

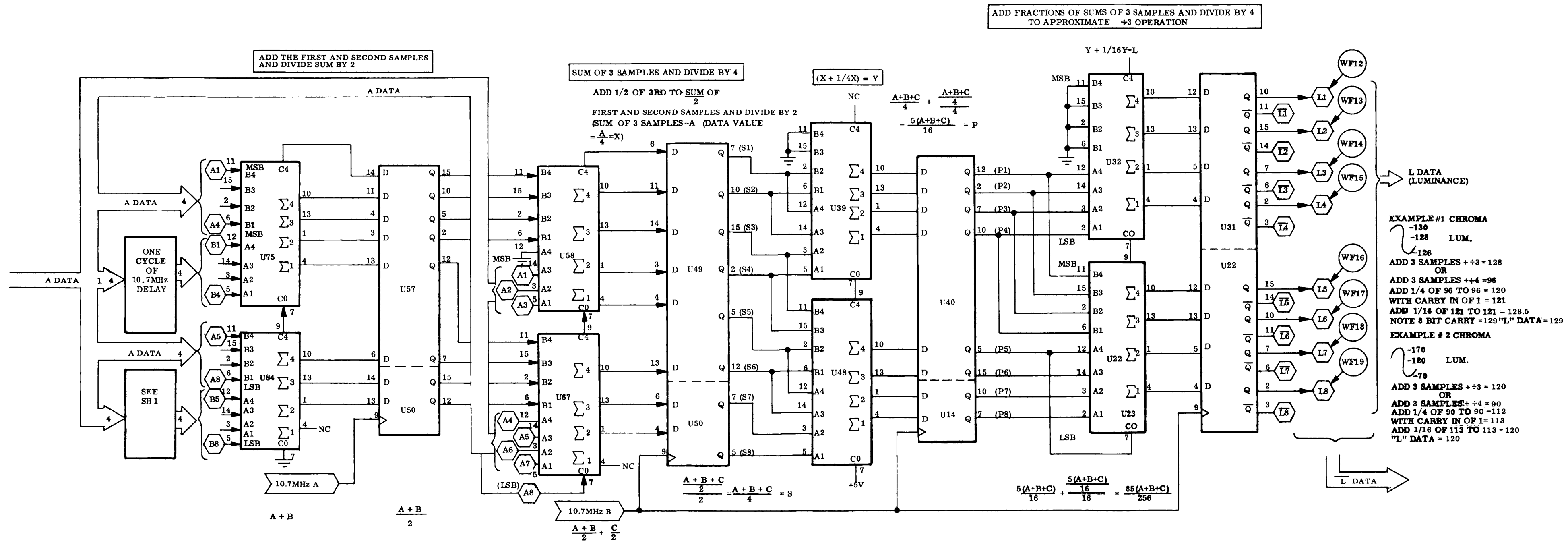


Figure 11-6.
Luminance Filter Simplified Schematic,
Serial/Parallel One-Line DOC PWA 7

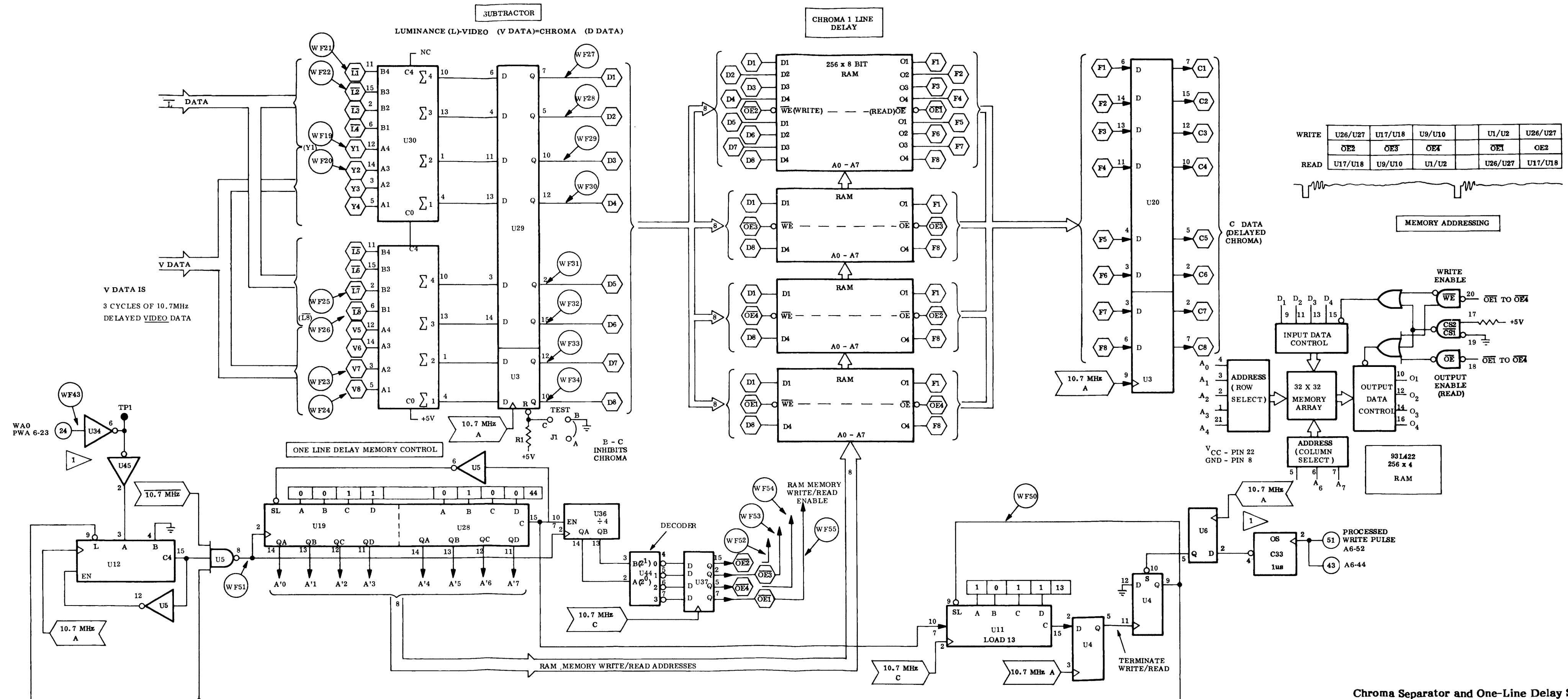


Figure 11-7.
Chroma Separator and One-Line Delay Simplified Schematic,
Serial/Parallel One-Line DOC PWA 7

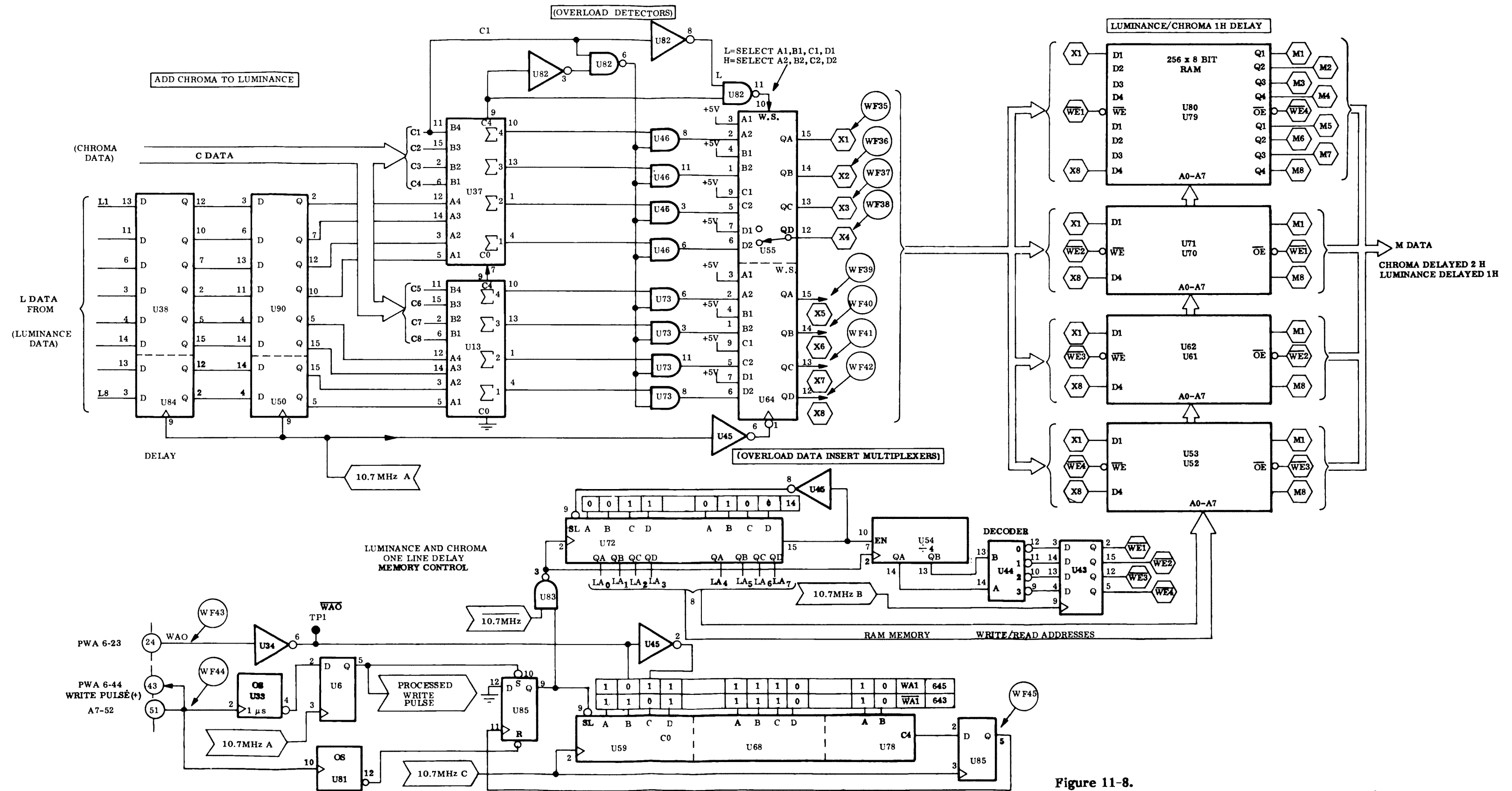
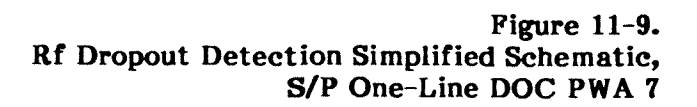


Figure 11-8.
Delayed Chroma to Luminance Adder and One-Line Delay
Simplified Schematic, Serial/Parallel One-Line DOC PWA 7



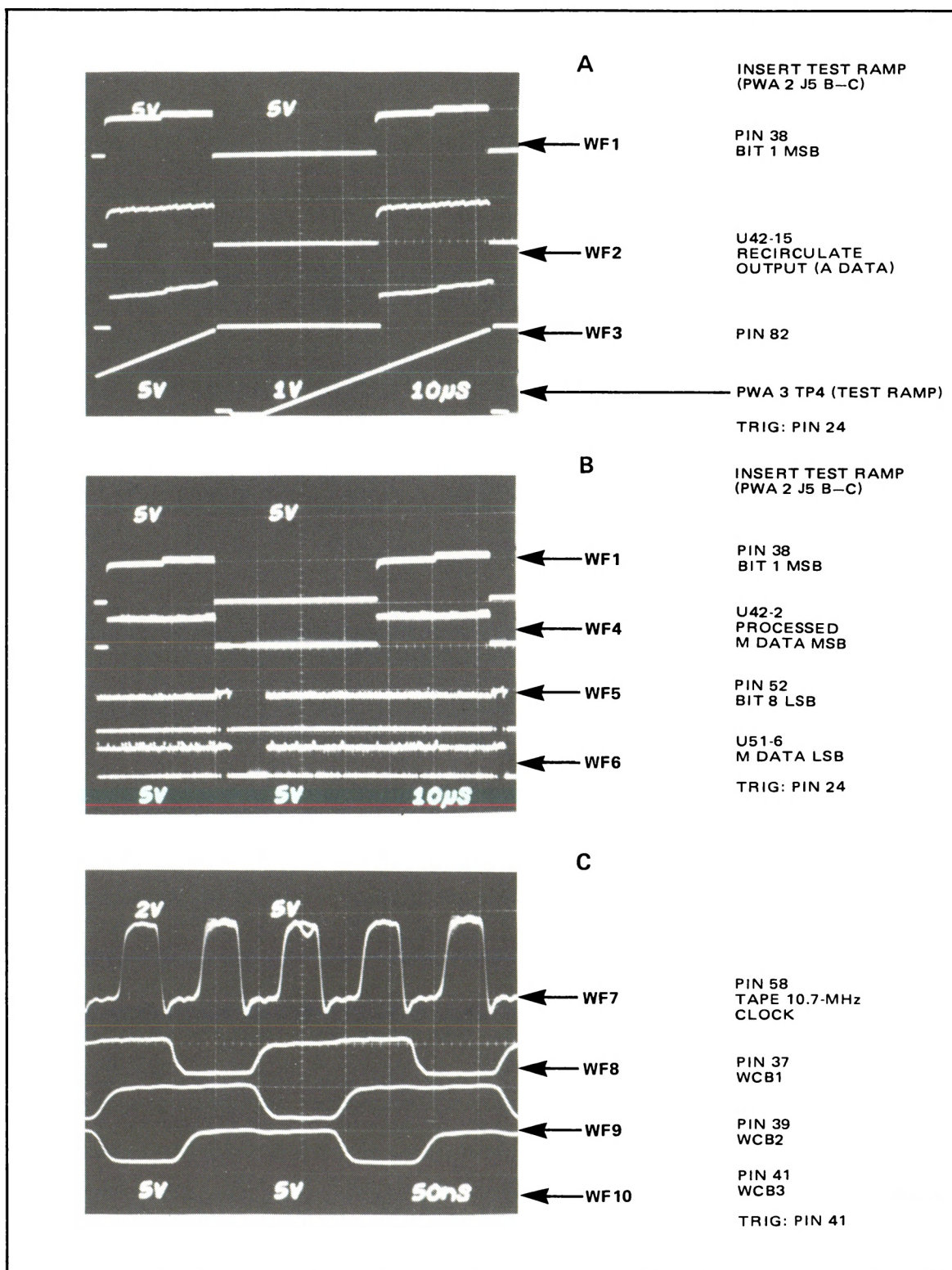


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 1 of 6)

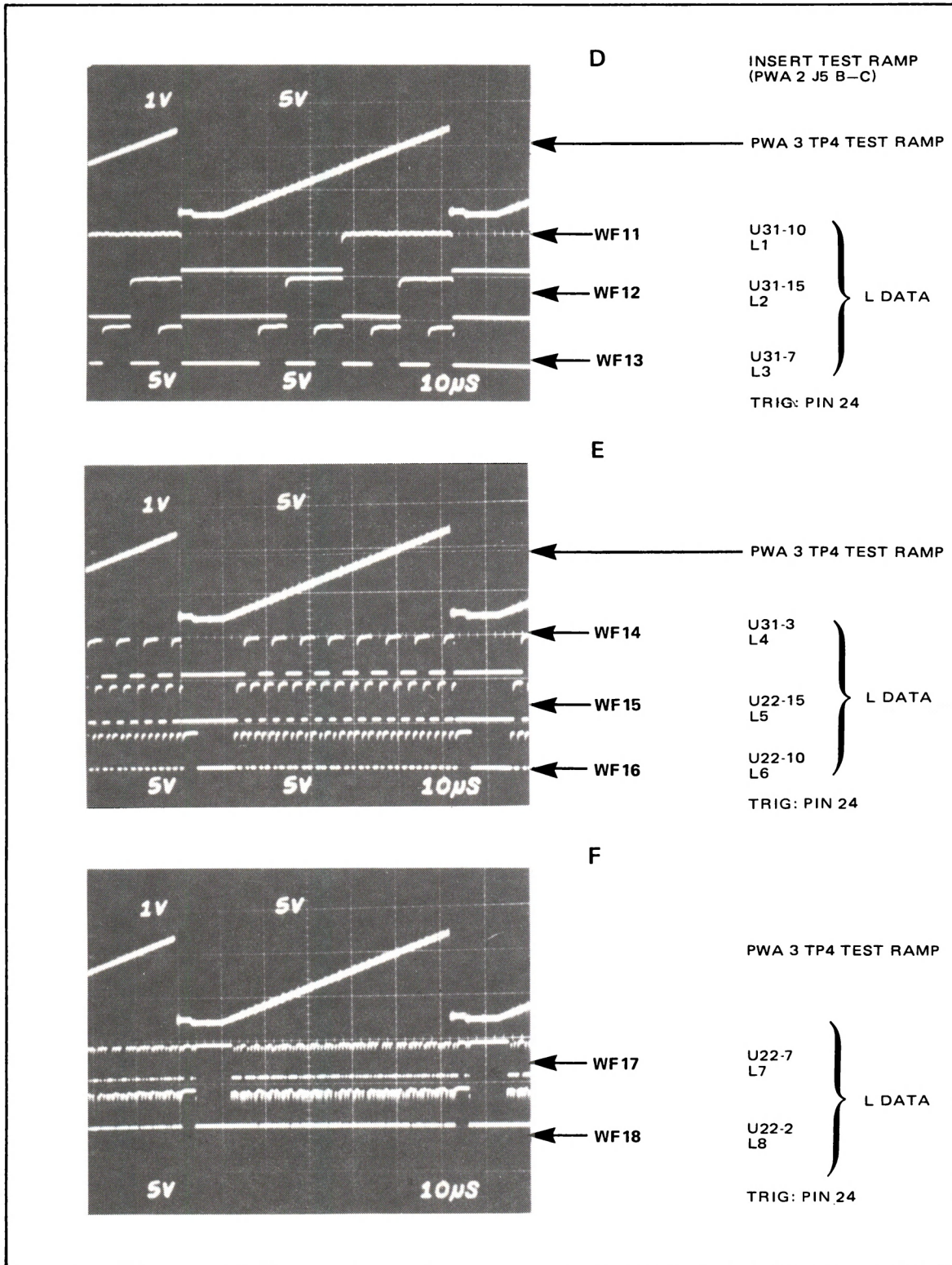


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 2 of 6)

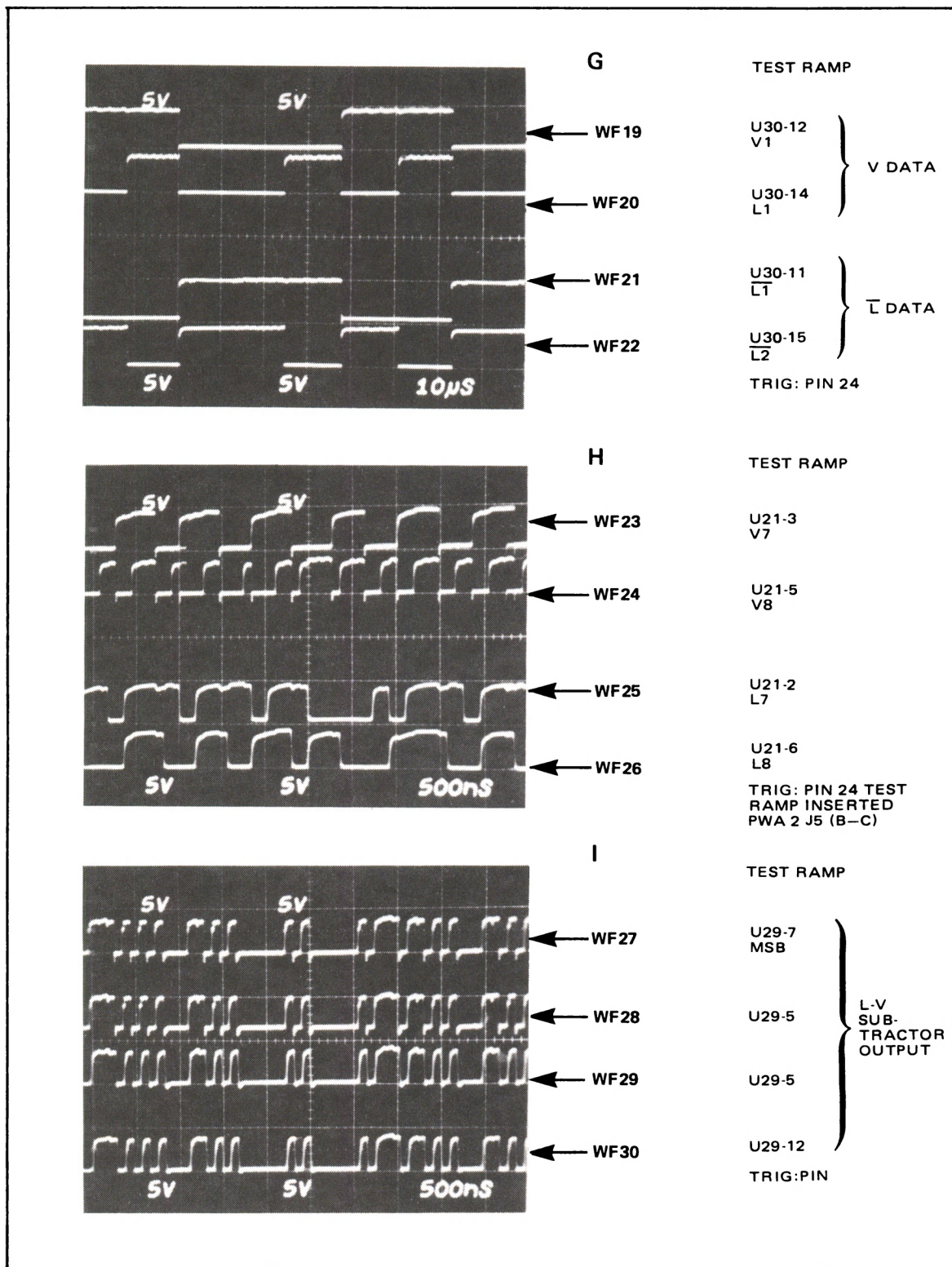


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 3 of 6)

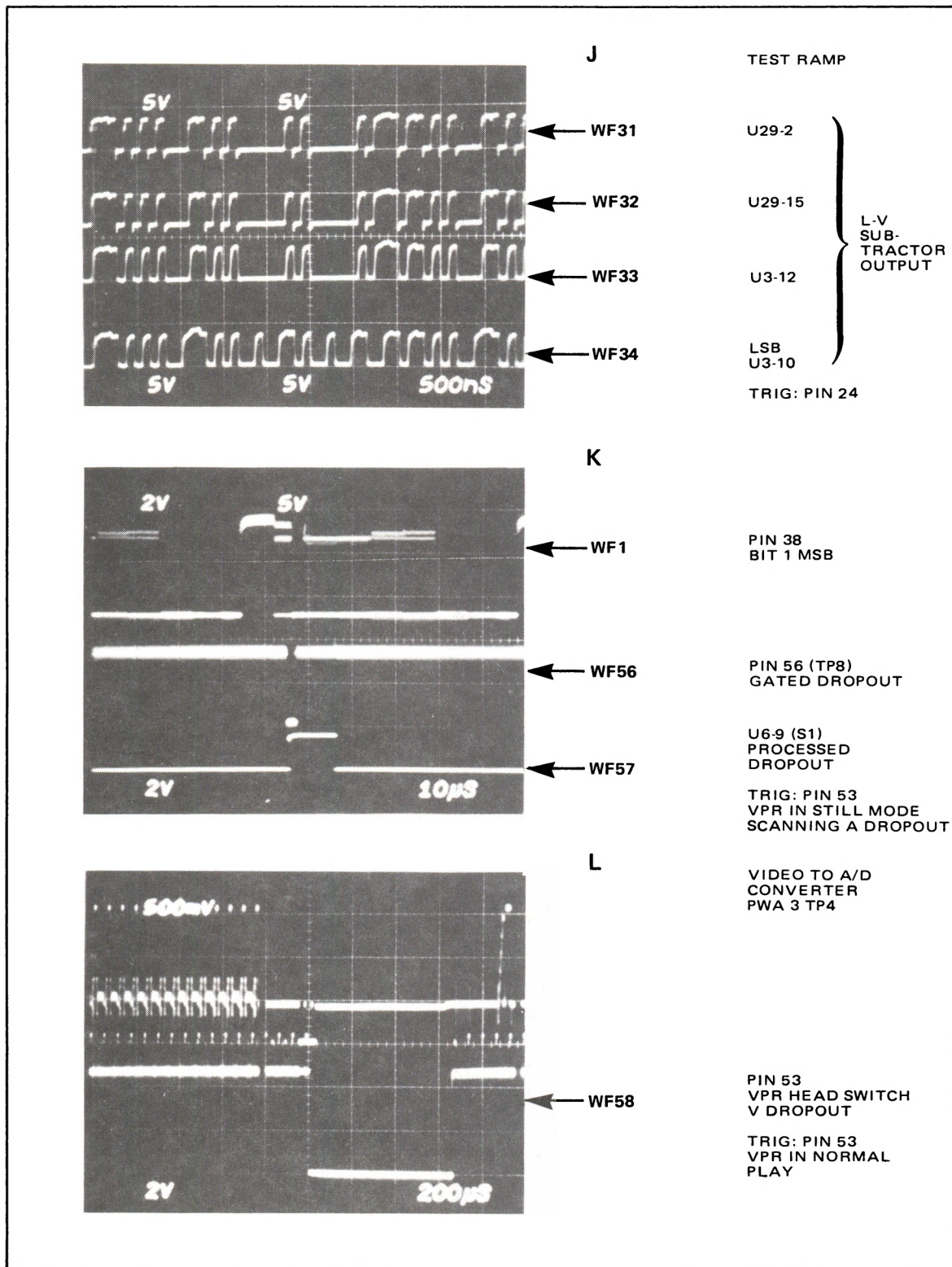


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 4 of 6)

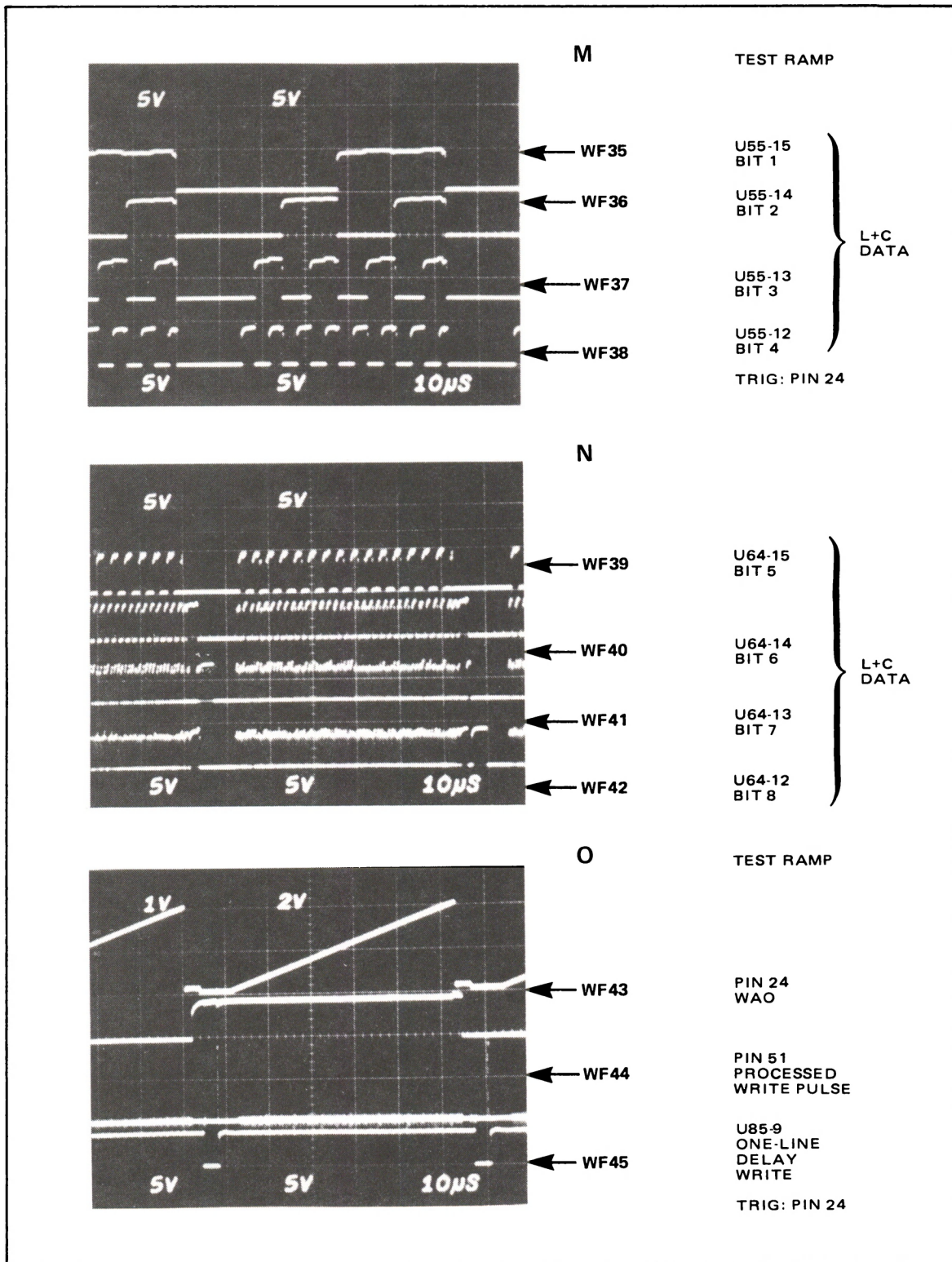


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 5 of 6)

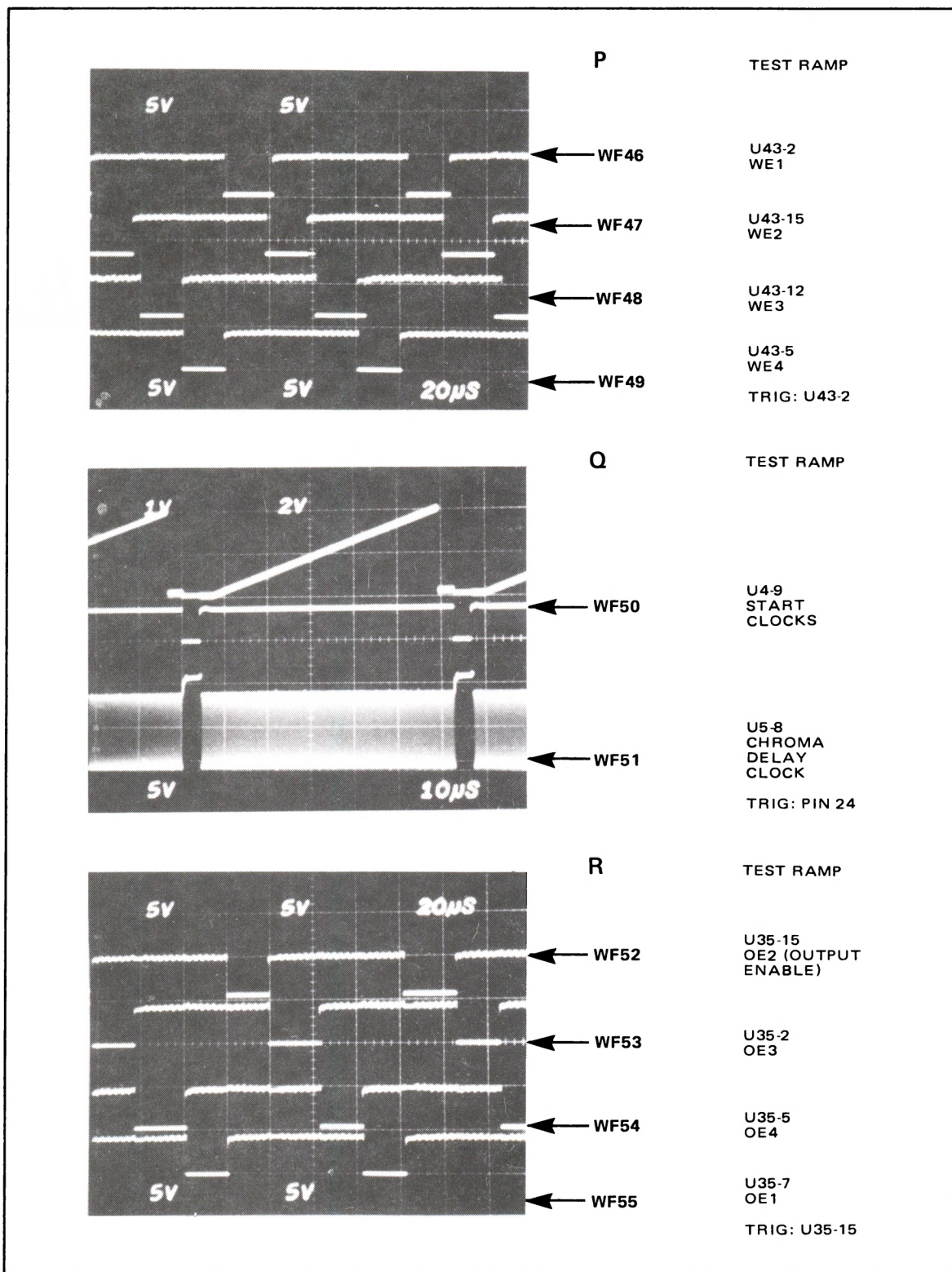
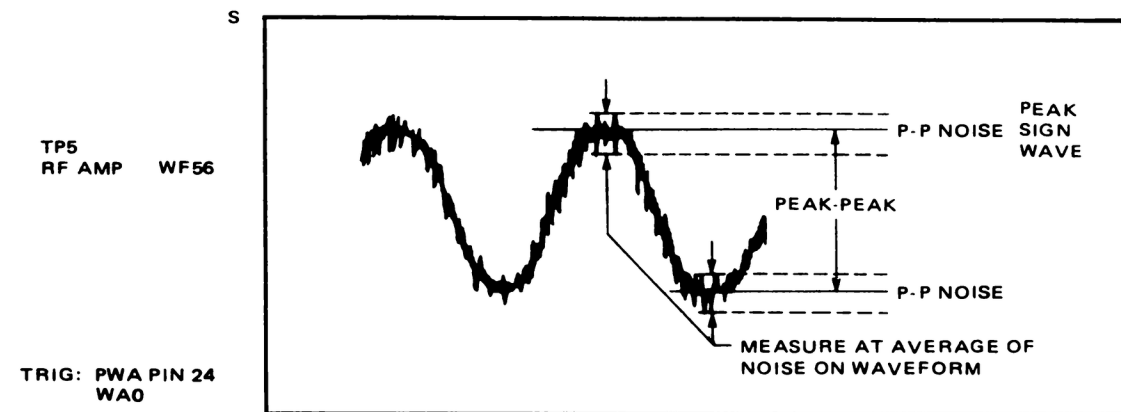


Figure 11-10. S/P Line DOC PWA 7 Waveforms (Sheet 6 of 6)

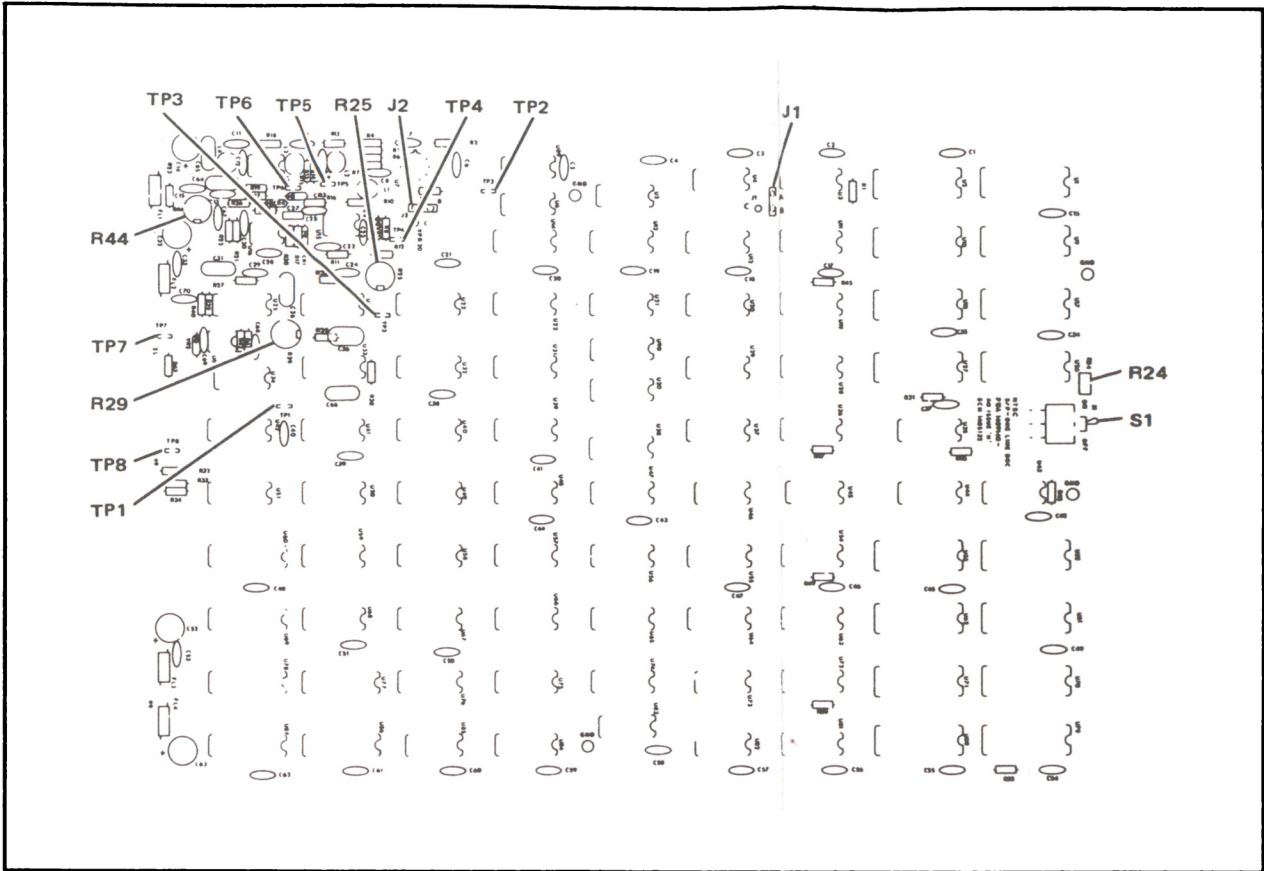


PWA 7 Test Points

Test Point	Name
TP1	Write address zero (WA0)
TP2	Dropout present
TP3	Duration
TP4	Discriminator output
TP5	Gain controlled amplifier output
TP6	AGC amplifier output
TP7	RF input
TP8	TTL dropout pulse

PWA 7 Adjustable Components

Component	Function
R24	AGC level
R25	Duration
R44	Forward gain
R29	Dropout pulse stretcher
S1	DOC on/off



PWA 7 Component Locator

PWA 7 Jumpers

Jumper	Position	Function
J1	A-B B-C	Factory Test Normal Test Data Disable
J2	A-B A-C	Dropout Select Normal. Inhibits PWA 7 onboard dropout detector. VPR-2B, VPR-3, Heterodyne use. Inhibits VTR dropout command and enables PWA 7 on-board dropout detector. VPR-20 use.

Figure 11-11.
Test Points, Jumpers, Adjustable Components, Component
Locator, S/P One-Line DOC PWA 7

PART II

SECTION 12

MEMORY PWA 8,9,10,11

DESCRIPTION AND MAINTENANCE

12-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1463574
Schematic No. 1402383

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 12-3, simplified block diagram
- Figure 12-4, detailed block diagram
- Figure 12-5, maintenance data

Memory PWA 8, 9, 10, and 11 function summary:

- Memory stores 12 or 16 H-lines of 24-bit data. PWA 8 stores lines 1—4; PWA 9 stores lines 5—8; PWA 10 stores lines 9—12, and PWA 11 (if used) stores lines 13—16. Write timing is synchronous to tape timing; read timing synchronous to reference video.

12-2 DESCRIPTION

Memory PWAs 8, 9, 10, and 11 (if used) are 12-line (or 16-line) storage mechanisms for quantized digital video signal from Serial/Parallel One-Line DOC PWA 7. Control of data in and data out of memory is under the direction of Memory Control PWA 6. Digital data is time-base corrected by storing and accessing 24-bit data words in the Memory PWAs under control of separate read and write timing and addressing signals from the Memory Control PWA. Each Memory PWA is identical and each provides storage for four horizontal lines.

Three 8-bit words in a 24-bit parallel data format are presented to the input of the memories. The 24-bit words are clocked into a given line of memory at Fsc rate by a two-phase clock synchronized with tape-derived Fsc signal from the Memory Control PWA. They are later clocked out of memory at an Fsc rate which is slaved to the station master sync generator. This process is the time-base correction of errors recorded on the tape or errors caused by operation of the playback mechanism.

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12-3 Memory Shift Registers

Each line of memory is made up of six 1024-bit dynamic shift registers. Each register is organized as four 256-bit shift registers. Each 256-bit register is further configured as two parallel registers, with $\Phi 1$ clock entering the first bit of data into one of the parallel registers, and $\Phi 2$ clock entering the second bit of data into the other parallel register. The third bit is entered into the first of the parallel registers by the next $\Phi 1$ clock, the fourth bit of data into the second parallel register by the following $\Phi 2$ clock, etc., until all 256 bits have been shifted. In the read cycle, the data will be shifted out in the same order, first-in, first-out. See Figure 12-1.

12-4 Memory Organization

The 24-bit data words are presented to all 12 or 16 lines of memory in parallel. Figure 12-2 shows the memory organization of the 12-line system. However, only the line currently addressed by the Memory Control PWA will have its write gates enabled. Memory logic decodes WMA-WA0-WA1 as line 1 address on PWA 8. See Figure 12-3.

The next event in the WMA-WA0-WA1 sequence will be decoded as line 2. The next as line 3, then line 4. In the following sequence WMB-WA0-WA1 will sequentially address lines 5, 6, 7, and 8 on PWA 9, WMC-WA0-WA1 will address lines 9, 10, 11, and 12 in similar fashion.

The read decode logic will access line 1 of PWA 8 with RMA-RA0-RA1. In a manner similar to the write address it will access lines 2, 3, and 4 in sequence. RMB-RA0-RA1 will sequentially access lines 5, 6, 7 and 8 on PWA 9 and lines 9, 10, 11 and 12 will be accessed by RMC-RA0-RA1.

With a six-line difference in location, as data is written into memory, previously written data is simultaneously read out of memory; i.e., as line 6 is written, line 1 is read, then line 7 is written while line 2 is read, etc., until line 12 is written while line 7 is read. Then line 1 is written as line 8 is read and so on. The Memory Control PWA maintains the six-line difference in the read/write relationship to avoid a coincident read-write operation on a line. Although the shift register could clock data in and out of the register simultaneously using the same clock, the TBC, even in normal play, does not operate the read clock and the write clock with exact coincidence; therefore a simultaneous read-write on a line would thoroughly scramble the data.

All the most significant bit outputs of the shift registers are wire-ORed together on a given memory PWA to a bit-1 driver gate. Bit 2 is similarly wire-ORed to a bit-2 driver gate, and so on, to bit 24. Outputs of the bit-1 driver gates of PWA 10 and 11 are wire-ORed by the motherboard. Bit-2 driver gates of PWA 9, 10, and 11 are similarly wire-ORed, and so on, to bit 24. See Figure 12-2.

12-5 Dual Load

Of the 12 lines in memory, the read function for a given read timing decode (i.e., RMA line 1) will lag the corresponding write timing decode (WMA line 1) by six lines. As an example, if PWA 8 line 1 is being loaded, then PWA 10 line 2 is being

read or unloaded. If tape speed is such that a possibility exists for any given line to be simultaneously accessed for write and read function, an overload signal will be generated. The Memory Control PWA will advance or retard the write address counter two lines to correct for the timing discrepancy. Since this would leave two lines of data empty (white bar on screen), the dual load signal is sent to the write clock decoder in the memory. If line 3 is accessed, lines 1 and 3 are loaded in parallel. When line 4 is accessed, lines 2 and 4 are filled in parallel. The dual load is removed and normal sequencing is resumed until another overload is generated.

12-6 MAINTENANCE

There are no adjustments on the Memory PWAs. Refer to paragraph 3-21 for notes on fault isolation.

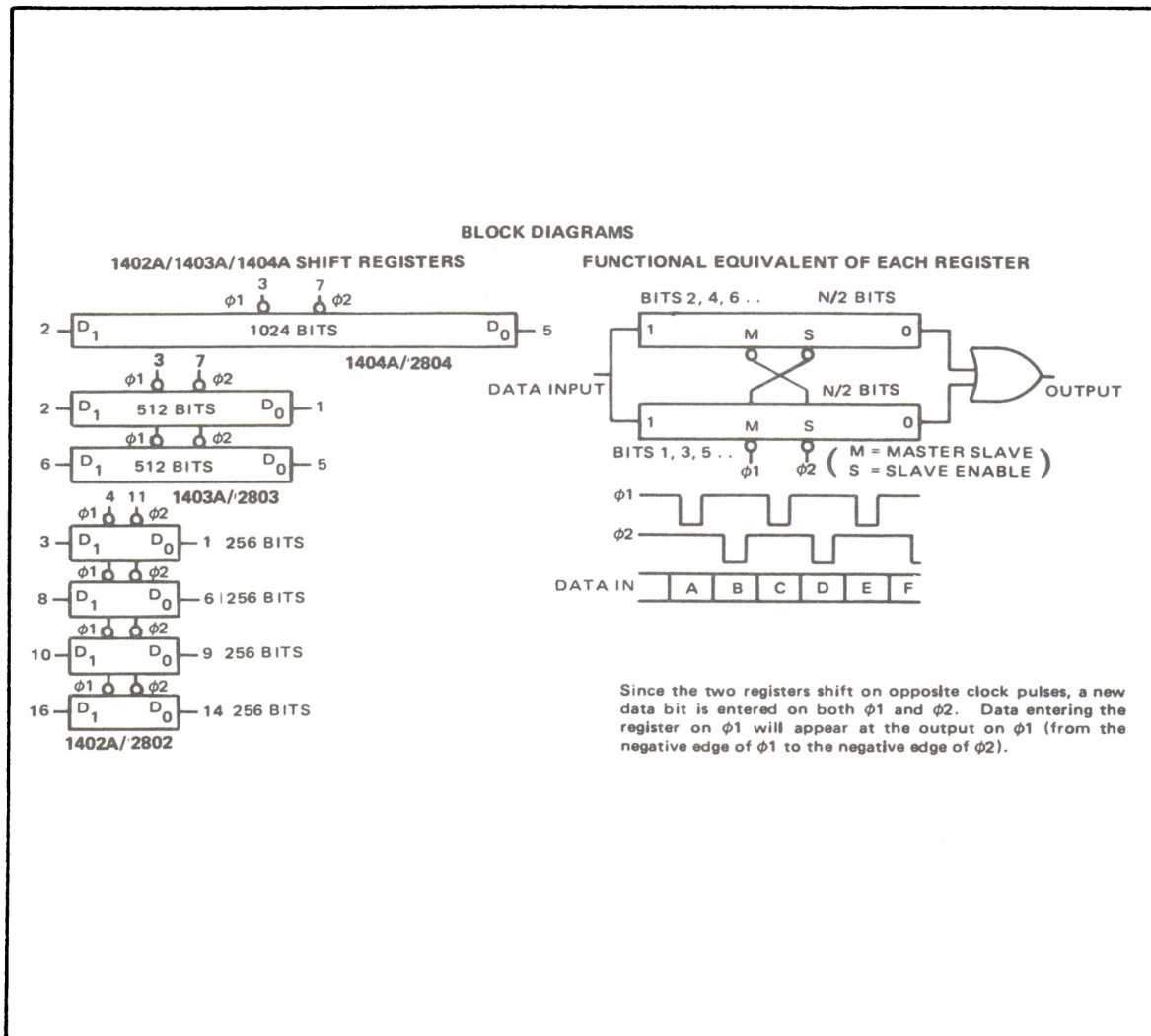


Figure 12-1. Shift Register Block Diagram

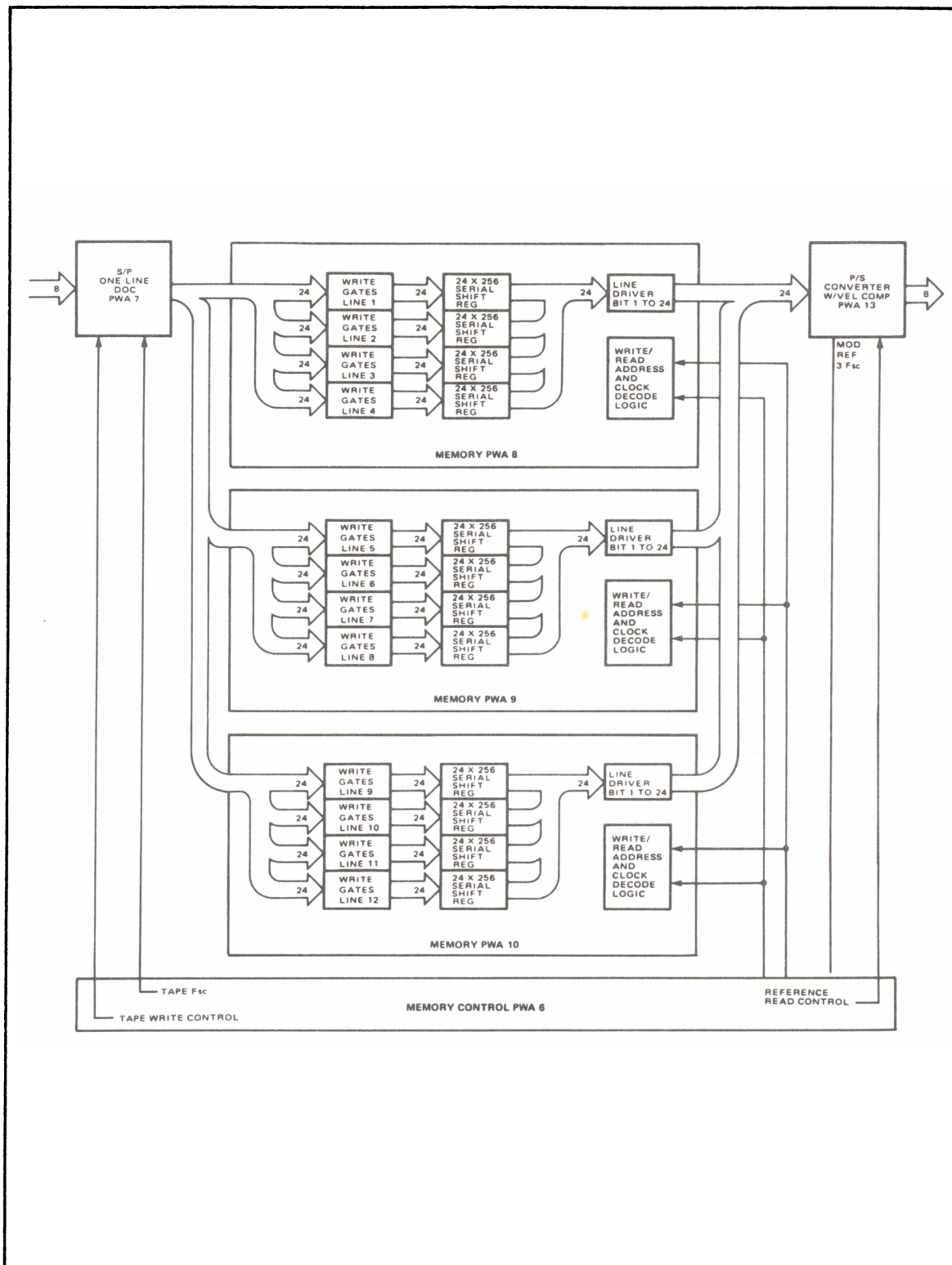


Figure 12-2. 12-Line Memory Organization Simplified Block Diagram

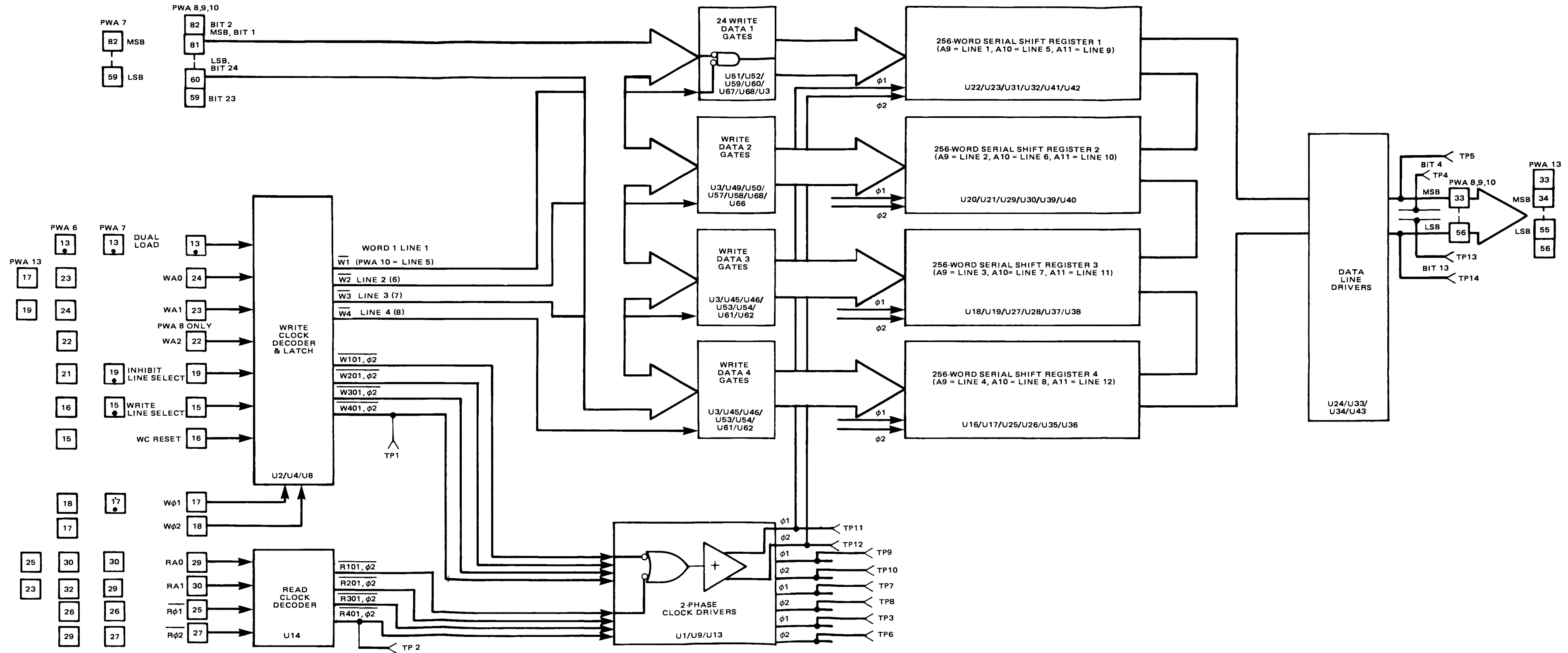
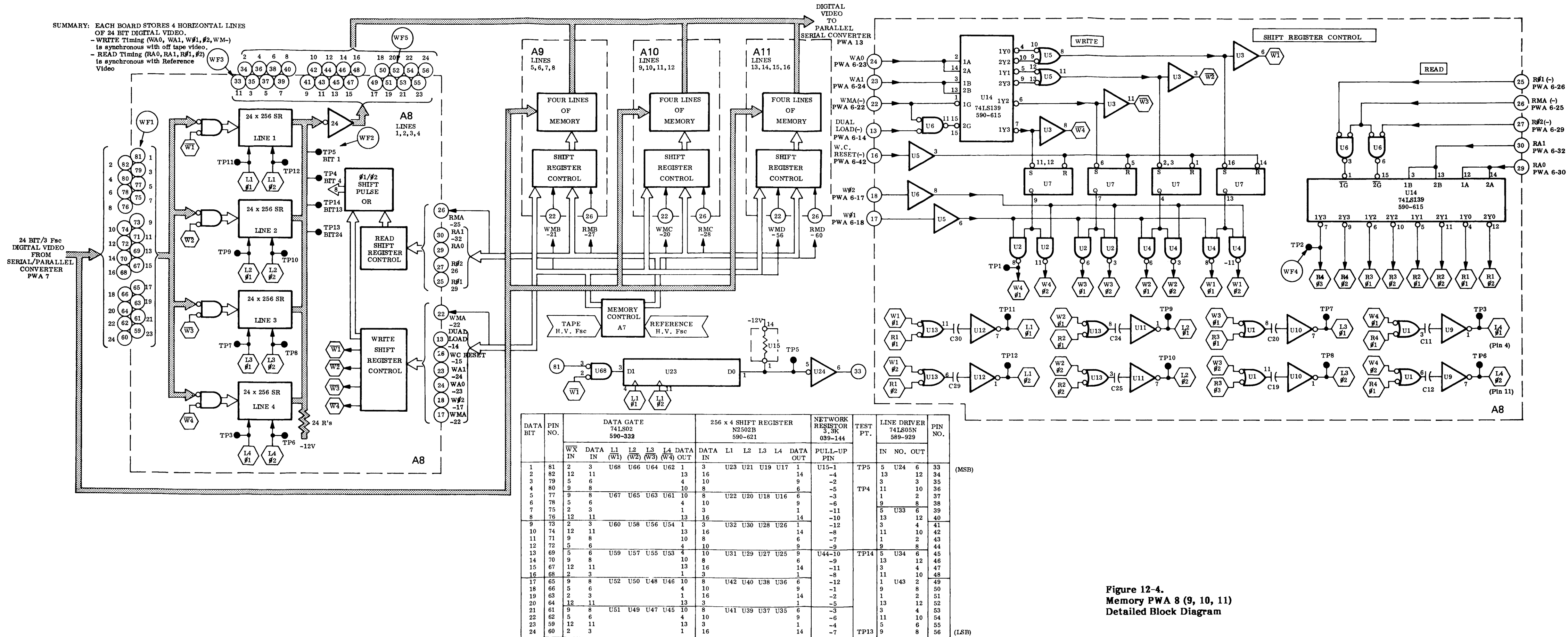


Figure 12-3.
Memory PWA 8 (9, 10, 11) 12-Line
Simplified Block Diagram



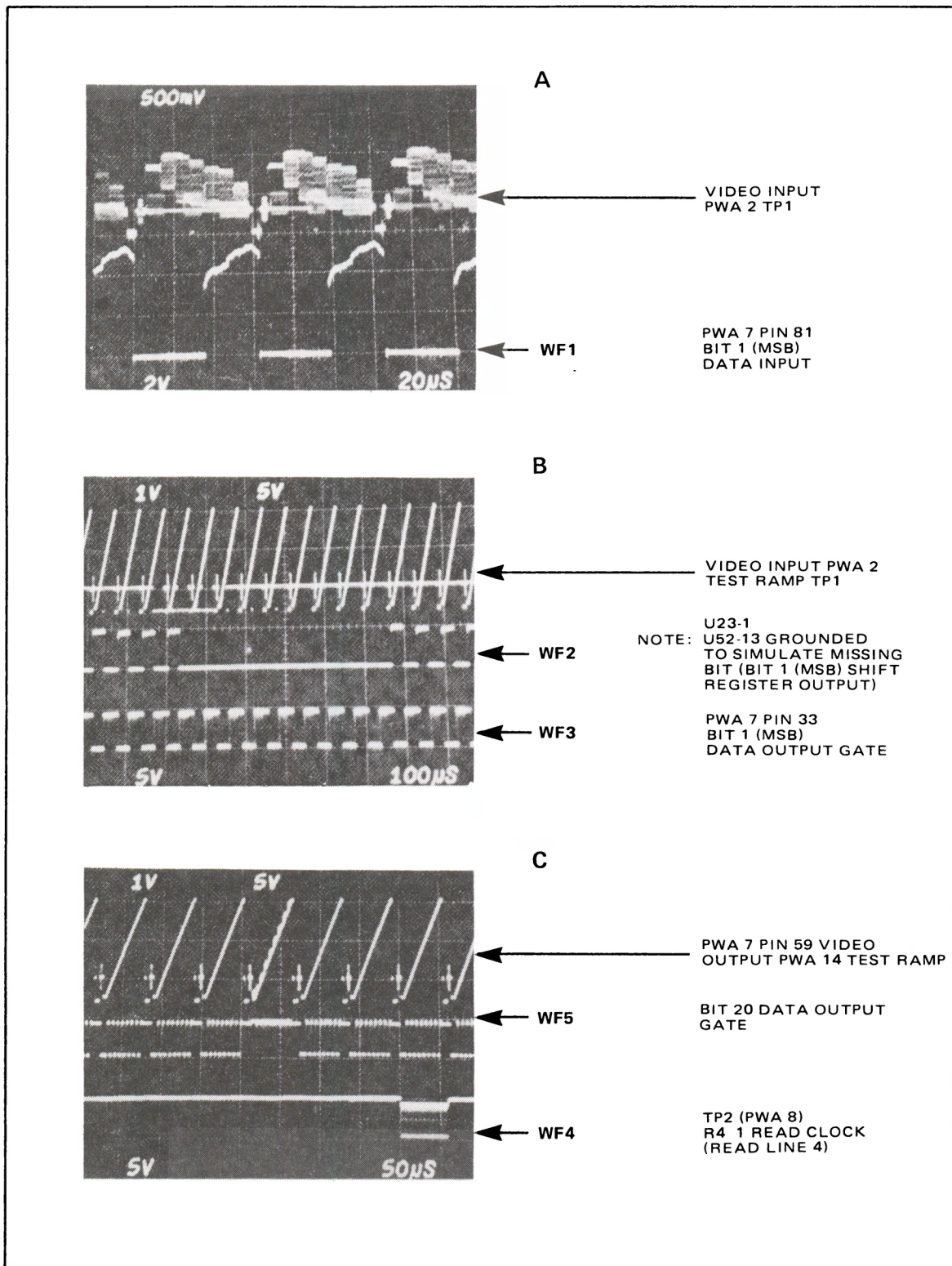


Figure 12-5. Waveforms (Sheet 1 of 2)

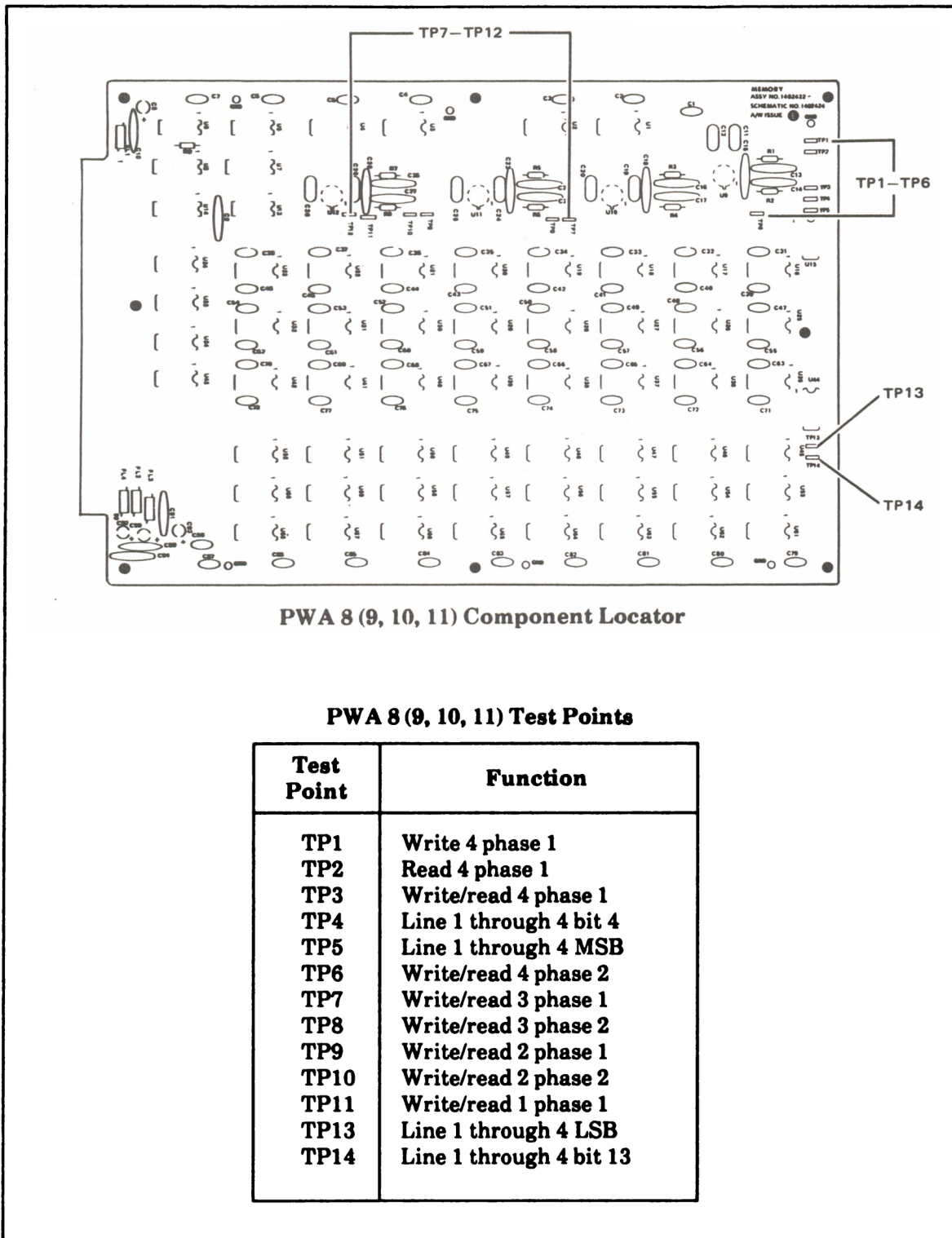


Figure 12-5. Test Points, Component Locator, Memory PWA 8 (9, 10, 11)
(Sheet 2 of 2)

PART II

SECTION 13

PARALLEL/SERIAL CONVERTER W/VEL COMP PWA 13 DESCRIPTION AND MAINTENANCE

13-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual:

Assembly No. 1463531
Schematic No. 1463533

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follow:

- Figure 13-3, block diagram
- Figures 13-4 to 13-6, simplified schematic
- Figure 13-7, waveforms
- Figure 13-8, maintenance data

Parallel/Serial Converter w/Vel Comp PWA 13 function summary:

- Using 3:1 multiplexers, converts 3.58-MHz rate 24-bit data to 10.7-MHz 8-bit data for use in D/A converter section of Video Output PWA 14.
- The velocity compensator compares the sync phase error of each successive H-line, converts the error to an 8-bit binary number, and stores 12 H-lines or 16 H-lines (jumper selectable) of line error data corresponding to the 12 or 16 video lines in memory. As a line from memory is read, the line error for that line is also read from the velocity compensator error store which is used to modulate the 3.58-MHz read clock.

13-2 DESCRIPTION

13-3 General

The parallel-to-serial converter portion of PWA 13 clocks the 24-bit words of digitized video from the Memory PWAs at F_{sc} rate, into serial 8-bit words at $3F_{sc}$ rate. The serial sequence of data is sent to the Video Output PWA on a line-by-line basis where it is converted back into analog video. Clocking of the digital information is under control of the Memory Control PWA.

13-4 Parallel-to-Serial Conversion

See simplified schematic diagram Figure 13-4. RCB1 and RCB3 from the Memory Control PWA are the clock signals for the conversion process. See Figure 13-7,

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waveform B. RCB1 clocks the 24-bit data words from the Memory PWAs into a 24-bit register consisting of four hex D flip/flops U16-U19. RCB1 and RCB3 together are an encoded clock that operates the output multiplexer consisting of four dual 4-line-to-1-line data selectors U4-U7. When RCB1 alone is high, bits 1 through 8 are presented to the output pin of the Parallel/Serial Converter PWA. At the next interval, coincident with the next cycles of reference subcarrier, both RCB1 and RCB3 are low; bits 9 through 16 are multiplexed through. Then RCB3 goes high, allowing bits 17 through 24 to appear at the output. The next following RCB1 pulse initiates the sequence for the following 24-bit word. The serial 8-bit values are transformed into analog video signal in the Video Output PWA.

13-5 Velocity Errors

Velocity errors are nonlinear time-base errors of the recorded signal due to a complex combination of factors that affect the rate at which video information is recorded onto and/or read out of the tape on the VTR. The rate of change of error varies from beginning to end of a given line of video (short-term errors), and from beginning to end of a given field (long-term errors). The TBC makes a correction for these errors in the velocity compensator on a line-by-line basis. Variations in tip-to-tape velocity are minute, but are sufficient to cause a change of hue throughout the frame of displayed color video.

13-6 Velocity Compensation

On a line-by-line basis, the velocity error is assumed to be a ramp function for correction purposes. The Tape H Comparator PWA measures the velocity error for a given line of tape signal and forwards that information to the velocity compensation circuits as a line error signal. The velocity compensation circuits sample this value and store it. The stored value is retrieved from memory and compared with the value for the following line. The difference in value between the two is used to determine the slope and polarity of the output of a ramp generator circuit. The reference 3.58-MHz signal from the Sync Generator PWA is converted to a series of ramps at 3.58-MHz rate. The line error ramp, developed by the velocity compensation circuits as an analog of the line error rate of change, modulates the 3.58-MHz ramp. The resultant output from the voltage comparator is a 3.58-MHz-pulse train which varies in phase as a function of the slope of the line error ramp. The modulated 3.58-MHz signal is used as a clock to develop the read function timing signals in the Memory Control PWA. These timing signals are used for the read function by the Memory, Parallel/Serial Converter, and Video Output PWAs. Each succeeding line receives an updated line error ramp correction.

13-7 Velocity Compensation Circuits

13-8 Functional Description

See Figure 13-3. The TBC stores the off-tape video in a digital memory on the Memory PWAs. This digital information is read out of the memory in a line-by-line sequence six lines later in time than it is written into the memory. The line error signal is developed in the Tape H Comparator PWA coincident with the memory write operation. To preserve this signal until the corresponding read function for a given line of memory takes place, the velocity compensator converts the incoming differential line error voltage to an 8-bit digital value and stores it in an 8-bit x12, x16, or x20 register in the velocity compensation circuits. Timing signals from the

Memory Control PWA are encoded to select the line error word in the register that corresponds to the line of digitized video that is being processed by the Parallel/Serial Converter PWA. The selected line error word is converted back to analog form and applied to the line error ramp generator. The line error ramp is applied to a voltage comparator as a reference value against the 3.58-MHz ramp signal. The line error ramp slices the 3.58-MHz ramps and the resultant output is a phase-modulated 3.58-MHz clock (read Fsc). This signal is routed back to the Memory Control PWA.

13-9 Circuit Description

13-10 Analog-to-Digital Converter

Analog-to-digital conversion circuits in the velocity compensation option consist of five integrated circuits:

- 74LS02 steering gates to control the start signal and the 3.58-MHz/2 clock pulses.
- Successive approximation register
- Digital-to-analog converter
- Voltage comparator
- Serial-to-parallel shift register

See Figure 13-1. The digital-to-analog converter DAC-08 outputs current values indicated on the table in the figure as programmed by the digital outputs of the successive approximation register AM2502 (U24). These currents are summed at one input to the NE529 (U11-7) voltage comparator. Reference input of the comparator is at circuit ground. If the error current is more than the D/A I/O current, the comparator output is low. If the error current is less than the D/A I/O current, the comparator output is high.

Flywheel sync from the Tape VCO PWA is delayed 14 μ s from the leading edge of H-sync in the write function. This generates a 3.7- μ s start signal which is reclocked by the 3.58-MHz/2 clock. Master latches of the successive approximation register are reset by the start pulse. At the first low-to-high transition of the clock pulse after the end of the start pulse, slave latches are set with Q1 through Q6 high and Q7 low. Bit 1 of the D/A converter produces a mid-scale I/O of 1 mA. If error current is greater than this, the slave latch of Q7 is locked low and a low is clocked into the serial-to-parallel shift register. The next clock pulse sets Q6 low and a similar comparison/shift register entry is made. This action continues until all eight of the binary weighted values have been tried. The complete conversion output stops the clock and triggers two one-shots that perform the next step. One of the one-shots operates the sample-and-hold circuit to store the error voltage for that line so that it may be compared with the value of the next line. The line error voltage has been made at burst crossing time. The next line error voltage is established at burst crossing of the following line. Thus, the differential voltage established represents the accumulated error from the beginning of a line to the end of that line. The other one-shot enables the write address gates to clock the contents of the serial-to-parallel shift register into the 8-bit x 12-line or 16-line storage register.

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The read address signals from the Memory Control PWA are encoded to match up the digitized line error signal out of the storage register with the appropriate line of video currently processed by the parallel-to-serial converter circuits. Because the differential line error voltage is read into the storage register one line behind the relevant line of video written into the Memory PWAs, the read address signals are re-encoded in the velocity compensation circuits to provide a read address of one line ahead of the read address of the parallel-to-serial converter. To express it another way, a given line in the P/S converter arbitrarily designated as line 1 will have the line error data for that line stored in line 2 of the line error storage register. Thus, while line 1 of the P/S converter is accessed, line 2 of the line error storage register must be accessed.

13-11 Digital-to-Analog Converter

The RA0' signal from the read address re-encoder clocks data out of the 8-bit x 12-line or 16-line storage register. The RA0', RA1', RA', RB', and RC' signals access appropriate data words in sequence. The D/A converter integrated circuit used here is the same type as was used in the analog-to-digital converter circuit. By placing a resistor on the I/O output capable of sourcing 1 mA of current, the D/A converter is operated in a bipolar mode. That is, the range of output voltages extends from a positive full-scale output of -10V (binary 256 at the digital input), through a midscale zero output, to a negative full-scale output of +10V (binary 000 at the digital input). The D/A converter feeds the input of an inverter operational amplifier with a gain of -2.

13-12 Line Error Ramp Generator

An FET switch and noninverting voltage follower form a sample-and-hold circuit for the buffered output of the D/A converter. RA0' trips a one-shot (U36-12) that operates the sample-and-hold and dumps the charge on the ramp generator charging capacitor C44. When the one-shot times out, the ramp starts and continues to the end of the video line.

13-13 Read Fsc Phase Modulator

Reference Fsc from the Sync Generator PWA clocks a 3.58-MHz rate ramp generator. This waveform is applied to one input of a voltage comparator. The linear error ramp slices the 3.58-MHz pulse train which is labeled as read Fsc at the output of the Parallel/Serial Converter PWA.

13-14 Second-Order Velocity Error Compensation

Voltage value at the output of the voltage follower U37-1 is an analog of the nonlinear time-base error from the start of a given line to the end of that line. It is derived by measuring the velocity error at the beginning of a line, storing that value, and comparing it with a value obtained from the succeeding line to obtain the difference between the two. The ramp derived from the differential line error voltage and the correction time length is the velocity compensation ramp. The second-order rate of change of velocity error is given as:

$$\frac{d^2 (\text{velocity error})}{dt^2}$$

Error amplifier U38-7 generates a waveform which has a symmetrical curvature to satisfy the conditions stated above. It is then added to the first order correction of the error correction ramp generated by U37-7. If there is no second-order rate of change, the linear ramp is not affected. (See Figure 13-2.) The second-order difference of velocity error is determined by taking the differences between two successive first-order differences in the sample-and-hold difference amplifier U45-1. This second-order difference is integrated and offset by U38-7 to generate a line-rate ramp which is symmetrical around zero. This is then integrated along with the first-order difference in the integrator of the correction ramp generator U37-7.

13-15 MAINTENANCE

See Figures 13-6 and 13-7 at the end of this section for simplified schematics and waveforms called out in these procedures.

Before undertaking any adjustments to the P/S converter velocity compensation circuits, review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-6 for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the P/S converter and interactive functions between it and other PWAs before making any adjustments.

This procedure is intended as a check of the basic performance of the velocity compensator and a method of adjustment for error within the circuit. If problems are suspected after completion of the procedure, substitution of PWA 13 should be used as a troubleshooting aid. Further adjustment requires the use of specialized equipment available only at the factory.

13-16 Velocity Compensator Alignment

- STEP 1** Use the basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN and a vectorscope at VIDEO OUT 1.
- STEP 2** With power off place P/S Converter PWA on an extender board and install into card rack.
- STEP 3** Switch velocity compensation on (switch S1 up, PWA edge).
- STEP 4** Set jumper J1 to B-C (test). This forces a median value out of the D/A converter, U52.
- STEP 5** Clock ramp generator:
 - a. Connect oscilloscope as follows: CH1—TP21 (clock ramp). Trigger on internal
 - b. Adjust R118 (ramp reset) for a ramp with 20 ns off-time at negative edge as shown in WF20(K). If adjustment is not properly made, the clock ramp generator will drift.

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STEP 6 Input/output offset compensation:

- a. Connect oscilloscope as follows: CH1—TP20 (vel comp ramp). Trigger on PWA 13 pin 21 (RMC). Typical line-by-line ramps are given in WF22 (L), Figure 13-7.
- b. Adjust R100 (first-order output offset) so that no ramp is visible. Use maximum vertical gain on the oscilloscope.
- c. Connect oscilloscope as follows: CH1—TP23 (second-order correction). Trigger on pin 83 (flywheel sync).
- d. Adjust R97 (second-order offset) for no ramp.
- e. Return jumper J1 to A-B.
- f. Ground TP2 (line error input).
- g. Return oscilloscope probe to TP20.
- h. Adjust R6 (input offset) for no ramp.
- i. Remove ground on TP2 and disconnect oscilloscope.

STEP 7 First order correction gain and ramp timing:

- a. Connect vectorscope to VIDEO OUT 1.
- b. Misadjust R1 (vernier correction gain) to a 3/4 clockwise position.
- c. Play a recording of 75% color bars.
- d. Adjust R51 (correction start) for a 2.5- μ s pulse ($\pm 10\%$) at the Q3 collector (junction R63/66). Ramps must start between the end of burst and the start of picture video.
- e. Adjust R64 (coarse correction gain) for minimum vector dot size.
- f. Adjust R1 for minimum vector dot size.

Note

This completes first-order correction adjustments.

STEP 8 Second-order correction gain:

- a. Connect oscilloscope as follows: CH1—TP23 (second-order correction); CH2—PWA pin 83 (flywheel sync). Trigger on PWA pin 83.
- b. Adjust R86 (second-order ramp gain) so that ramps cross 0-V_{dc} level at the center of the horizontal line as illustrated in WF24(N).

Note

Adjustment of R65 should be done with care.

- c. Adjust R65 (second-order output gain) for minimum vector dot size.
- d. With power off, remove PWA from the extender board and replace it in the card rack.

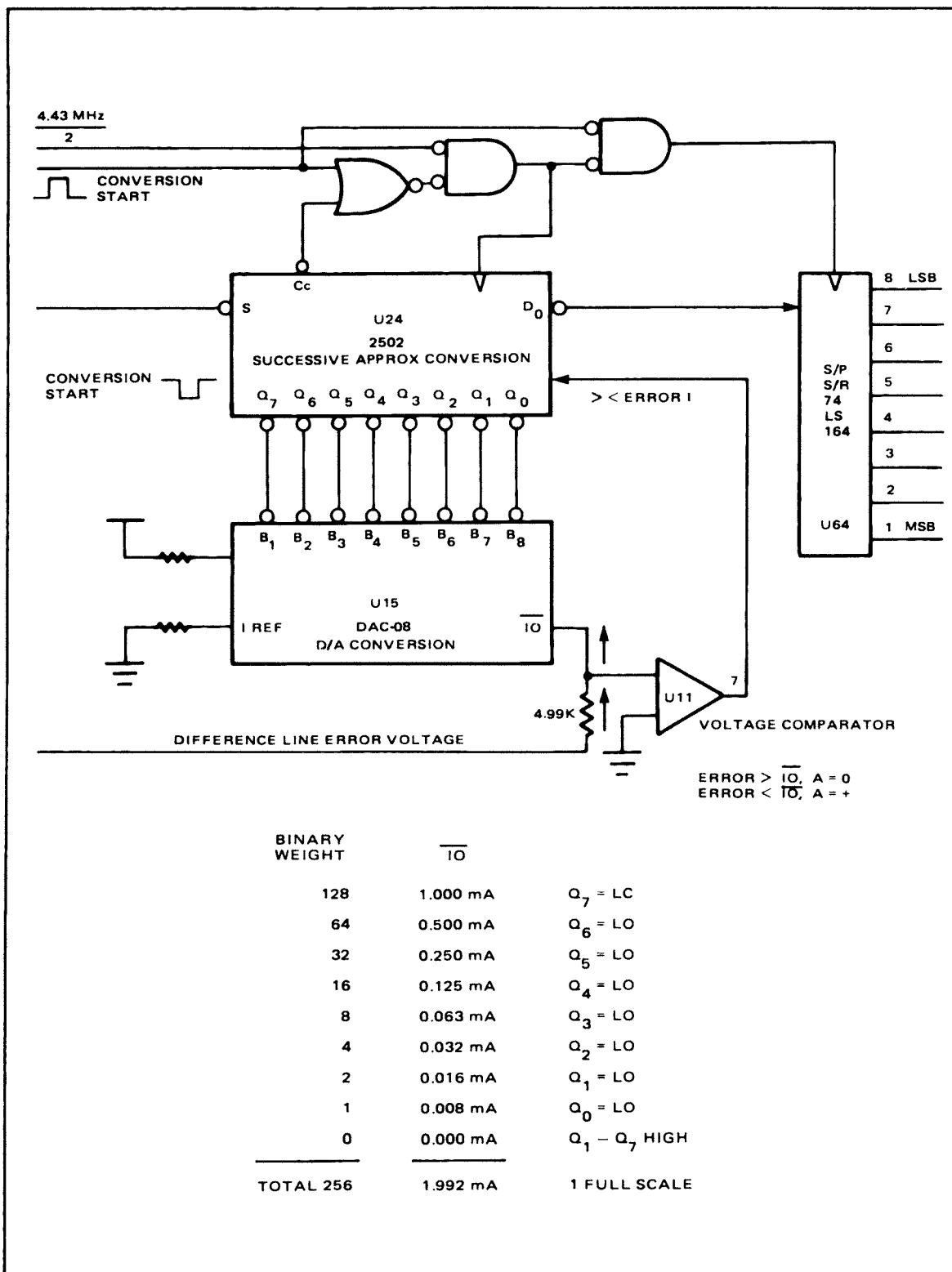


Figure 13-1. Differential Line Error, Analog to Digital Converter PWA 13

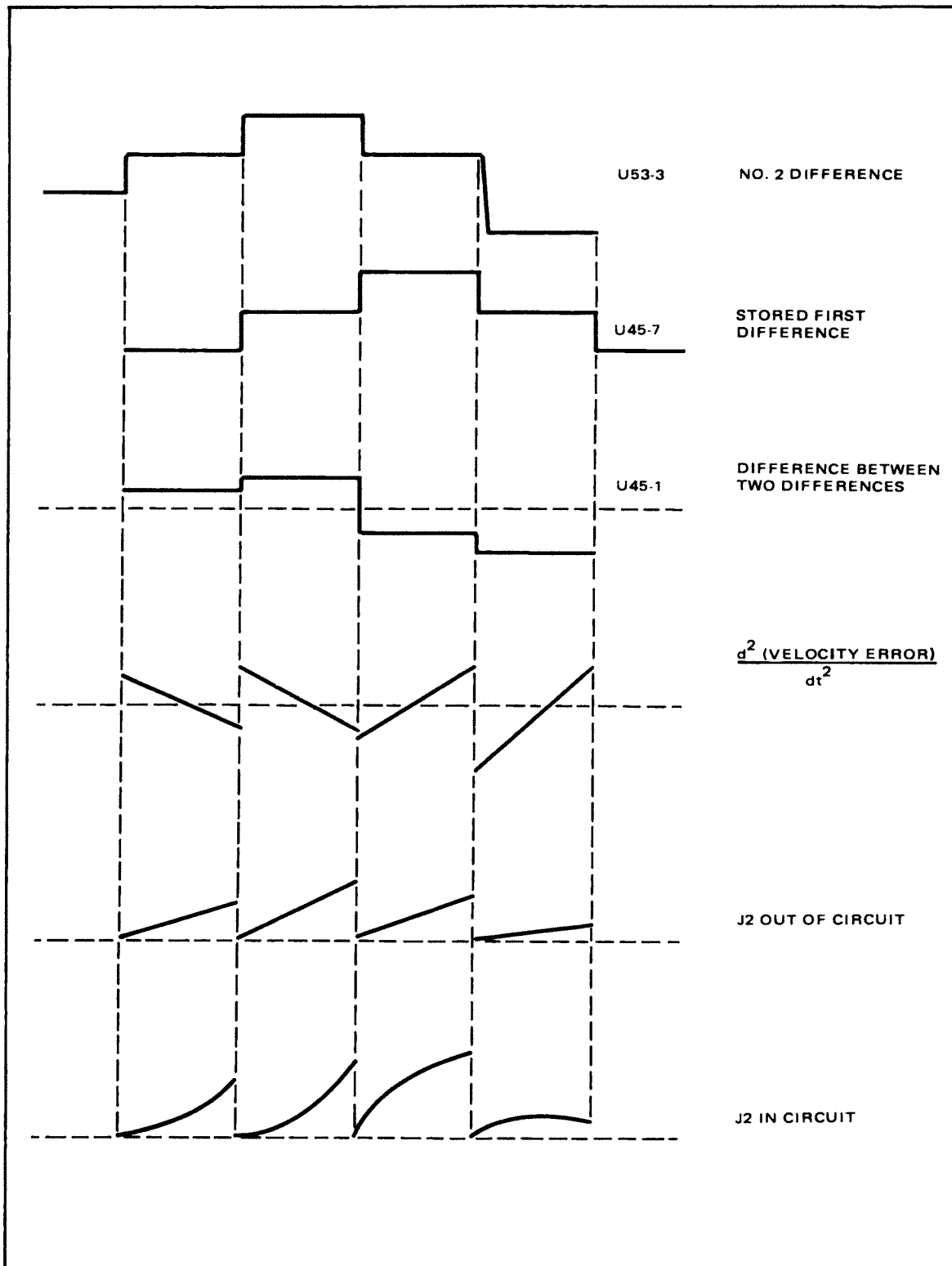


Figure 13-2. Second Order Correction Waveforms

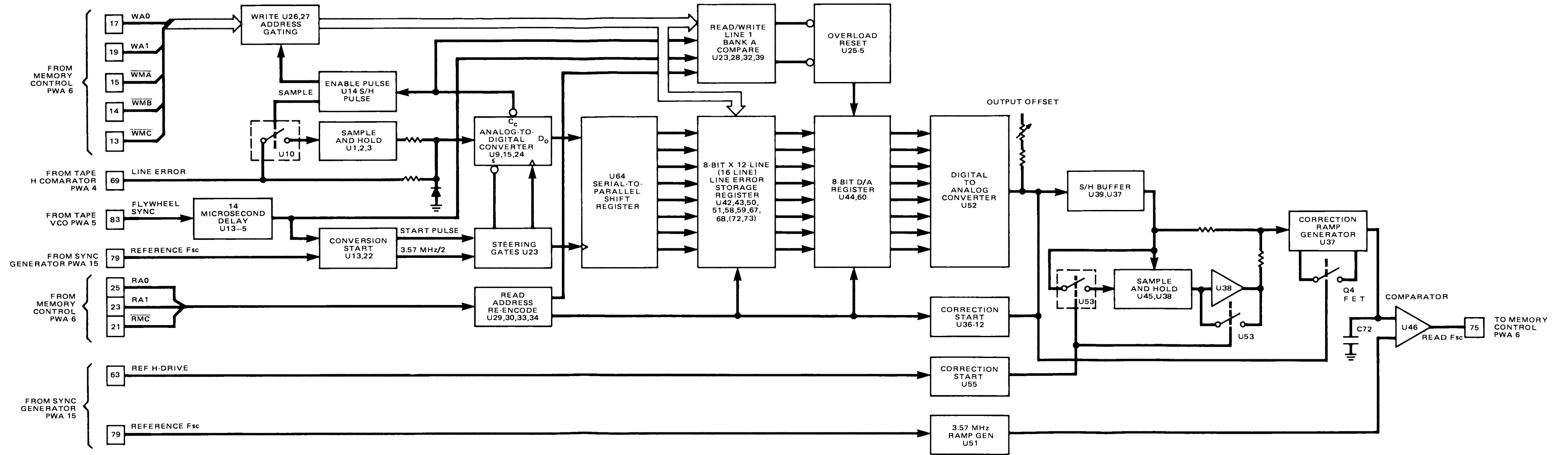


Figure 13-3.
Velocity Compensator Simplified Block Diagram,
Parallel/Serial Converter w/Vel Comp PWA 13

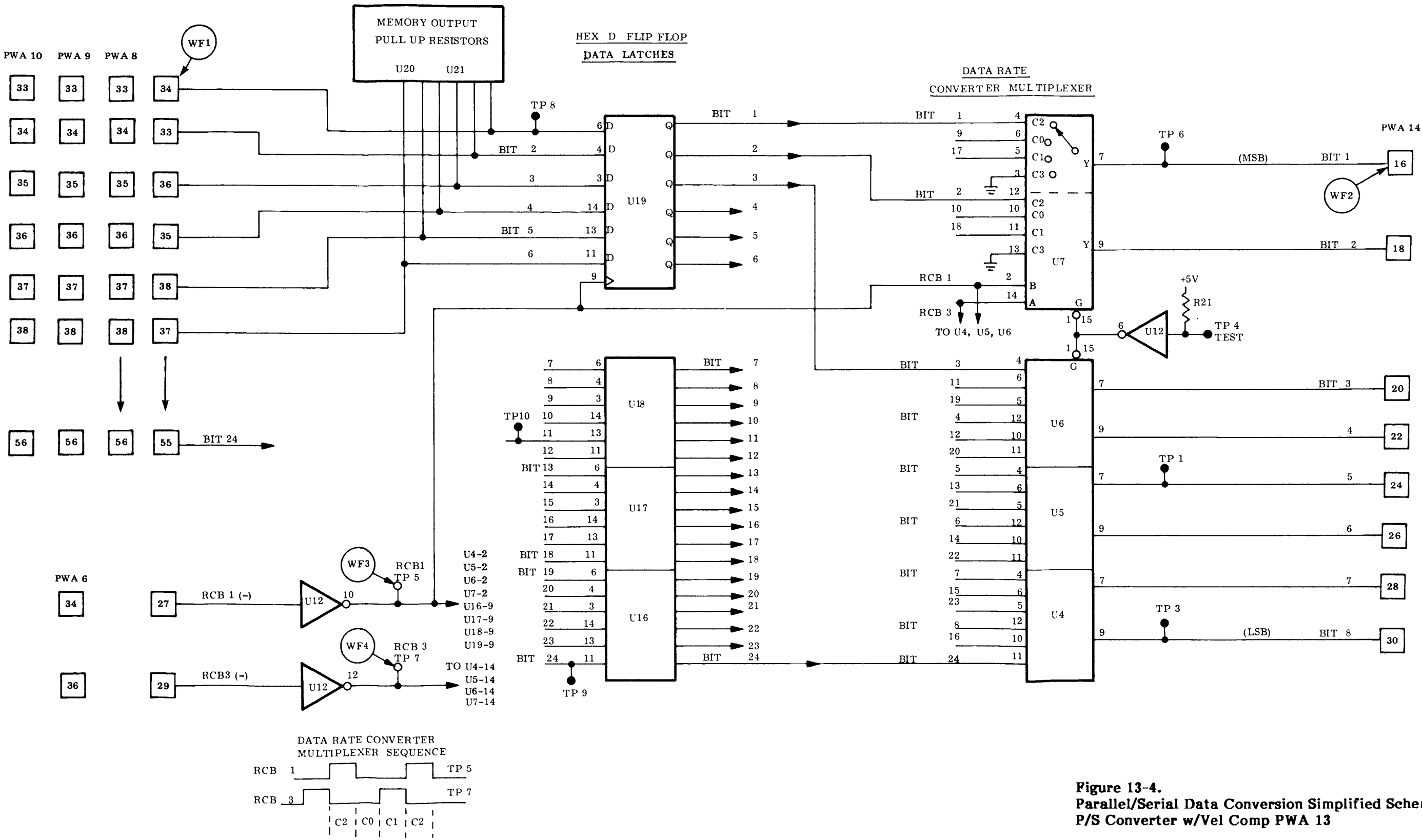


Figure 13-4.
Parallel/Serial Data Conversion Simplified Schematic,
P/S Converter w/Vol Comp PWA 13

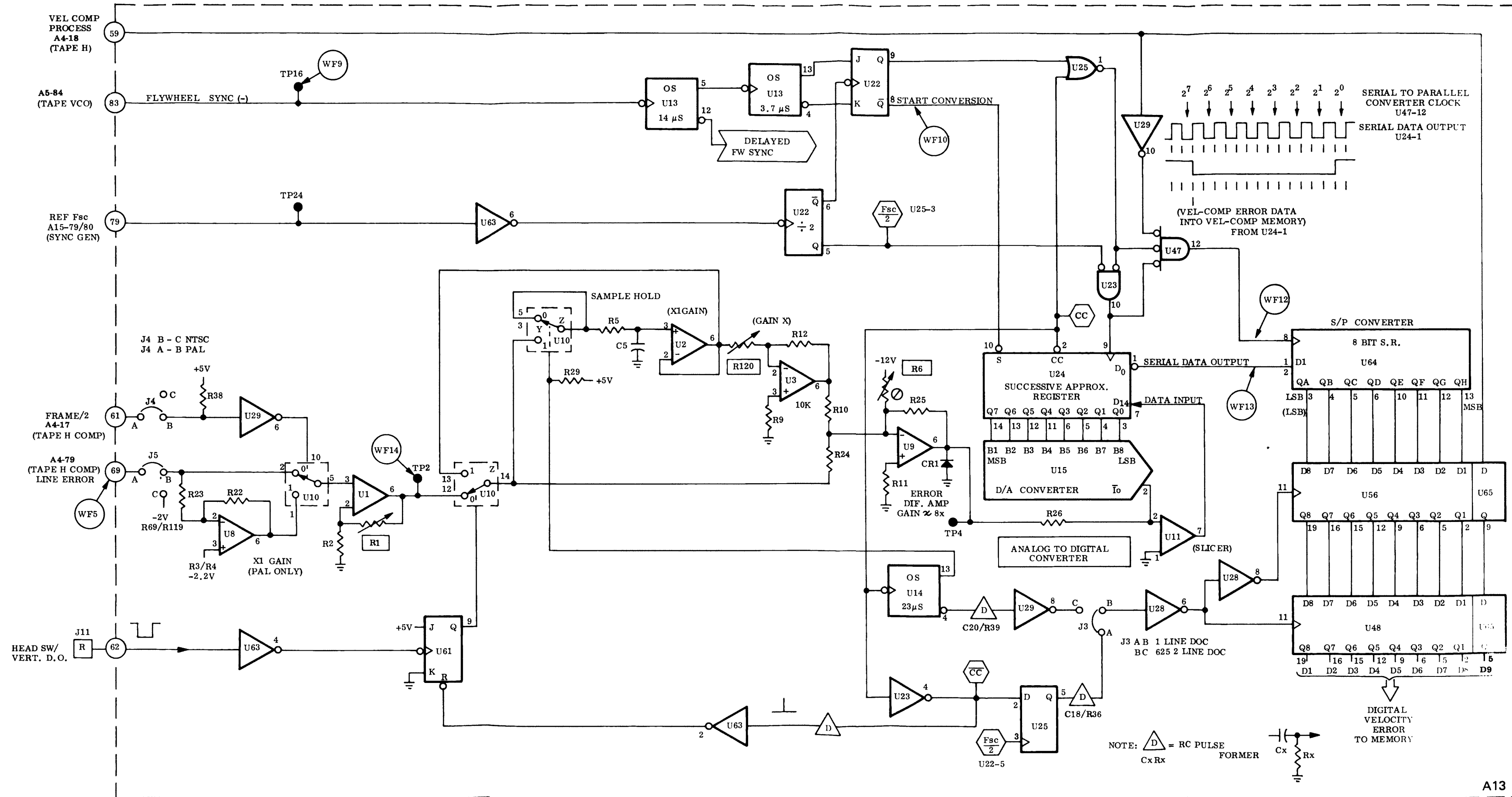


Figure 13-5.
Velocity Compensator Simplified Schematic,
P/S Converter w/Vel Comp PWA 13
(Sheet 1 of 2)

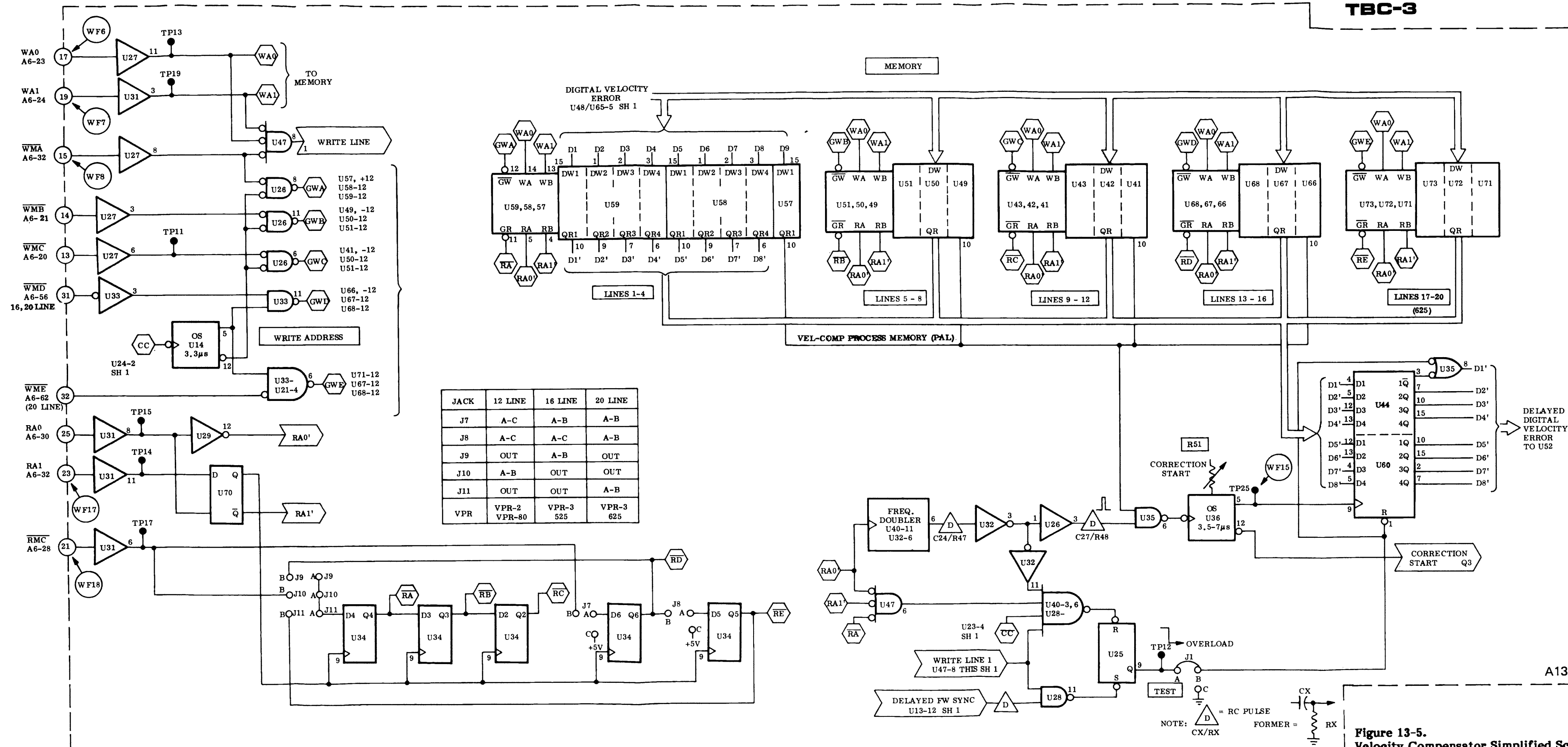


Figure 13-5.
Velocity Compensator Simplified Schematic,
P/S Converter w/Vel Comp PWA 13
(Sheet 2 of 2)

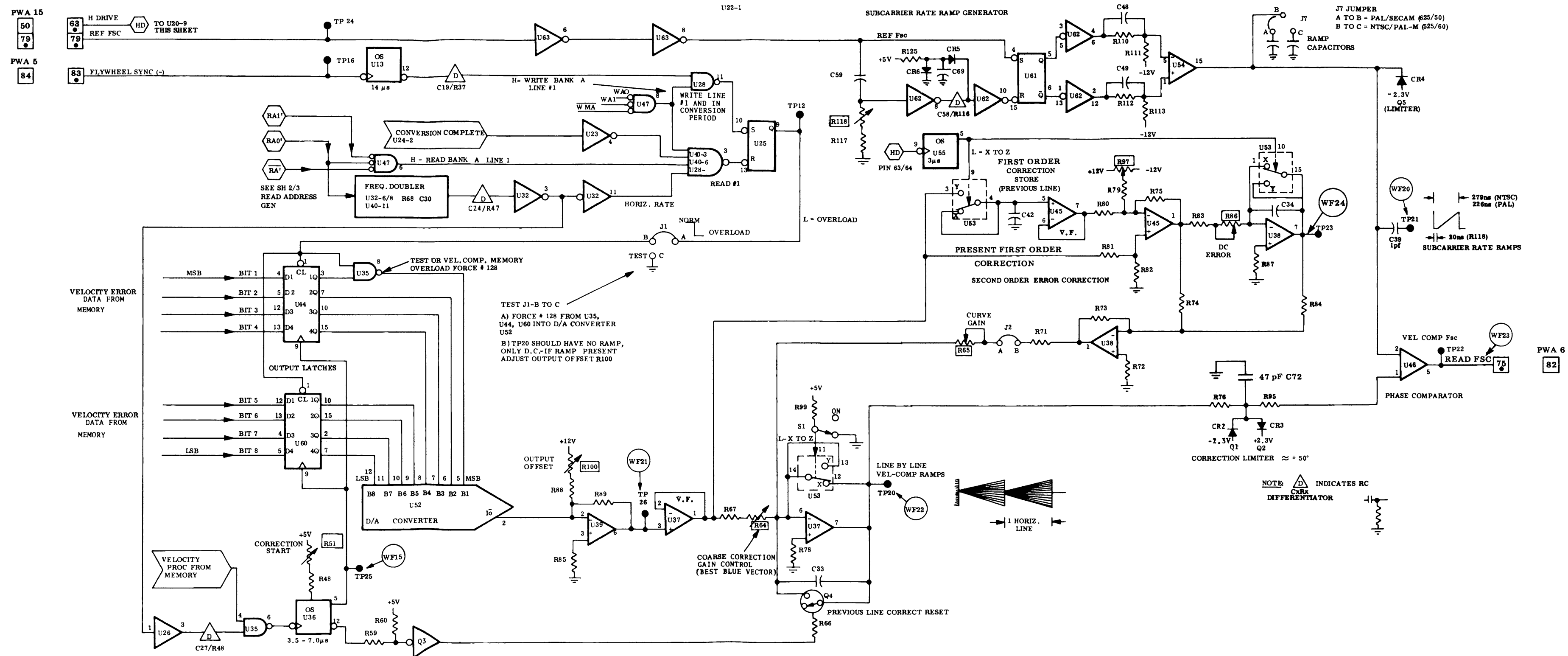


Figure 13-6.
Velocity Error Output Simplified Schematic,
P/S Converter w/Vel Comp PWA 13

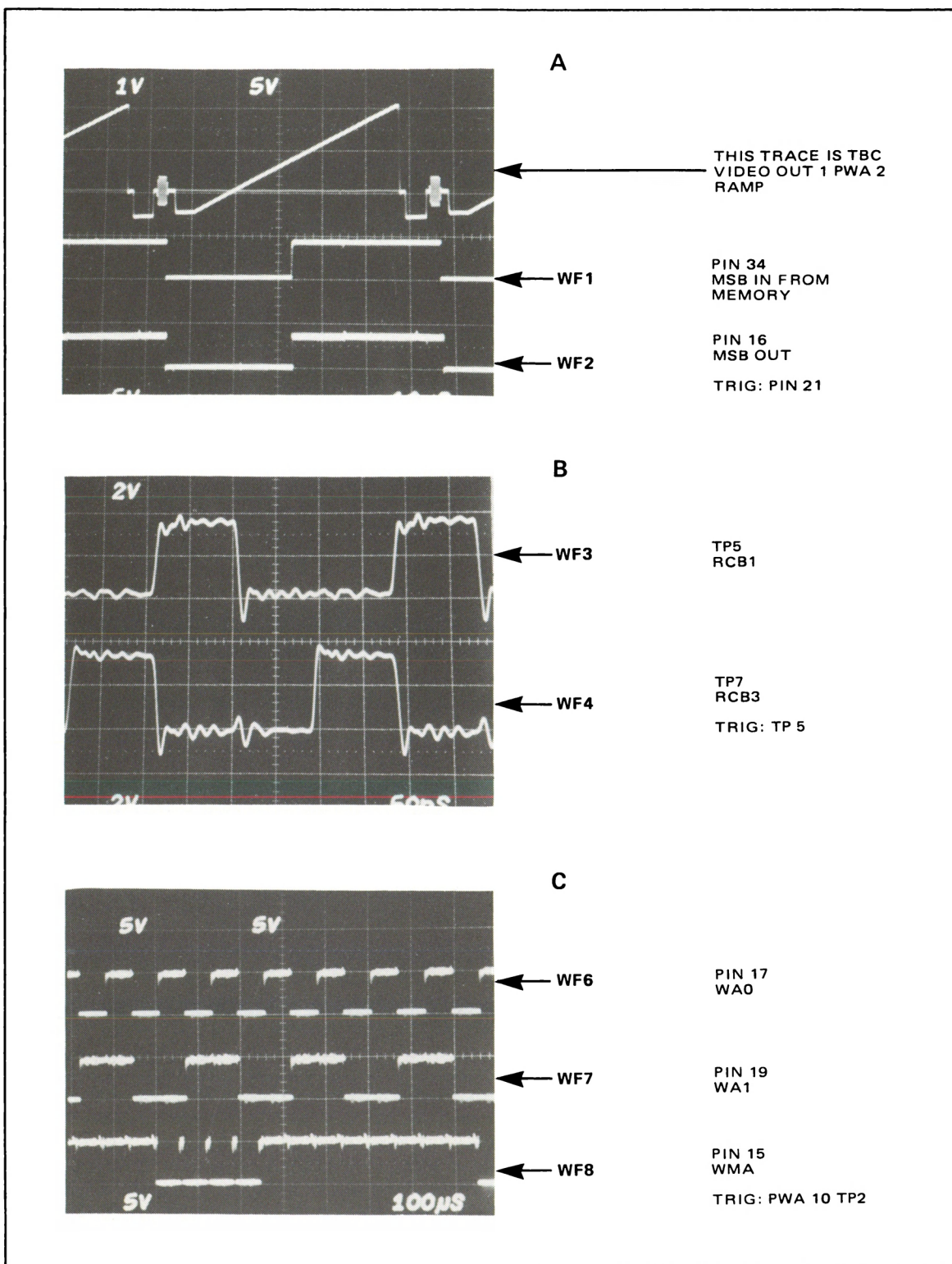


Figure 13-7. P/S Converter w/Vel Comp PWA 13 Waveforms (Sheet 1 of 5)

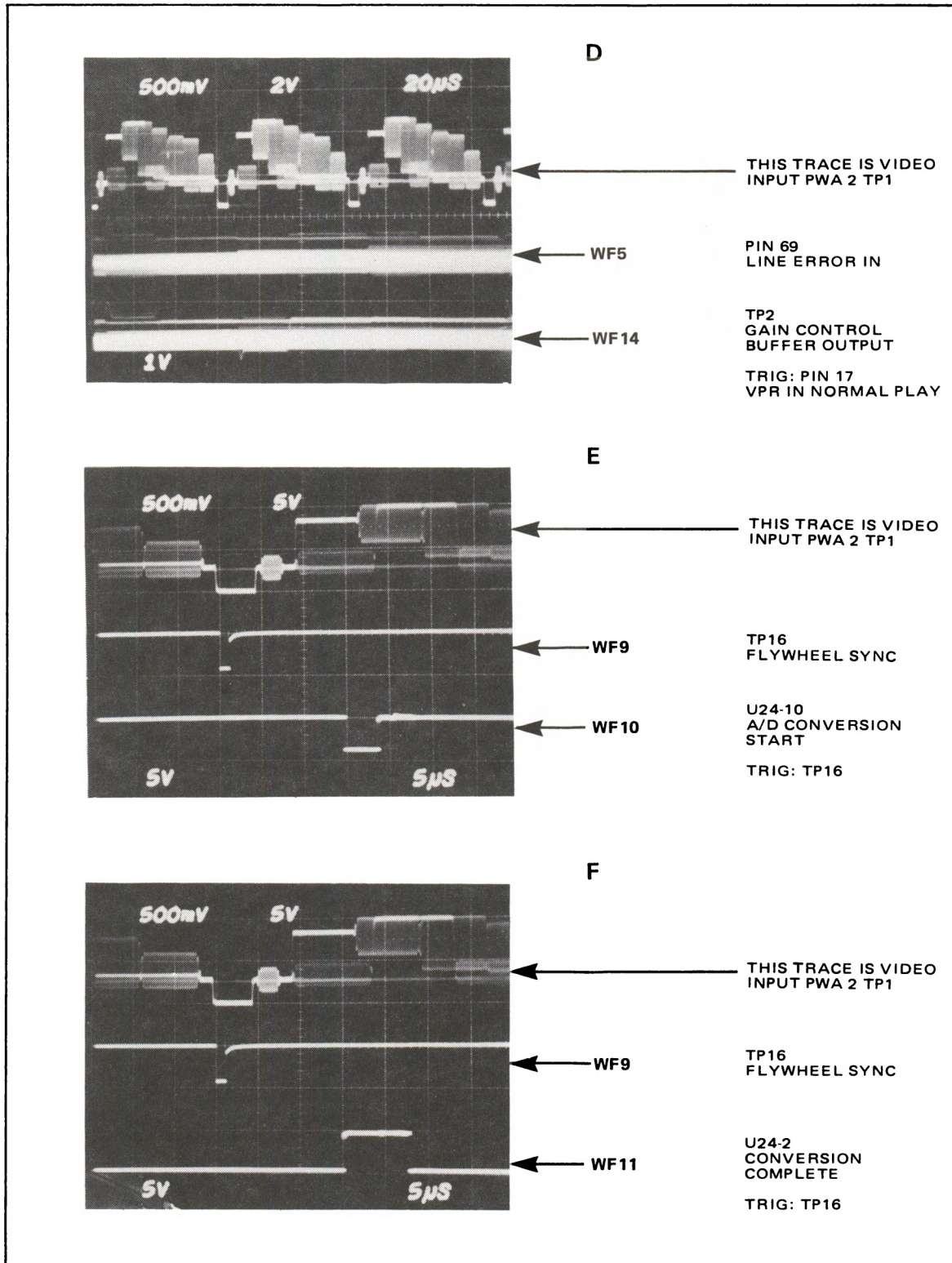


Figure 13-7. P/S Converter w/Vel Comp PWA 13 Waveforms (Sheet 2 of 5)

TBC-3

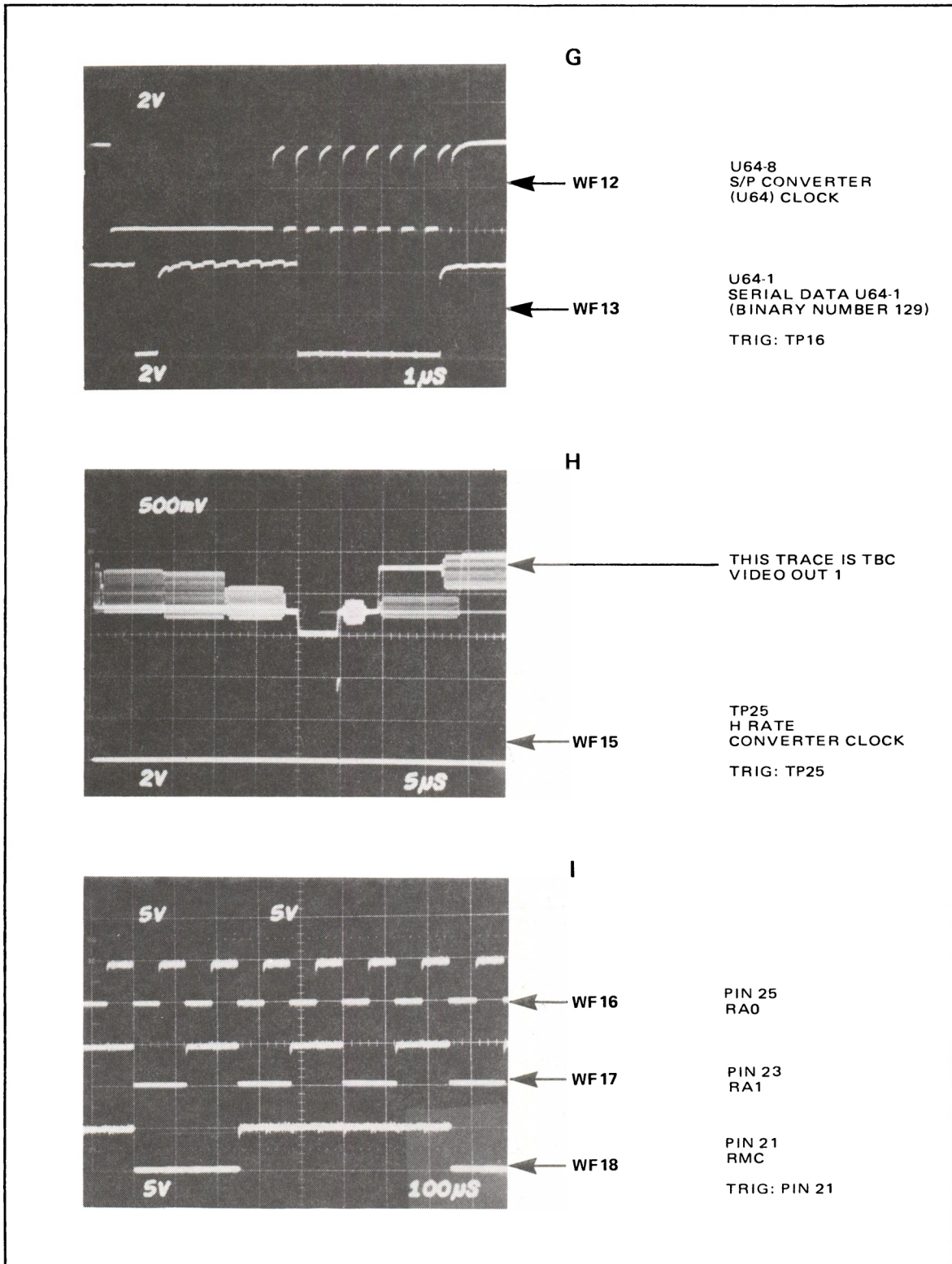


Figure 13-7. P/S Converter w/Vel Comp PWA 13 Waveforms (Sheet 3 of 5)

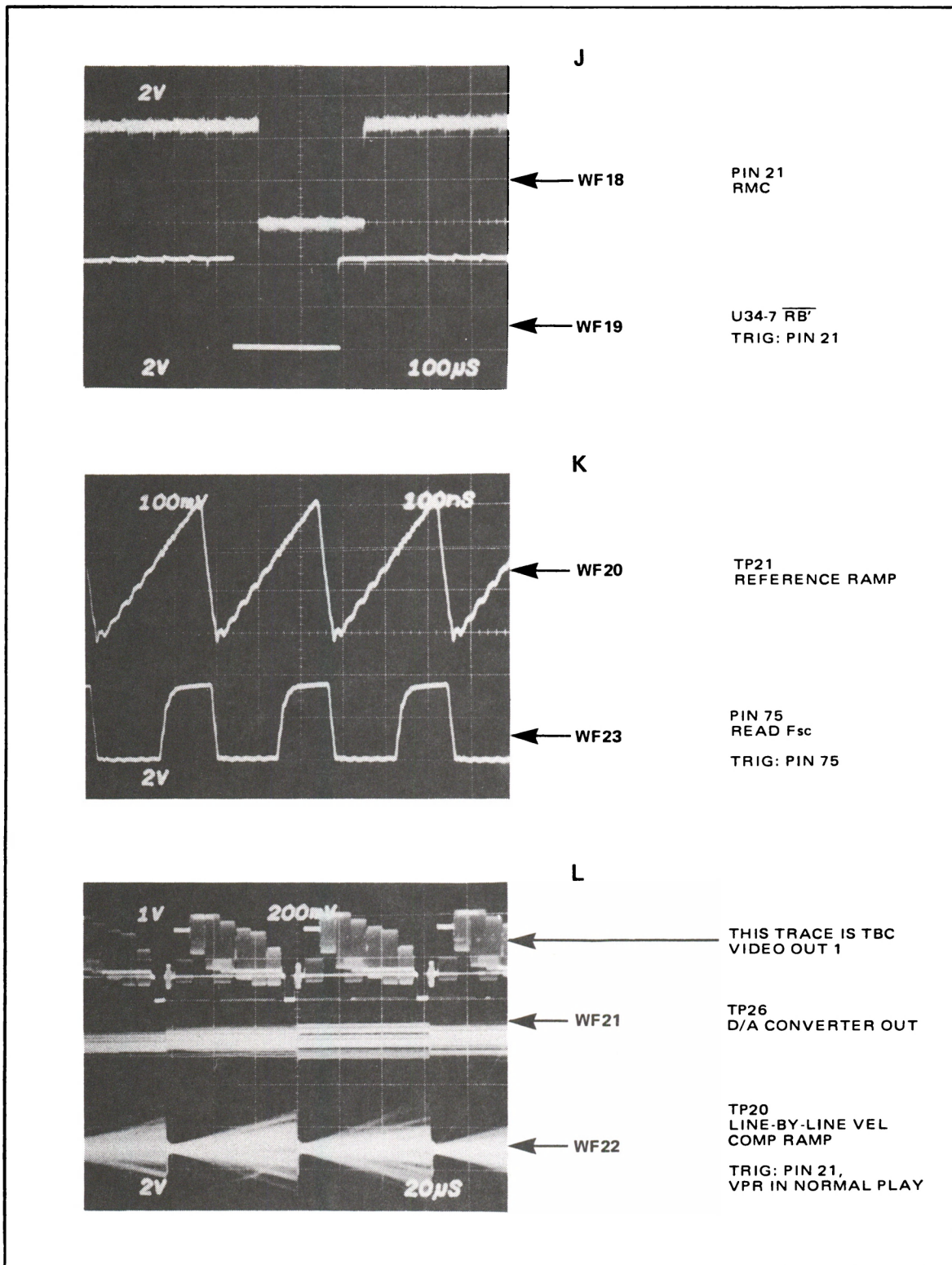


Figure 13-7. P/S Converter w/Vel Comp PWA 13 Waveforms (Sheet 4 of 5)

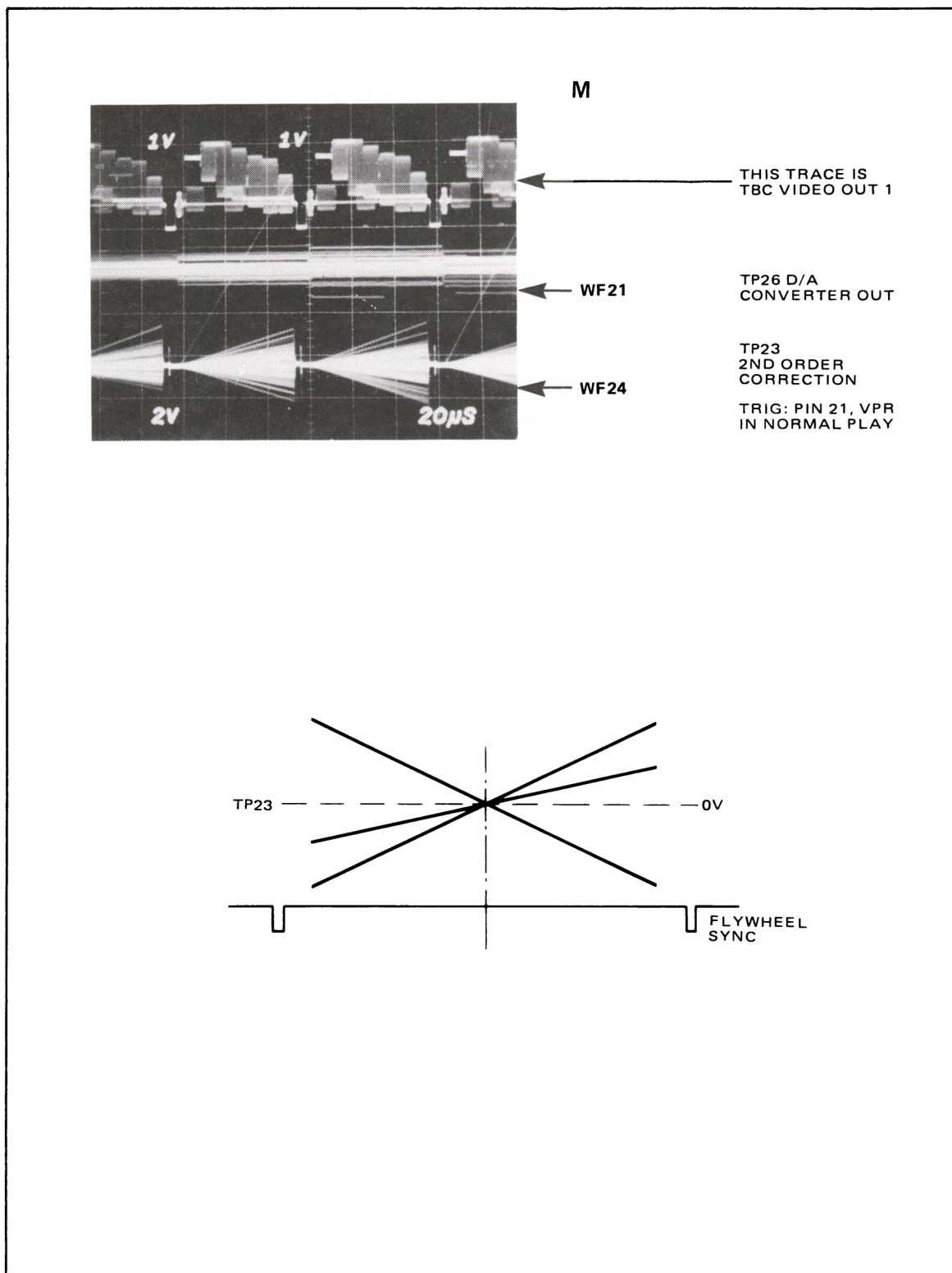


Figure 13-7. P/S Converter w/Vel Comp PWA 13 Waveforms (Sheet 5 of 5)

PWA 13 Jumpers

Jumper	Position	Function
J1	A-B	Factory Test
	B-C	Normal
		Test--forces memory overload condtion.
J2	A-B	Second Order Correction
		Normal
	Removed	Disconnects second-order correction
J3	A-B	Standard Select
		NTSC
	B-C	PAL/SECAM
J4	A-B	Standard Select
		PAL-M
	B-C	NTSC
J5	A-B	Factory Test
		Normal
	B-C	Test-inserts fixed error voltage
J6	A-B	12.5 Hz Select
		PAL/SECAM
	B-C	PAL-M/NTSC
J7	A-B	J7 through J11 are set as shown for each memory size.
20-line	A-B	
16-line	A-B	
12-line	A-C	
J8	A-B	
20-line	A-B	
16-line	A-C	
12-line	A-C	
J9	remove	
20-line	remove	
16-line	A-B	
12-line	remove	
J10	remove	
20-line	remove	
16-line	remove	
12-line	A-B	
J11	A-B	
20-line	A-B	
16-line	remove	
12-line	remove	

PWA 13 Adjustable Components

Component	Function
R1	Vernier correction gain
R6	Input offset
R51	Correction start
R64	Coarse correction gain
R65	2nd order output gain
R86	2nd order ramp gain
R97	2nd order offset
T100	1st order output offset
R118*	Ramp reset
R120**	Loop gain
S1	Vel comp on/off

*

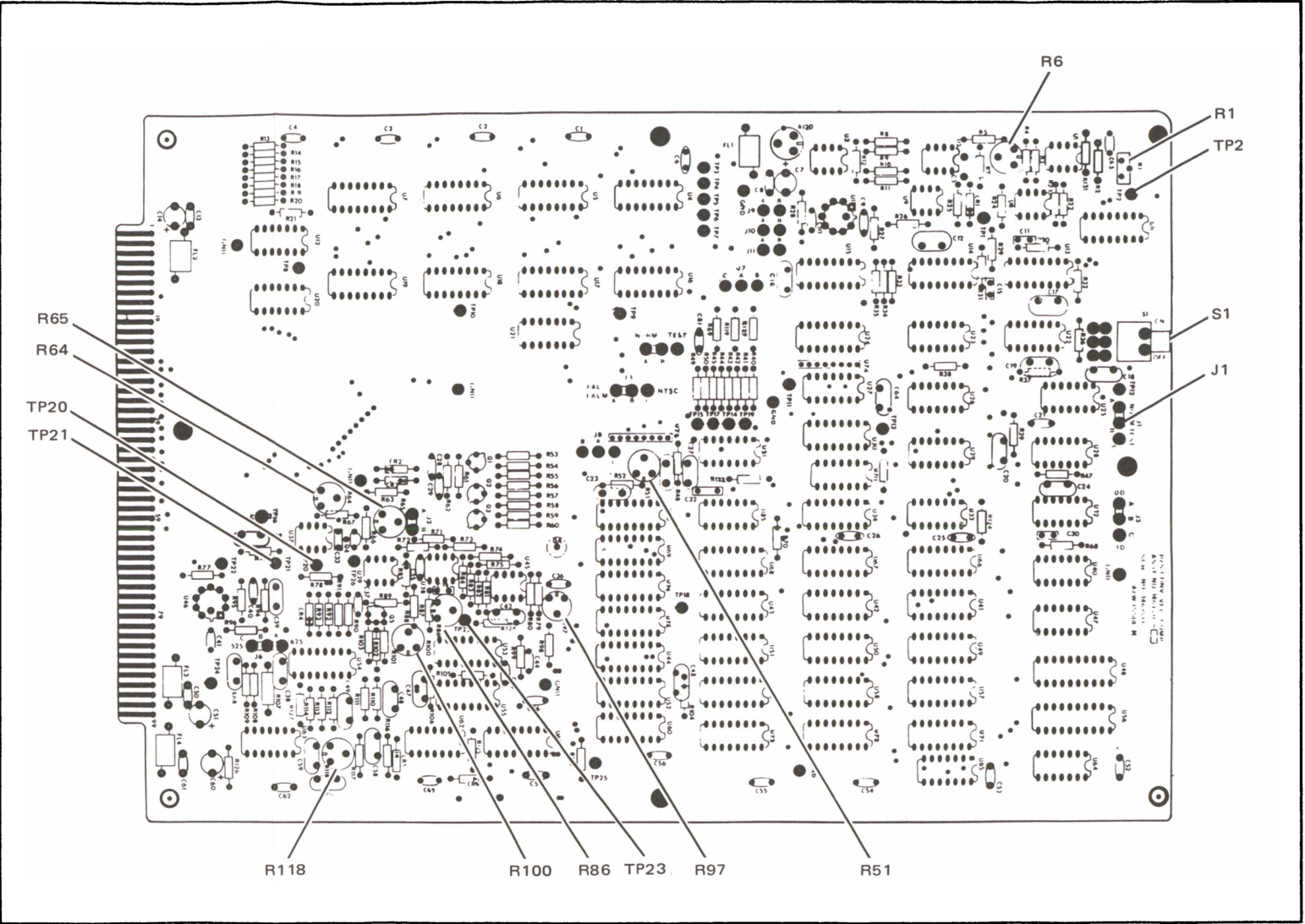
 Factory adjust only

**

 Not used in NTSC

PWA 13 Test Points

Test Point	Name
TP1	Error difference
TP2	Processed line error
TP3	LSB
TP4	+ 5V
TP5	RCB1
TP6	MSB
TP7	RCB3
TP8	MSB byte 1
TP9	LSB byte 3
TP10	3rd MSB byte 2
TP11	WMC
TP12	Memory overload
TP13	Write address zero (WA0)
TP14	Read address one (RA1)
TP15	Read address one (RA0)
TP16	Flywheel sync
TP17	RMC
TP18	Read memory C
TP19	Write address one (WA1)
TP20	Correction ramp
TP21	Clock ramp
TP22	Read Fsc
TP23	2nd order correction
TP24	Reference Fsc
TP25	H rate clock
TP26	D/A converter



PWA 13 Component Locator

Figure 13-8.
Test Points, Jumpers, Adjustable Components, Component
Locator, S/P Converter w/Vel Comp

PART II

SECTION 14

VIDEO OUTPUT PWA 14

DESCRIPTION AND MAINTENANCE

14-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1405189

Schematic No. 1405191

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 14-1, overall simplified block diagram
- Figure 14-2 and 14-3, simplified schematics
- Figure 14-4, waveforms
- Figure 14-5, maintenance data

Video Output PWA 14 function summary:

- Provides digital-to-analog conversion of the serial 8-bit data from P/S Converter w/Vel Comp PWA 13 back to analog video.
- During blanking interval the D/A conversion circuits are preset to the binary equivalent of the blanking level, yielding an analog video signal referenced to blanking.
- The analog video is filtered and clamped to the reference black level.
- Adds sync, burst, and reference timing from the Sync Generator PWA 15 to the time-base-corrected video.
- Provides three outputs. VIDEO OUT 1 and TBC video (for monitoring) are composite video; VIDEO OUT 2 sync can be inhibited by removing jumper J5.

14-2 DESCRIPTION

Video Output PWA 14 accepts 8-bit data words from Parallel/Serial Converter w/Vel Comp PWA 13 and converts them into analog video. In addition, horizontal and vertical sync, blanking, and burst, slaved to station master video, are reinserted in the video to form composite video and complete the time-base correction process. Video output drivers 1 and 2 each provide a 1 Vp-p composite video signal (into 75 Ω) to coaxial connectors at the rear panel of the TBC. Video

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output driver 1 also provides composite video, via jumper J1 on the motherboard of the TBC, to Video Input PWA 2.

14-3 Digital-to-Analog Conversion

Serial 8-bit data words are clocked into the input latch by reference $3F_{sc}$. The clocking process is inhibited during horizontal and vertical blanking periods by the blanking rise time control circuits. (See Figure 14-1.) Latched data bits are applied to the D/A converter which converts the digital value to an equivalent value of output current which is supplied to the buffer amplifier.

14-4 Analog Video Processing Circuits

Vertical and horizontal blanking from Sync Generator PWA 15 is inserted into the quantized video signal by blanking rise time control circuits in the buffer amplifier. To eliminate spurious oscillations that occur during transition from one quantized value to the next, the sample-and-hold circuit reads the quantized value after the signal has settled to a true value. In the next stage, horizontal blanking is clamped to ground to establish a reference level for the video signal. Low-pass and $(\sin X)/X$ filtering smooth the steps of the quantized video. The amplitude equalizing amplifier boosts the video to compensate for losses in video processing circuitry. The below-black-level noise clip amplifier removes any noise present in blanking intervals prior to reinsertion of vertical and horizontal sync, and burst.

14-5 Composite Sync and Burst

Burst flag gates subcarrier into the burst shaper. These signals are from Sync Generator PWA 15. The burst shaper contours the envelope of the 3.58-MHz burst. The sync shaper controls the rise and fall times of composite sync from the Sync Generator PWA.

14-6 Inhibit White Line Circuit

Bits 1 through 8 from the Parallel/Serial Converter w/Vel Comp PWA are decoded in the inhibit white line circuit to produce a flag if all 1's are present (white line). During the vertical blanking interval or when in search mode, the flag produces an inhibit to the output video amplifiers. When this inhibit is present, the output of the video amplifiers is clamped to a level close to the black level of horizontal blanking. This circuit is required because in freeze mode two and three lines of video are alternately deleted from each field. In search mode the write clock is randomly advanced or retarded to delete or add lines of video to maintain a recognizable picture on the monitor. Both of these events may cause white line conditions. Thus, video output is attenuated.

14-7 Output Video Amplifier

The reconstituted analog video, sync, burst, and white line inhibit are mixed in the output video amplifiers to produce a composite video signal which is time-base corrected and will deliver a 1-V_{p-p} signal into a 75 Ω impedance load.

14-8 MAINTENANCE

See Figures 14-4 and 14-5 for the waveforms, component locator diagram, jumper, test-point, and adjustable component summaries called out in these procedures.

Before undertaking any adjustments to the Video Output PWA, review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-6 for a general understanding of the nature and scope of these field adjustments.

Before making any adjustments, consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the interactive functions between the Video Output PWA and other PWAs.

14-9 Blanking Filter

- STEP 1 Use basic tape/reference test loop setup with a 0% APL flat field test signal to TAPE VIDEO IN.
- STEP 2 With power off put Video Output PWA 14 on the extender.
- STEP 3 Connect oscilloscope to the junction of R125 and R126. Trigger on PWA pin 71.
- STEP 4 Adjust R55 (blanking level dc balance) so that there is no step in the video at blanking.
- STEP 5 Adjust signal generator to 50% APL flat field.
- STEP 6 Connect oscilloscope (terminated) to PWA pin 59 (or VIDEO OUT 1). Trigger on PWA pin 49.
- STEP 7 Adjust L4 and L5 (blanking insertion filters) for a smooth transition and a fall time of 275 ± 30 ns from the 50% APL level to blanking.
- STEP 8 Adjust R65 (blanking insertion level) to obtain rounded corners (minimum preshoot and overshoot) at the video blanking insertion level.

Note

Be aware that the H-blanking leading and trailing edge (R46 and R45 on PWA 15) settings may interfere with adjustment of R65—appearing as ringing at the video/blanking level transition.

14-10 Sync Levels

- STEP 1 Use basic tape/reference test loop setup with a 75% color-bar signal at standard level connected to TAPE VIDEO IN.
- STEP 2 With power off put Video Output PWA on the extender.
- STEP 3 Connect oscilloscope to VIDEO OUT 1, trigger on pin 49.

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STEP 4 Adjust R192 (sync level) for 286 mV.

STEP 5 Adjust R221 (burst level) for 286 mV.

STEP 6 Adjust R206 (burst balance) so that burst is symmetrical with respect to blanking.

14-11 White Bar Suppression Clamp

STEP 1 Use the basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

STEP 2 With power off put Video Output PWA on extender.

STEP 3 Connect oscilloscope to VIDEO OUT 1 (terminated); trigger on pin 49. Display vertical interval.

STEP 4 Misadjust R320 (vertical clamp timing) fully clockwise.

STEP 5 With power off, pull Memory PWA 8 out just enough to disconnect it from motherboard. This empty memory produces a white bar.

STEP 6 Adjust R314 (vertical clamp level) so that the offset of white bar video in the vertical interval is 10-IRE units (75 mV) above blanking level.

STEP 7 With power off, reinsert Memory PWA 8

STEP 8 Connect oscilloscope as follows CH1—U20 pin 12; CH2—PWA pin 72; Trigger PWA pin 49

Note

For the next step, the adjustment depends on the setting for R65 (PWA edge SLO-MO) on the sync generator which users may adjust for a particular line in the vertical interval. In this case, R65 should blank out line 16 through its pedestal.

STEP 9 Adjust R320 so that positive edge of the pulse at U20 pin 12 is coincident with positive edge of vertical blanking at PWA pin 72 as shown in WF14/15(I).

14-12 Black Clip

STEP 1 Use the basic tape/reference test loop setup with a 75% color-bar signal at standard level to TAPE VIDEO IN.

STEP 2 Connect oscilloscope to VIDEO OUT 1 (terminated); trigger on pin 49.

STEP 3 With power off put Video Output PWA on extender and activate the test ramp with Video Input PWA 2 jumper J4 set to B-C.

- STEP 4** Adjust R135 (black clip) so that negative clipping point of ramp is 35 mV below blanking. The clipped ramp may be seen in WF13(D).
- STEP 5** Remove PWA 14 J4 and verify that negative point of ramp is not clipped. Replace J4.
- STEP 6** With power off, return PWA 2 J4 to A-B and PWA 14 to its slot.
- STEP 7** Recheck system unity gain.

14-13 Interpolation Filter

The interpolation filter (C80/C83/L8/L9/L10/L1/L12/T2/T3), the D/A converter (R114/R115/R116/R117/R122/R123) and the differential gain below black (L13 and R282) are factory aligned to very high tolerances using special test fixtures and measuring devices. These circuits should not be aligned in the field.

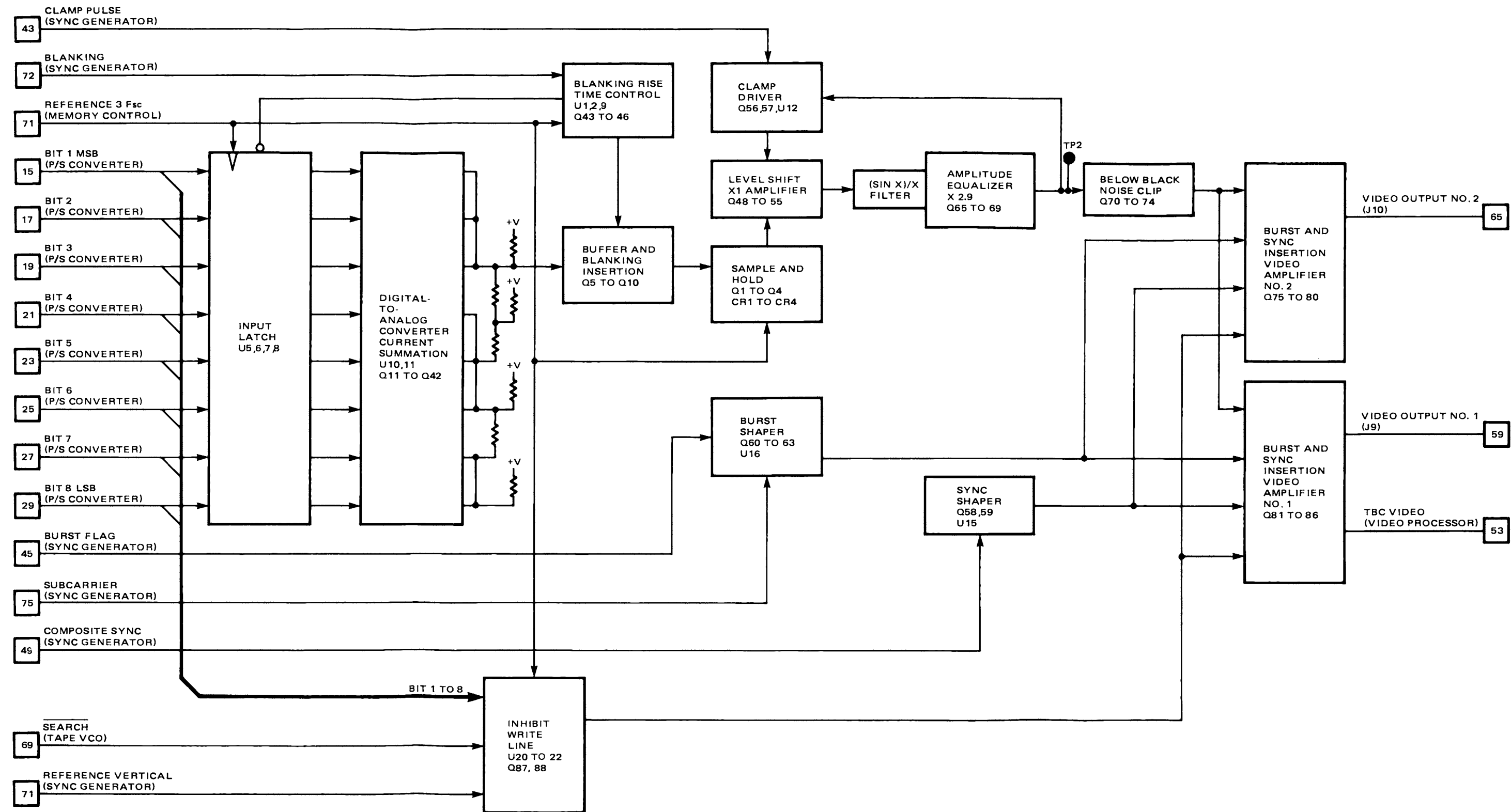


Figure 14-1.
Video Output PWA 14 Block Diagram

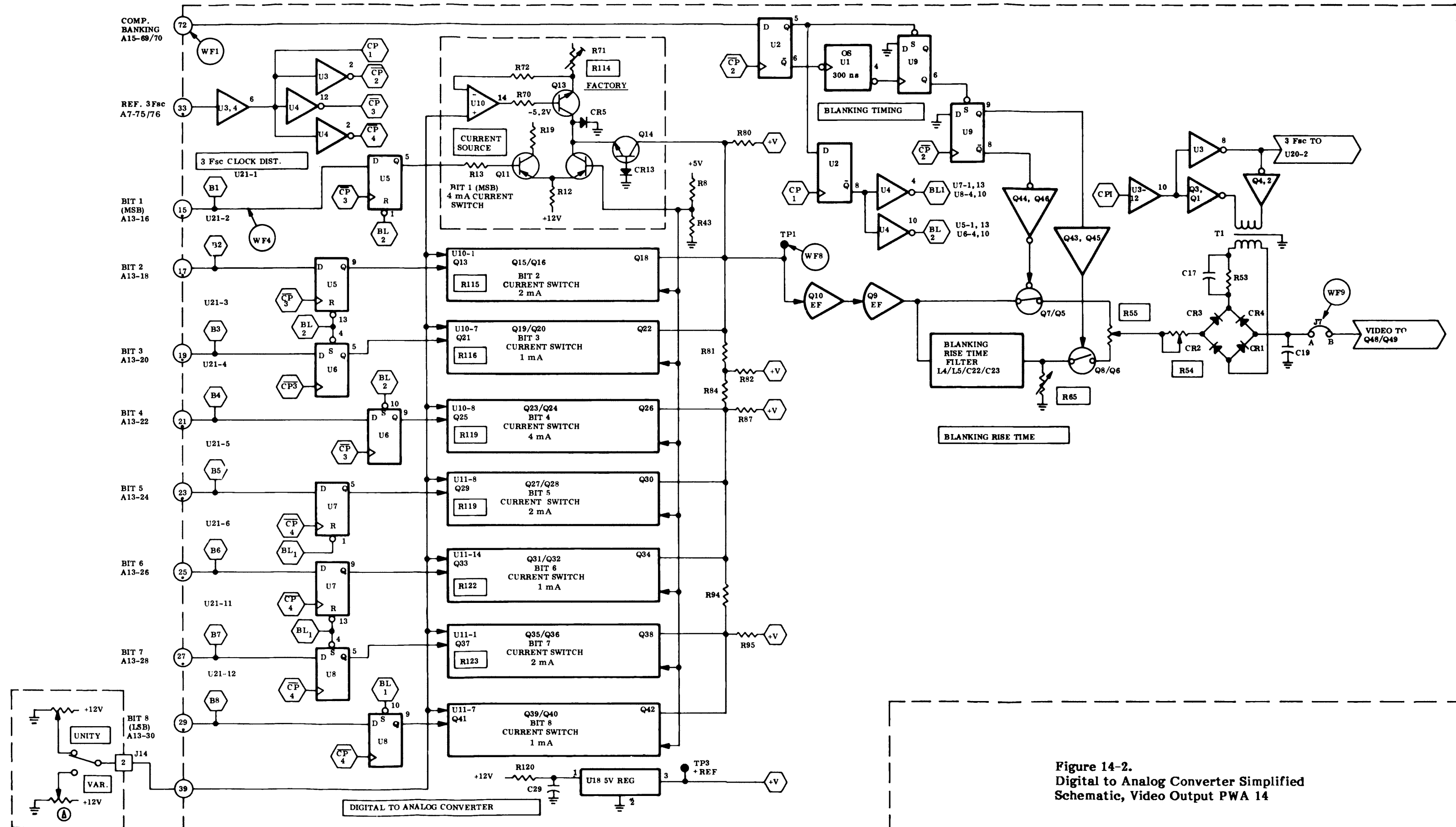


Figure 14-2.
Digital to Analog Converter Simplified
Schematic, Video Output PWA 14

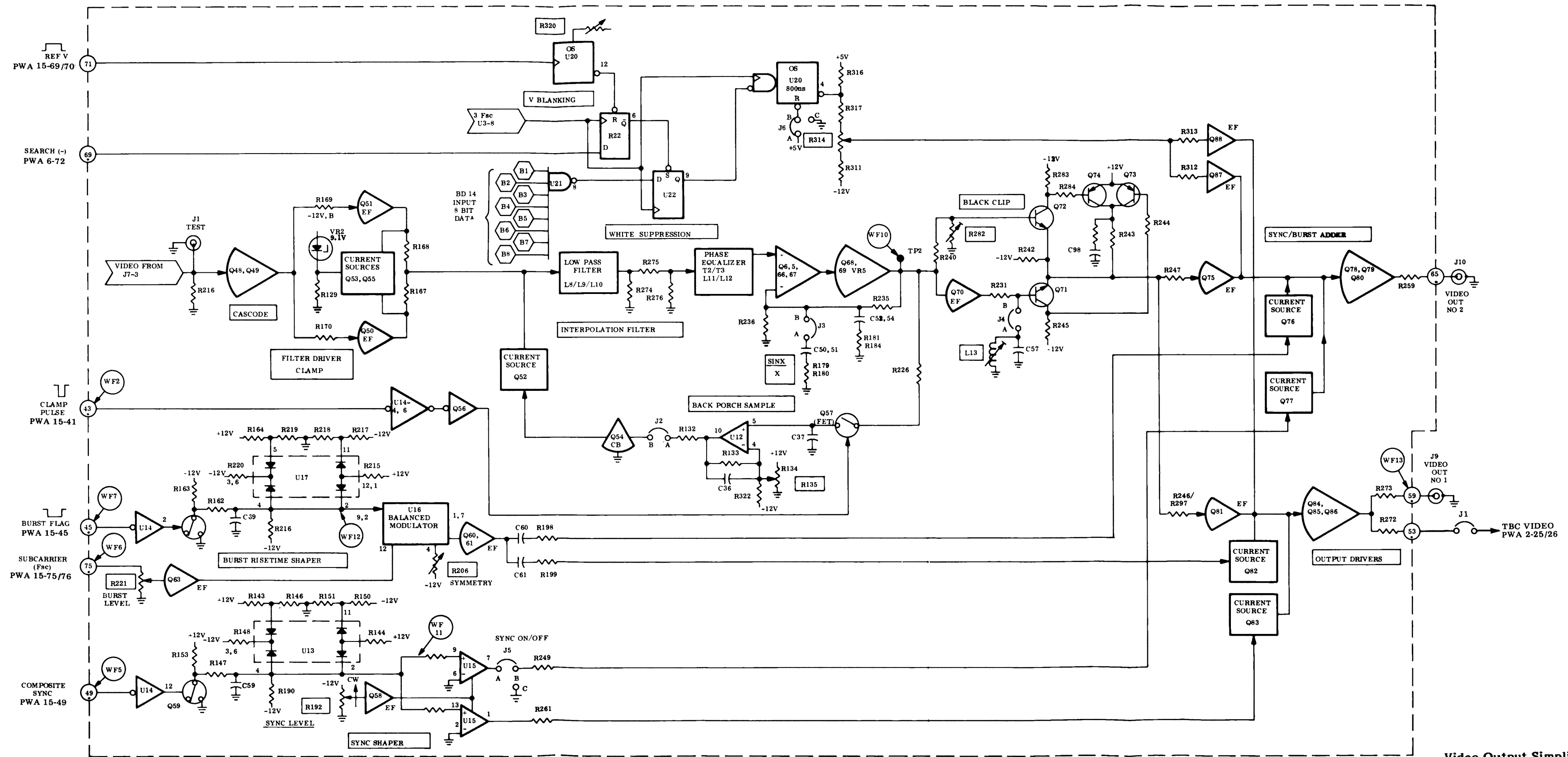


Figure 14-3.
Video Output Simplified Schematic,
Video Output PWA 14

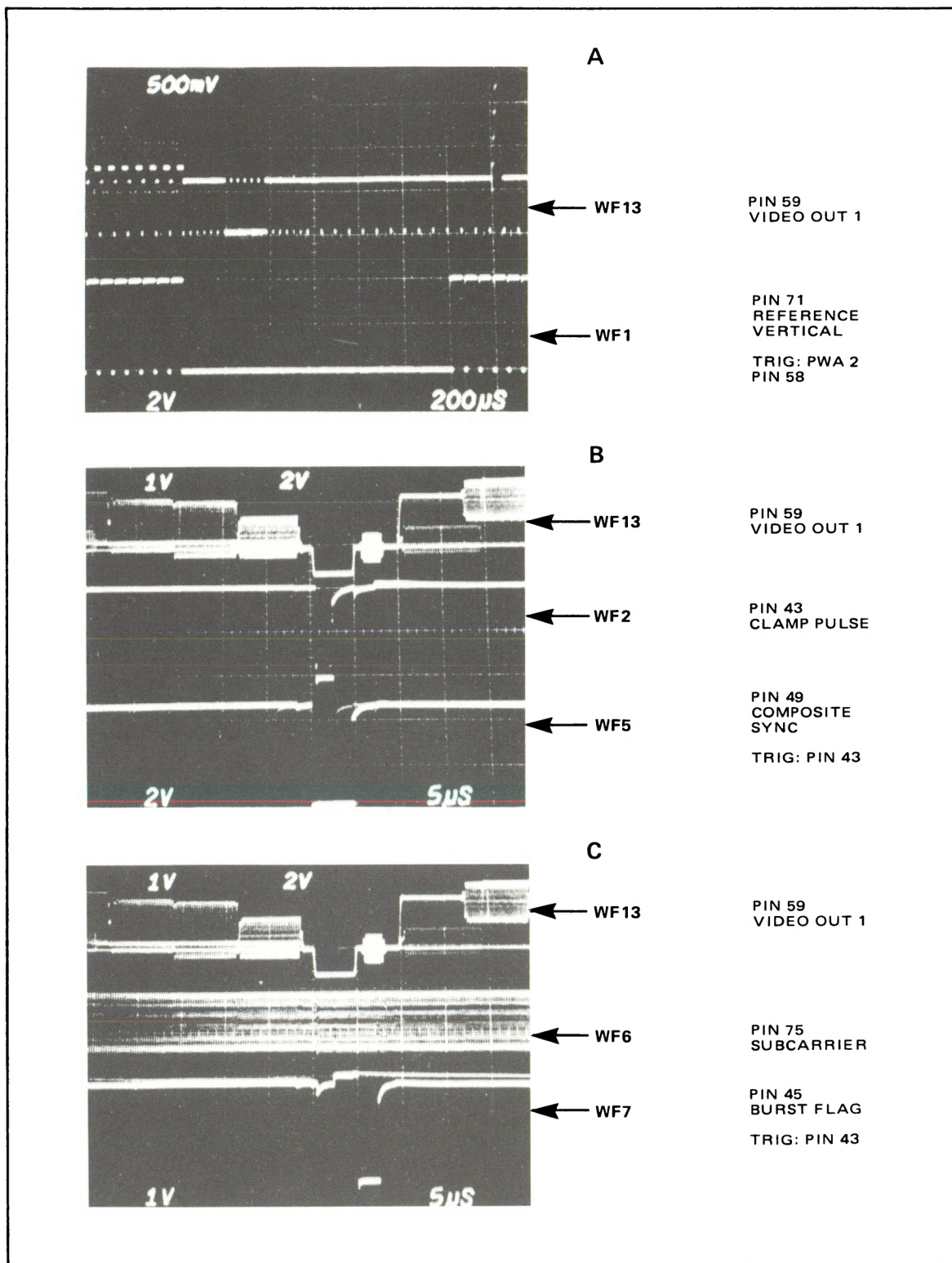


Figure 14-4. Video Output PWA 14 Waveforms (Sheet 1 of 3)

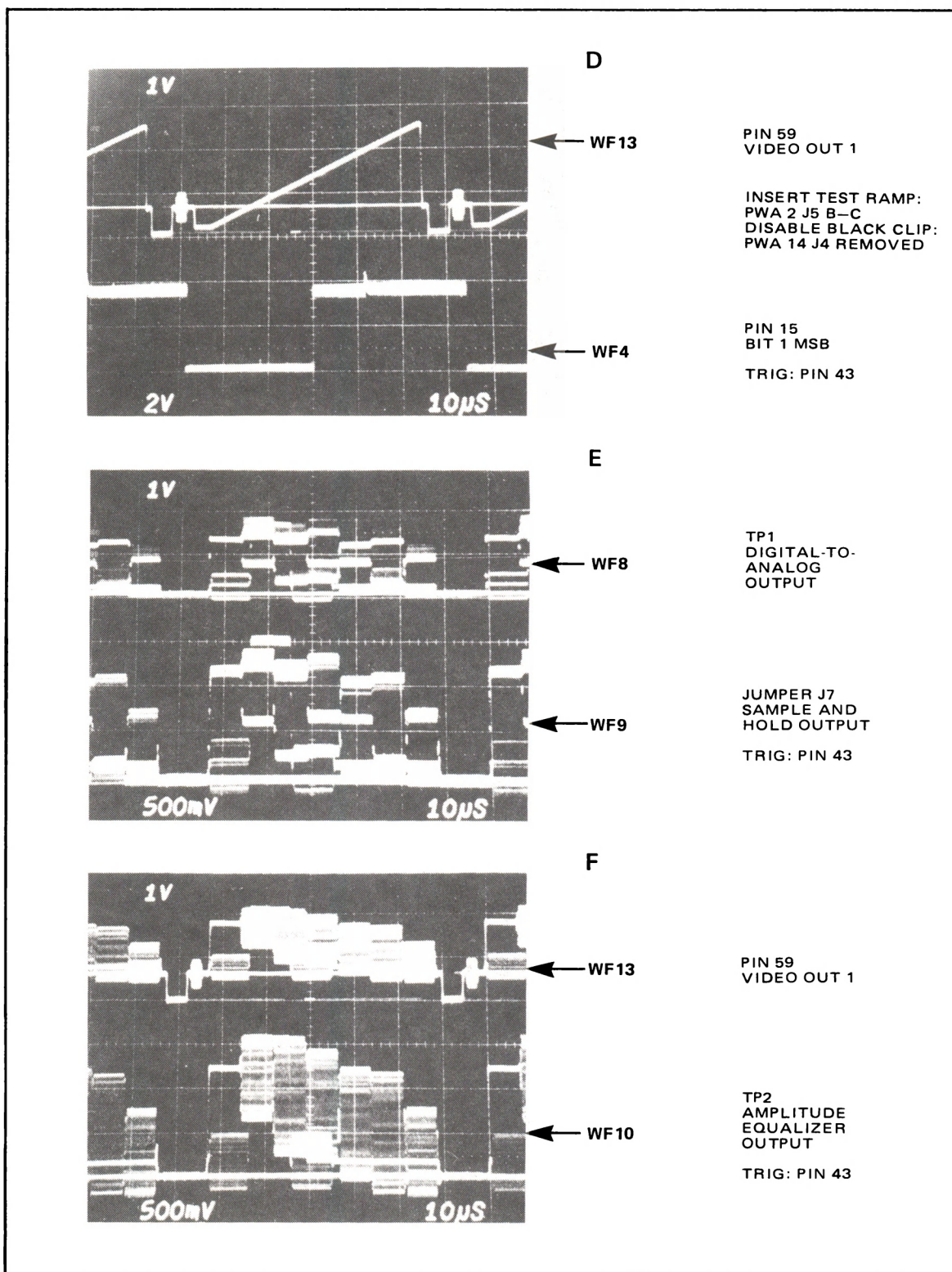


Figure 14-4. Video Output PWA 14 Waveforms (Sheet 2 of 3)

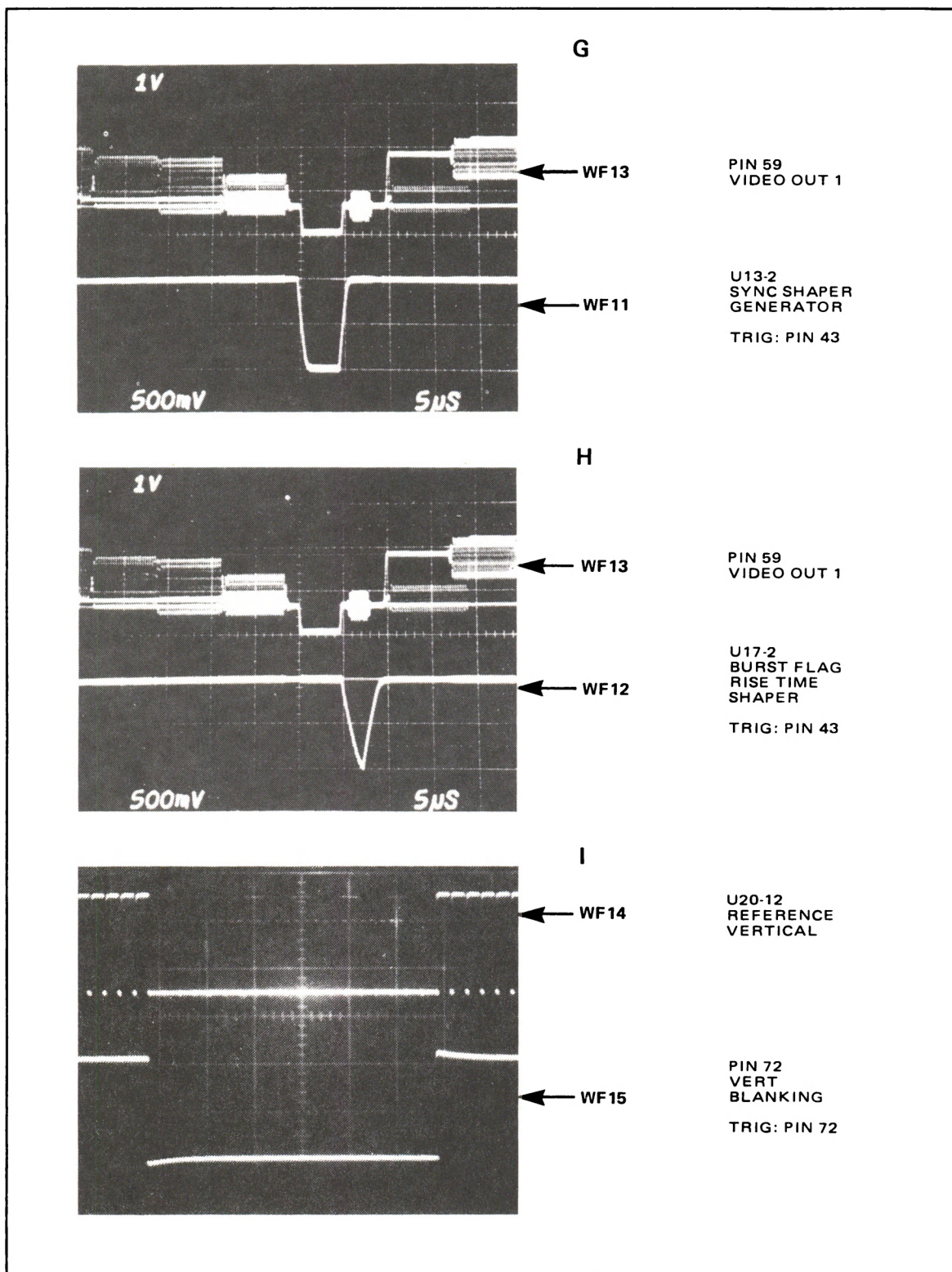


Figure 14-4. Video Output PWA 14 Waveforms (Sheet 3 of 3)

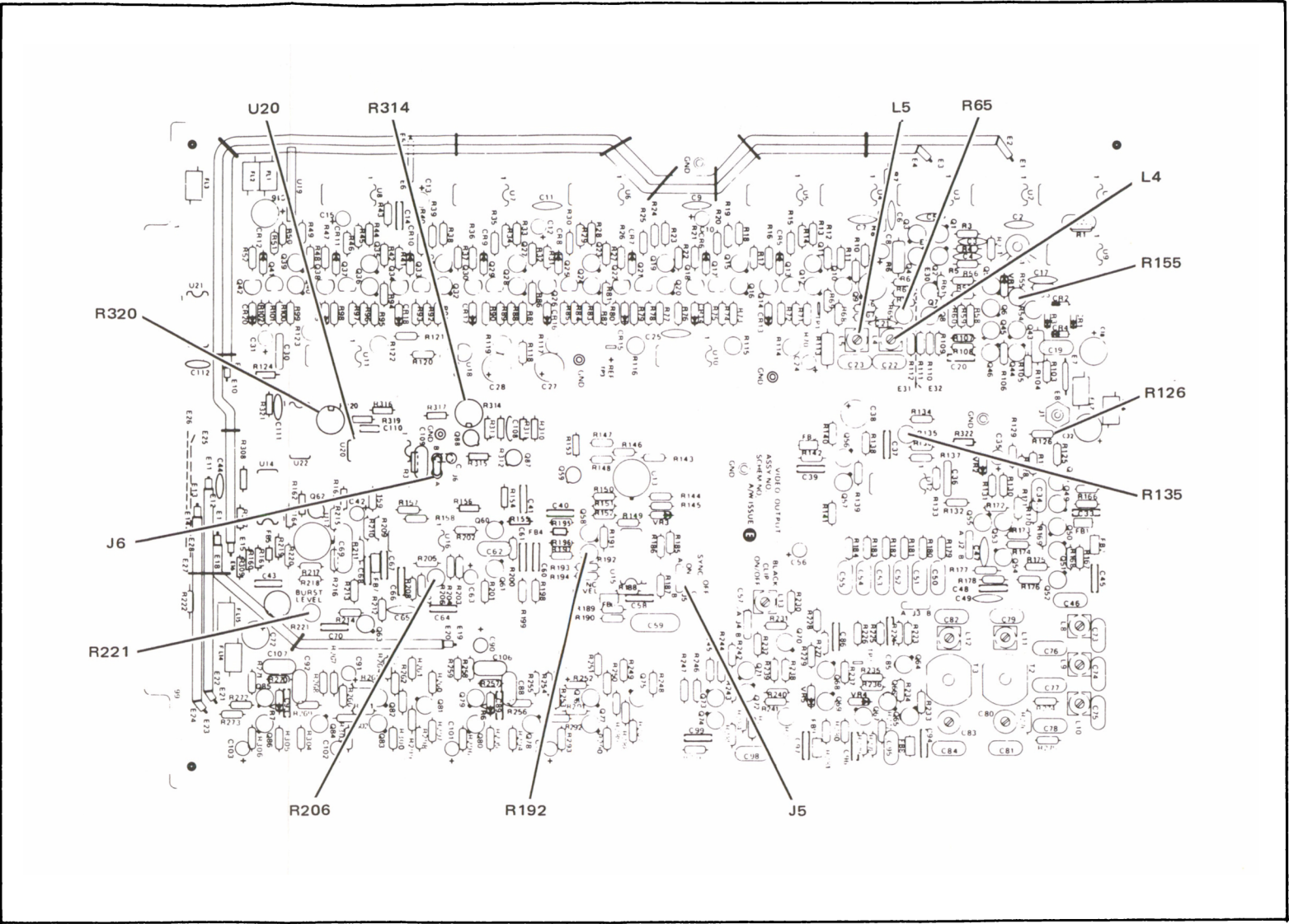
PWA 14 Jumpers		
Jumper	Position	Function
J1	RF connector	Factory Test Test only – insert sweep to interpolation filter
J2	A-B Removed	Factory Test Normal Test–removes clamp pulse
J3	A-B	Factory Test Normal Test–removes phase equalizer
J4	A-B Removed	Black Clip Normal–black clip on Test– removes black clip
J5	A-B	Composite/Non-Composite Normal–composite sync on VIDEO OUT 2
J6	A-B B-C	Factory Test Normal Test–inhibits V-internal clamp
J7	A-B Removed	Factory Test Normal Blocks D/A video. Used in conjunction with J1

PWA 14 Adjustable Components	
Component	Function
C80*	Interpolation filter
C83*	Interpolation filter
L4	Blanking insertion filter
L5	Blanking insertion filter
L8*	Interpolation filter
L9*	Interpolation filter
L10*	Interpolation filter
L11*	Interpolation filter
L12*	Interpolation filter
L13*	Differential phase below black
R54**	Frequency response
R55	DC balance
R65	Blanking insertion level
R114*	MSB gain
R115*	2nd MSB gain
R116*	3rd MSB gain
R117*	4th MSB gain
R119	5th MSB gain
R122	6th MSB gain
R123	7th MSB gain
R135	Black clip
R192	Sync level
R206	Burst balance
R221	Burst level
R282*	Differential gain below black
R314	Vertical clamp level
R320	Vertical clamp timing
T2*	Interpolation filter
T3*	Interpolation filter

* Factory adjustment only.

** R54 adjusts the high end frequency response (chroma level) and should only be adjusted using a spectrum analyzer with 0.1 dB accuracy.

PWA 14 Test Points	
Test Point	Signal
TP1	D/A video
TP2	Non-comp video
TP3	+ 5 V



PWA 14 Component Locator

Figure 14-5.
Test Points, Jumpers, Adjustable Components, Component
Locator, Video Output PWA 14

PART II

SECTION 15

SYNC GENERATOR PWA 15

DESCRIPTION AND MAINTENANCE

15-1 INTRODUCTION

Refer to the following documents in the *TBC-3 Parts Lists and Schematics* manual.

Assembly No. 1405186 (12-line)

Assembly 1463659 (16-line)

Schematic No. 1405188 (12-line)

Schematic 1463661 (16-line)

The 12-line version Sync Generator PWA is used with VPR-2B and the 16-line version is used with VPR-3 (video tape recorders).

The following figures, to which PWA descriptions and maintenance procedures refer, are located at the end of this section as follows:

- Figure 15-3, overall block diagram
- Figures 15-4 to 15-11, simplified schematics
- Figure 15-12, waveforms
- Figure 17-13, maintenance data

Sync Generator PWA 15 function summary:

- Using reference video input, Sync Generator PWA 15 develops composite sync, burst key, and blanking signals for insertion in the time-base-corrected video in Video Output PWA 14.
- 14.3-MHz LC (for monochrome and nonservoed capstan modes of operation) and crystal (for all other modes) oscillators are the source for two TV sync generator ICs (normal and advanced sync) as well as the analog 3.58 MHz to Video Output PWA 14 and TTL 3.58 MHz to Memory Control PWA 6 by way of velocity compensator on PWA 13.
- The 14.3-MHz oscillators are genlocked by an error signal which results from digital comparison of H-rate sync with the burst position.
- A separate loop with its own TV sync generator integrated circuit provides advanced reference sync for VTRs that do not have internal capability for both fixed and floating 5-1/2-line advance. Floating 5-1/2-line advance is mainly used on units using tach lock drum servos.

TBC-3

15-2 DESCRIPTION

Note

The following discussion pertains to the 12-line and 16-line versions of Sync Generator PWA 15. Any differences are noted in the text.

Sync Generator PWA 15 produces the read timing signals that recover digitized video from memory at reference 3Fsc rate. Off-tape video is digitized and entered into memory at the tape velocity rate. Reading data out of memory at a reference rate is the basis of the digital time-base correction process. In addition, Sync Generator PWA 15 produces horizontal and vertical sync, blanking, and burst. These are inserted into the time-base-corrected analog video in Video Output PWA 14 to form the composite video output of the TBC.

Sync Generator PWA consists of four basic functional areas: reference video processing, reference oscillator and control processing, output sync and blanking, and advance reference. These are shown in the simplified block diagrams of Figure 15-3. The reference processing portion of sheet 1 illustrates how reference video is processed to extract the basic timing signals (burst crossing, H-sync, vertical color frame) for servo loops within the sync generator. Figures 15-4 and 15-8 are detailed diagrams of these circuits. The reference oscillator and control portion of Figure 15-3, sheet 1, shows the 14.3-MHz reference oscillator which becomes the source for read timing signals to the TBC. Note that control panel controls are part of the basic servo loop of which the phase comparator, the 14.3-MHz oscillator, and the sync generator IC are central elements. (See Figures 15-6 and 15-10.) Note also that signal HD2 (horizontal drive), at the input to the phase comparator, is from the sync generator IC, and that the signal 130H (hex) is the 2-MHz clock for that IC. This is the basic phase comparator loop around which the sync generator operates and is shown in greater detail in Figures 15-5 and 15-9. The third functional area is shown on the output sync and blanking portion of Figure 15-3, sheet 2, an overview of the sync generator IC and the sync input signals.

Figure 15-3, sheet 2, also contains a simplified block diagram of the advanced reference sync generator IC loop for nonservoed capstan VTRs. This information is presented in more detail in Figures 15-7 and 15-11. The simplified schematics and associated waveforms (Figure 15-12) supplement the following information regarding sync generator operation.

15-3 Reference Video Sync Processing

EIA standard RS170A expresses the relationship of horizontal sync to subcarrier as the zero crossing of subcarrier relative to the leading edge of horizontal sync. This is equivalent to considering the subcarrier as the reference, and the leading edge of horizontal sync coincident with a zero crossing of subcarrier. Because the horizontal line contains 227-1/2 cycles of subcarrier, the phase of the leading edge of horizontal sync relative to subcarrier changes by 180° (140 ns) on alternate lines. The subcarrier does not shift in phase (relative to itself) from one line to the next; nor does the sync pulse shift. Because subcarrier frequency is an odd multiple of one-half the horizontal rate, the zero crossing coincident with the leading edge of sync will be positive-going on one line and negative-going on the next. This relationship will continue for each alternate line. (See Figure 15-1.)

The phase relationship of vertical sync relative to subcarrier, and color frame relative to carrier is much more subtle. As noted above, the phase of H-sync to subcarrier changes on alternate lines. Each field contains 262-1/2 lines (59,718.75 cycles of subcarrier). Each frame contains 525 lines (119,437.5 cycles of subcarrier). Since the frame ends on a half-cycle, it is apparent that the phase of the vertical rate relative to subcarrier will change by 180° each alternate frame. (See Figure 15-2.)

The phase relationship of 7.8-kHz (as it is used in the TBC) to horizontal sync changes at the transition between each even-numbered field and the following odd-numbered field of the color frame, between frame A and frame B of the color field, and between field IV and field I of the following color frame.

15-4 Burst Crossing

See Figure 15-4 or 15-8. Since horizontal sync changes phase by 180° (140 ns) relative to subcarrier on alternate lines, the frame 7.8 kHz shifts burst-crossing enable by 140 ns on each alternate line. This ensures that the selected burst crossing is always detected at the zero crossing on a positive-going transition. If the frame 7.8 kHz comes up in an incorrect phase of startup, a circuit consisting of U34-5 and U35-6 reclocks the frame 7.8-kHz flip/flop to the correct phase and is inactive thereafter. Once the correct phase is established, the 7.8-kHz flip/flop is clocked by delayed H from U49-6. (See Figure 15-2.)

15-5 Frame Lock

See Figure 15-4 or 15-8 and waveforms A-D and M-Q. Frame-lock circuitry provides a third phase-locked loop to complete the synchronization of the composite video signal. The vertical broad pulse detector circuit uses the characteristics of the difference between the vertical blanking interval signals of field I and field II of the video frame to identify field II. The broad pulse gate (waveform 26) identifies the third serration of the vertical sync signal. The 2 x H rate suppressor permits only the horizontal sync pulses to pass. The H-sync for line 5 of the vertical blanking interval is only coincident with the third serration in field I and field III of the color frame. The three signals, 2 x H rate suppressor, third broad pulse gate, and 7.8 kHz are ANDed to produce the color frame pulse (see waveform 27) to the vertical reset counter and the frame rate reset circuit.

As illustrated in Figure 15-1, the frame 7.8-kHz signal changes phase relative to horizontal sync at the transition between frame A and frame B of the color frame. Therefore, the color frame reset pulse represents either the first or third field of the color frame, depending on the condition of the flip/flop at startup.

The first equalizing pulse of the first and third fields of the color frame is coincident with the horizontal sync of line 1 of the field. This is not true of the second and fourth fields. The equalizing pulse detector takes advantage of this condition to produce a pulse at the start of field I and of field III. The pulse from the frame detector (field II or IV) sets the frame rate reset flip/flop. The pulse from the equalizing pulse detector clocks the flip/flop. The result is a color frame rate reset 15-Hz pulse to the reference 3.58-MHz quad phase circuit and the reference 7.8-kHz circuit, locking the reference output synchronizing signals to

the color frame. It should be noted that the 14.3-MHz oscillator which is phase-locked (genlocked) to the station master H-rate, clocks the reference 3.58-MHz divide-by-four circuit. One phase of the 3.58-MHz signal reclocks the H-drive from the sync generator integrated circuit to the horizontal phase comparator. The 14.3-MHz oscillator, which is normally phase-locked to station master burst crossing, provides a 2-MHz clock via the divide-by-seven counter to the sync generator integrated circuit. The sync generator integrated circuit provides the output synchronizing signals which are a part of the various feedback loops of the Sync Generator PWA. Therefore the outputs of the Sync Generator PWA are firmly locked to all components of the station reference video.

15-6 Vertical Blanking and Reset Counters

See Figure 15-4. The broad pulse gate from U43-7 provides a high to the D-input of U53-2. The line 5 H-pulse clocks it through to clear the vertical blanking counter U63 to zero. The counter is clocked by H-rate pulses from U34-13. When the Q_D output of U63 goes low on count 256, one-shot U62 is triggered at the beginning of the vertical blanking interval time. This signal inhibits the horizontal phase comparator, the burst present and burst crossing detectors, and the genlocked indicator during the vertical blanking interval. The 14.3-MHz oscillator must, therefore, freewheel for approximately 22 lines.

The vertical reset counter (U45/U56/U55) is a 12-bit binary counter capable of counting 4,096 clock pulses, if started at a count of zero. To achieve the desired counts of less than this amount, some of the programmable inputs are hard-wired either high or low. Other inputs are programmed by signals from the VTR. The programmed number is loaded when the color frame rate pulse pulls the load inputs low. The H-rate pulse clocks the counter until the carry output resets the sync generator integrated circuit. The counter rolls over to zero and continues to count, but is reset four frames later before another carry can be generated. In the normal condition, vertical reset occurs five horizontal lines less than one complete field after the start of the count. The color frame rate pulse occurs 5-1/2 to 6 lines into the vertical interval. With a minus 5-line count, sync generator IC is reset at the beginning of the vertical blanking interval once during the color field. The zero offset signal from the VTR is used in E-E operation, or direct electronic transfer of signal. When zero offset is low (active) the count will be 263 H-pulses or one complete field. When sync retard is low (active) the VTR is in edit mode, recording video and reading video 120° (approximately 1-1/3 fields) later on the read head. The 1-1/3 field plus 6-H count for the vertical reset signal compensates for the 1/3-field delay of the read head.

15-7 Basic Phase Comparator Loop

Follow the basic loop through Figures 15-5 and 15-6 or 15-9 and 15-10. The heart of the Sync Generator PWA is the MM5321N (U14) large scale integration (LSI) sync generator and the phase-locked loop (genlock) necessary to lock the LSI circuit to the station master reference video in. The loop contains two oscillator circuits; one is crystal-controlled and is used for color video with servoed capstan VTRs, the other is an LC circuit and is used with nonservoed capstan VTRs and/or with monochrome video. If burst is not detected for more than approximately 12 lines, the LC oscillator will be automatically switched in.

The reference time base for control and sync signals produced by the Sync Generator PWA is established by either of two 14.3-MHz oscillators; one is crystal controlled and the other is an LC circuit. The crystal oscillator is used when the TBC is allied to a servoed capstan VTR such as the Ampex VPR series. If the optional TBC-3 noncapstan servo control panel is installed, the LC oscillator is active when the TBC-3 is used with a nonservoed capstan VTR. In this mode of operation, time-base errors continue to be corrected on a line-by-line basis, but the vertical rate time-base errors are preserved because the 14.3-MHz LC oscillator is slaved to the vertical rate time-base error. If the resulting video is recorded on a servoed capstan VTR, passed through the TBC a second time, and re-recorded on a servoed capstan VTR, the final tape will be fully time-base corrected.

The H-drive output of the Sync Generator PWA integrated circuit is applied to one input of a horizontal phase comparator. The other input is referenced to a selected H-sync. For color video, a selected burst crossing is used. For monochrome operation, reference H-sync is selected. The resulting error voltage is applied to the 14.3-MHz oscillator circuit. The phase-corrected 14.3 MHz is applied to a divide-by-seven counter and a divide-by-four counter. The divide-by-seven counter generates a 2-MHz clock as the basic reference for the Sync Generator integrated circuit. The divide-by-four counter produces a 3.58-MHz signal. The Sync Generator integrated circuit requires vertical reset input in order to provide composite sync that is slaved to the reference video in.

15-8 Advanced Reference Sync

See Figure 15-7 or 15-11 and waveforms 10 and 22. A second MM5321N (U15) sync generator integrated circuit generates a VTR-advanced reference signal to provide a 5-1/2-line advance of off-tape video from the VTR with respect to the read function of the TBC-3 Memory PWAs. The advanced reference is required for operation with the VPR-3 but is not required for the VPR-2B, as this VTR generates its own advance reference sync. The vertical drive signal from the first sync generator integrated (U14) circuit is phase-compared with the tape vertical signal from the Tape VCO PWA 5. The resultant error voltage provides a servoed advanced vertical reset to the second sync generator integrated circuit. If a nonservoed capstan VTR is used, the same error voltage will be applied to the LC 14.3-MHz oscillator. If the TBC is used with a VTR which cannot accept a servoed 5-1/2-line advance, a fixed 5-1/2-line advance may be accessed by jumper J1 on the Sync Generator PWA.

The VPR-3 requires advance reference sync which is fed from the TBC-3 to the VPR-3 via a separate BNC connected cable. For VPR-3 use, jumper J1 (16-line sync generator) is set to the fixed advanced A-B position. This permits the period of sync retime one-shot U64-12 to be set by the adjustment of advance sync control R262. The control is set by placing the VPR-3 in play mode and adjusting R262 so that the green LED on the Memory Control PWA is lit, indicating there is neither a read or write overload condition. This corresponds to approximately an 11-line sync advance. Also for VPR-3 use, advance reference select jumper J2 is placed in the B-E (sync and subcarrier) position. This enables the advanced reference sync and subcarrier parameters to be adjusted. Burst level control R263 is adjusted to set burst amplitude equal to sync (287 mVp-p). Inductor L12 is used to trim $S_{cH\Phi}$.

TBC-3

15-9 Color Lock Indicators

When the 12-line sync generator is used, the GEN LOCK indicator on the TBC-3 control panel illuminates if the TBC-3 is genlocked. When the 16-line sync generator is used, the GEN LOCK indicator illuminates when the TBC-3 is genlocked and is receiving an RS170A standard signal. The PWA front-mounted color lock LED DS2 illuminates when the TBC-3 reference video input signal is a color signal.

15-10 MAINTENANCE

See Figures 15-12 and 15-13 for waveforms, component locator diagram, jumper, test-point, and adjustable-component summaries called out in these procedures.

Before undertaking any adjustments to the Sync Generator PWA review the system alignment sequence of Table 3-2 and the tape/reference test loop discussion of paragraph 3-6 for a general understanding of the scope of these field adjustments.

Consult reference waveforms and interconnect data on the simplified schematics to confirm normal operation of the interactive functions of the Sync Generator and interactive functions between it and other PWAs before making any adjustments. For example, some adjustments here require a normal signal from Video Output PWA 14.

15-11 SYNC GENERATOR ALIGNMENT

The Sync Generator PWA is set at the factory for operation with reference video which conforms to the RS170A standard for burst-to-H sync phasing. The following procedure may be used to return the TBC to the original RS170A standard or to realign the sync generator to a nonstandard reference. Using a nonstandard reference may require adjustment of the PWA 4 tape H burst/sync phase (R1) to nonstandard for properly color-framed tape interchange. It may also be necessary to perform the tape H-sync (write) timing of paragraph 3-14.

Whatever burst/sync phase is used, it must be maintained throughout the Sync Generator PWA alignment.

15-12 Input Sync and Chroma Processing

15-13 Initial Setup

- STEP 1 Use the basic tape/reference test loop setup with a color-bar signal at standard level to TAPE VIDEO IN. The waveform monitor and vectorscope will be used later in the procedure.
- STEP 2 With power off extend the Sync Generator PWA.
- STEP 3 Turn power on and verify that control panel GEN LOCKED indicator is on.

15-14 Burst and Chroma Filters

- STEP 1** Connect oscilloscope as follows: CH1—TP 1 (filtered video, nominal 5 Vp-p). Trigger on internal.
- STEP 2** Adjust L1 (L11 16-line system) video low-pass filter for minimum subcarrier on steps.
- STEP 3** Verify TTL-level composite sync at TP3.
- STEP 4** Verify a 0.25-Vp-p chroma level ($\pm 10\%$) and a 0.475-Vp-p burst level ($\pm 10\%$) at TP2.

15-15 Burst Crossing Selector

- STEP 1** Connect oscilloscope as follows: CH1—TP11 (reference video); CH2—TP12 (comparator reference burst). Trigger on TP3 (composite sync).
- STEP 2** Verify that the pulse on CH2 (TP12, approximately 300 ns) occurs near center of burst (TP11). See WF1/WF5(B).
- STEP 3** Connect oscilloscope as follows: CH1—TP13 (delayed reference sync); CH1—TP12 (comparator reference burst). Trigger on signal generator H drive. It is crucial to display the double pulse as shown in WF34/WF35(V). Use oscilloscope delayed sweep and chop mode.
- STEP 4** Adjust R225 (alternate line 140 ns) for 140 ns between positive edges of two pulses on CH2 (TP12).
- STEP 5** Adjust R223 (reference sync/burst calibration) for center of second pulse on CH2 (TP12) to occur at leading edge of pulse on CH1 (TP13). See WF34/WF35(V).
- STEP 6** Verify that indicator DS1 (reference sync/burst-PWA edge) is on. Note that DS1 will come on at more than one point as R223 is adjusted. For normal color framing, indicator must be on as noted above for the odd field burst crossing. If indicator is not on, sync generator may alternately select any burst crossing, making read timing unstable.
- STEP 7** Verify the following signals:
- a. TP7 (reference burst)—H rate, nominal 400-ns width.
 - b. TP6 (14.3 MHz) — see WF13(G).

15-16 Color/Mono Lock

- STEP 1** Connect oscilloscope as follows: CH1—TP15 (crystal oscillator error). Trigger on line.
- STEP 2** Adjust L9 (crystal oscillator frequency) for 0 Vdc.

TBC-3

- STEP 3** Verify that error voltage at TP15 shifts and then returns to 0 Vdc for each of the following conditions:
- a. Switch power off and on.
 - b. Momentarily ground PWA 15 Pin 26.
 - c. At signal generator turn burst off and on.
 - d. Disconnect and reconnect reference video at input.
- Repeat as required to ensure proper lock.
- STEP 4** Connect oscilloscope as follows: CH1—TP14 (LC oscillator error). Trigger on line.
- STEP 5** Switch burst off at the signal generator.
- STEP 6** Adjust L3 (LC oscillator frequency) for 0 Vdc.
- STEP 7** Verify that error voltage at TP14 responds opposite to conditions a, b, c, and d in step 3 above.

15-17 Preliminary Sync and Chroma Timing

- STEP 1** Return burst to the input video.
- STEP 2** Connect oscilloscope as follows: CH1—TP8 (reference 3.58 MHz). Trigger on internal.
- STEP 3** Adjust R173 (chroma symmetry) for a symmetrical square wave. See WF16(I). Because this signal is terminated it is below normal TTL level.
- STEP 4** Connect oscilloscope as follows: CH1—TP9 (subcarrier). Trigger on internal.
- STEP 5** Adjust R226 (subcarrier symmetry), L7, and L8 (subcarrier filter) for peak output of the 3.58-MHz sine wave. See WF17(I).
- STEP 6** Verify a symmetrical 7.8-kHz square wave at U21-10.

15-18 Color Frame Detector

Do not adjust R70 (third broad pulse detector level) until the four fields and the position of the frame pulse are clearly identified in the context of the procedure and need for adjustment is definitely established. Make certain also that burst crossing is properly calibrated and the reference sync/burst indicator is on.

- STEP 1** Connect oscilloscope as follows: CH1—U43-7 (broad pulse gate). CH2—U43-2 (integrator). Trigger on PWA Pin 69 (or signal generator V drive).
- STEP 2** Using delayed sweep, scan four fields of video. Positive edge of pulse on CH1 should be coincident with center of third (from the bottom)

transition on ramp on CH2 for the odd field. Normal condition is shown in WF25/WF26(P). If CH1 pulse occurs anywhere on the third transition, do not adjust R70, but proceed to next step.

- STEP 3** Connect oscilloscope as follows: CH1—TP11 (reference video input). CH2—U52-8 (color frame pulse). Trigger on PWA Pin 69.
- STEP 4** Desired display is shown in WF27(Q). Use delayed sweep and scan at least four fields. Color frame pulse is difficult to see and should occur on only one of four fields.
- STEP 5** If color frame pulse is at vertical third broad pulse, do not adjust R70; it will jump to fourth broad pulse of even field. If frame pulse is coincident with fourth broad pulse, adjust R70 for coincidence on third broad pulse. Recheck ramp coincidence of step 2.
- STEP 6** As a further check on validity of adjustment, compare reference video against TBC video out and note field-for-field coincidence of vertical interval sync pulses.

15-19 Output Sync and Blanking

15-20 Initial Setup

Continue the setup of the first part of this Sync Generator PWA procedure but select a color black signal at the generator and leave PWA in its slot for adjustment of blanking controls on the PWA edge.

15-21 Horizontal Blanking

H-blanking leading/trailing edges may be set at any time to the user's requirement but should be checked at this stage to ensure that any misadjustment of the edges does not interfere with burst adjustments in the next part of the procedure.

- STEP 1** Connect oscilloscope or waveform monitor to VIDEO OUT 1 and display horizontal interval.
- STEP 2** Turn BLACK LEVEL control fully clockwise to observe pedestal.
- STEP 3** With reference to H-interval illustration in proposed RS170A standard (Figure 2-1 in Part I) adjust R46 (H-blanking leading edge) for a horizontal front porch between 1.0 and 1.2 μ s.

Note

This is not RS170A standard. A very wide leading edge established here may interfere with rise-time adjustments of L4, L5, and R65 on the Video Output PWA. Most users keep the blanking narrower than RS170A standard to avoid losing picture video in the many production steps and to avoid contributing to a widening of the sync interval of the broadcast signal.

TBC-3

STEP 4 Adjust R45 (H-blanking trailing edge) for an interval (sync leading edge to blanking end) between 9.5 and 9.9 μ s.

STEP 5 Verify that the 50% point of first cycle burst lags negative edge of H-sync between 5.2 and 5.4 μ s.

15-22 Vertical Blanking

Normal speed vertical blanking is set for the user's requirement and the trailing edge may be set as far down as line 10 to unblank any vertical interval test and control signals. It is usually set for blanking of the line preceding such signals and may also be set as high as line 25 to blank out signals in lines 1-25. In slow-motion operation, test and control signals are blanked out (to prevent interference by the irregular field repetition of the slow-motion process).

Adjustment may be made with the basic tape/reference test loop or during tape playback with the VTR. In either case, slow-motion control of the VTR will be used for the R65 (slow-motion vertical blanking) adjustment.

STEP 1 Connect oscilloscope or waveform monitor to VIDEO OUT 1 and display vertical interval.

STEP 2 Turn BLACK LEVEL control clockwise.

STEP 3 VITS blanking adjustment

- a. Nonsync head system: Apply a video signal with VITS on line 16 (or user's preferred line position) to TBC-3. Adjust R64 (normal V-blanking) so that first line after line 16 is first unblanked line.
- b. Sync head system: Adjust R64 for any line desired after line 10 in the blanking interval.

Note

Unblanked lines will show a pedestal, blanked lines will not.

STEP 4 Switch to slow motion at the VTR.

STEP 5 Adjust R65 so that line with VITS signal is blanked out through its pedestal.

Note

Adjustment of R65 here must be coordinated with the adjustment of R320 (vertical clamp timing) on Video Output PWA 14. See Paragraph 14-11.

STEP 6 Return BLACK LEVEL to unity.

15-23 Output Subcarrier and Chroma Phasing

- STEP 1** Continue the tape/reference test loop setup and add waveform monitor and vectorscope for input/output comparison. Use a 75% color-bar signal at standard level and RS170A sync/burst phase (or normal phase of the facility). This procedure assumes normal operation in previous Sync Generator PWA test stages.
- STEP 2** Verify the following conditions:
- Indicator DS1 (reference sync/burst phase calibration) is on.
 - Reference 3.58-MHz signal at PWA Pin 79 (TP8) is a symmetrical square wave as adjusted by R173 (chroma symmetry).
 - Subcarrier signal at PWA pin 75 (TP9) is set for maximum level as adjusted by R226 (subcarrier symmetry), L7 and L8 (subcarrier filter).
 - Quad phases are available at U49-8, -12, -2, and -4 as shown in WF14/WF15(H). The four phases may also be checked by viewing PWA pin 79 (reference 3.58 MHz) with vectorscope (locked to external reference phase) and shifting jumper J4 in following sequence: B-D, B-E, B-C, and B-A; be sure to return jumper to its original position.
- STEP 3** While observing input/output video signals on waveform monitor (A-B mode), superimpose H-sync leading edges within a subcarrier cycle with HORIZ PHASE control on control panel.
- STEP 4** Observe chroma/burst on the vectorscope (locked on external subcarrier) and adjust SUBCARRIER PHASE on the control panel so that burst vectors are aligned. Bursts seen on waveform monitor will nearly cancel.

Note

If bursts cannot be aligned or either HORIZ PHASE or SUBCARRIER PHASE are not near their center positions, an adjustment of PWA edge control R208 (subcarrier phase) will shift the subcarrier phase without affecting H-sync leading edge.

- STEP 5** Adjust R208 (subcarrier phase) to align burst vectors. If more range is required, reposition jumper J3. Switch power off to change jumper and then adjust R208 with PWA in the cage.
- STEP 6** Turn control panel SUBCARRIER PHASE through its range and confirm a shift of 370° as viewed on the vectorscope. If the range is not 370° proceed as follows:
- With power off extend PWA.
 - Adjust R199 (subcarrier phase range) to achieve a 370° shift of SUBCARRIER PHASE control.
 - Return PWA to cage and restore subcarrier phase alignment determined in step 5.

TBC-3

STEP 7 Turn CHROMA PHASE control to center detent position.

STEP 8 Adjust R146 (chroma phase—PWA Edge) so that chroma vectors are aligned on vectorscope. If more range is required, select a new position for J4. Remember to switch power off to change the jumper and to adjust R146 with PWA in cage.

Note

If changes to the write timing at the Tape H/Tape VCO PWAs are made subsequent to this test it may be necessary to recheck this step.

STEP 9 Verify that for both the control panel CHROMA PHASE and R146 turned simultaneously to either extreme, there is no picture shift. If there is a horizontal shift, proceed as follows:

- a. With power off select opposite position (A-B or A-C) for jumper J5.

Note

There is no normal position for J5. It is used to ensure that the sync generator phasing does not create an unwanted H-drive/subcarrier phase coincidence on the Memory Control PWA.

- b. Recheck CHROMA PHASE/R146 extremes for no horizontal picture shift.
- c. Return PWA to rack.

STEP 10 Restore chroma vector alignment determined in steps 7 and 8.

STEP 11 Check control panel CHROMA PHASE range as follows:

- a. Mechanically center the unity chroma phase trim control (control panel top/center).
- b. Set CHROMA PHASE control to center unity detent position.
- c. Adjust vectorscope variable phase control so yellow vector is on convenient reference point on graticule.
- d. Turn CHROMA PHASE control and note amount of vector swing on either side of reference.
- e. Set CHROMA PHASE to center unity detent position.
- f. Adjust unity trim control in direction of largest swing.
- g. Reestablish a yellow vector reference.
- h. Repeat substeps 11c through 11g until the vector swings approximately 20° in either direction from reference setting.

STEP 12 Return vectorscope to external lock and repeat steps 7 and 8.

- STEP 13** Set CHROMA PHASE to center detent position and adjust unity trim for coincidence of chroma vectors. This step completes phasing of TBC to system reference.
- STEP 14** This step is for VPR-3 use only. Check $ScH\Phi$ output of the TBC-3 as follows:
- Feed a video reference signal to REFERENCE VIDEO IN on TBC-3.
 - Connect VIDEO 1 or VIDEO 2 OUT of TBC-3 to VIDEO IN of VPR-3.
 - Push VPR-3 front panel $ScH\Phi$ control knob to unity (in) position.
 - Note $ScH\Phi$ on $ScH\Phi$ meter. If $ScH\Phi$ is not within $\pm 40^\circ$, adjust subcarrier phase control R208 on Sync Generator PWA to center meter.
 - Connect VIDEO IN of VPR-3 to VTR ADVANCED REFERENCE output of TBC-3.
 - Note $ScH\Phi$ of advanced video on VPR-3 $ScH\Phi$ meter. If $ScH\Phi$ is not $\pm 40^\circ$, adjust $ScH\Phi$ trim L12 to center the meter.
 - Connect oscilloscope to TP4 (advanced reference) and trigger scope internal at horizontal rate.
 - Adjust advance sync burst level control R263 to set burst level amplitude equal to sync level (287 mV).

15-24 Advanced Reference Sync for Heterodyne Use

Normally there is no need for adjustment of the advance reference when the TBC-3 is used with a heterodyne VTR. Refer to paragraph 3-18 for guidance to operation with heterodyne and nonservoed capstan VTRs.

15-25 Output Sync/Burst Phase (Non-RS170A)

As factory calibrated, the Sync Generator PWA inserts sync on corrected video that conforms to proposed standard RS170A for sync/burst phasing. The use of OUTPUT SYNC/BURST control R240 allows matching standard RS170A output to any video source where a displacement of H-sync phase is required without affecting subcarrier phase. This procedure sets up range and symmetry for output sync/burst control, R240. To phase the TBC to the reference source refer to paragraph 3-12 in the system maintenance section.

- STEP 1** Use tape/reference test loop with standard level 75% color bars and RS170A burst/sync phase.
- STEP 2** With power off, extend Sync Generator PWA 15.
- STEP 3** Position jumper J6 to B-C.
- STEP 4** Connect oscilloscope to U74-13; trigger on internal.
- STEP 5** Adjust R72 (symmetry) for a symmetrical square wave.

- STEP 6** Connect oscilloscope to U74-12; trigger on internal.
- STEP 7** Preset R240 fully clockwise.
- STEP 8** Adjust R245 (range) for a positive 200-ns pulse.
- STEP 9** Connect oscilloscope to VIDEO OUT 1; trigger on signal generator H-drive output.
- STEP 10** Use delayed sweep and display leading edge of the H-sync.
- STEP 11** Adjust R240 through its range—at least 270 ns but no more than 300 ns.
- STEP 12** Adjust R245 to limit range of R240 to 270-300 ns.
- STEP 13** Return J6 to A—B unless TBC is to be phased to a non-RS170A source as outlined in the system maintenance section, Part I.

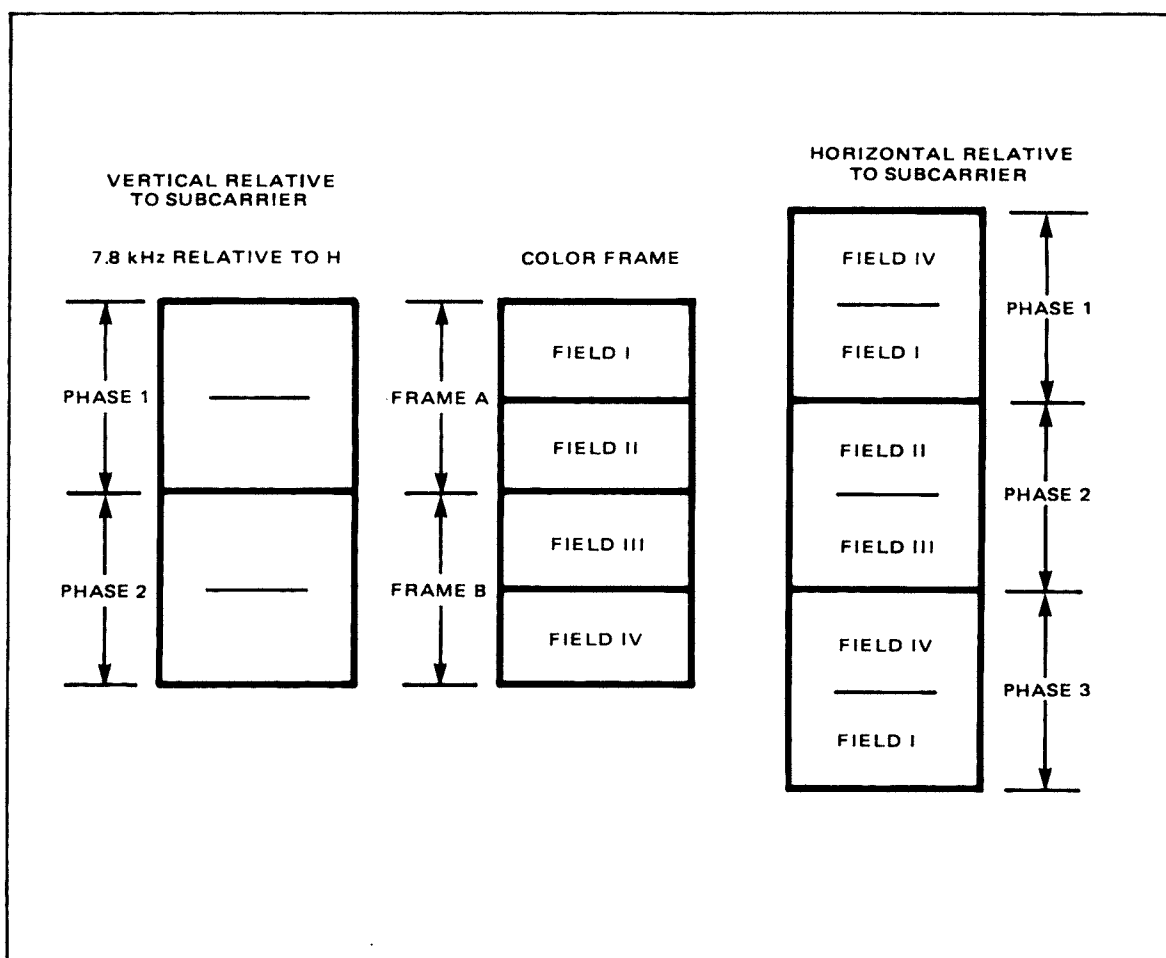


Figure 15-1. Color Field Phase Relationship

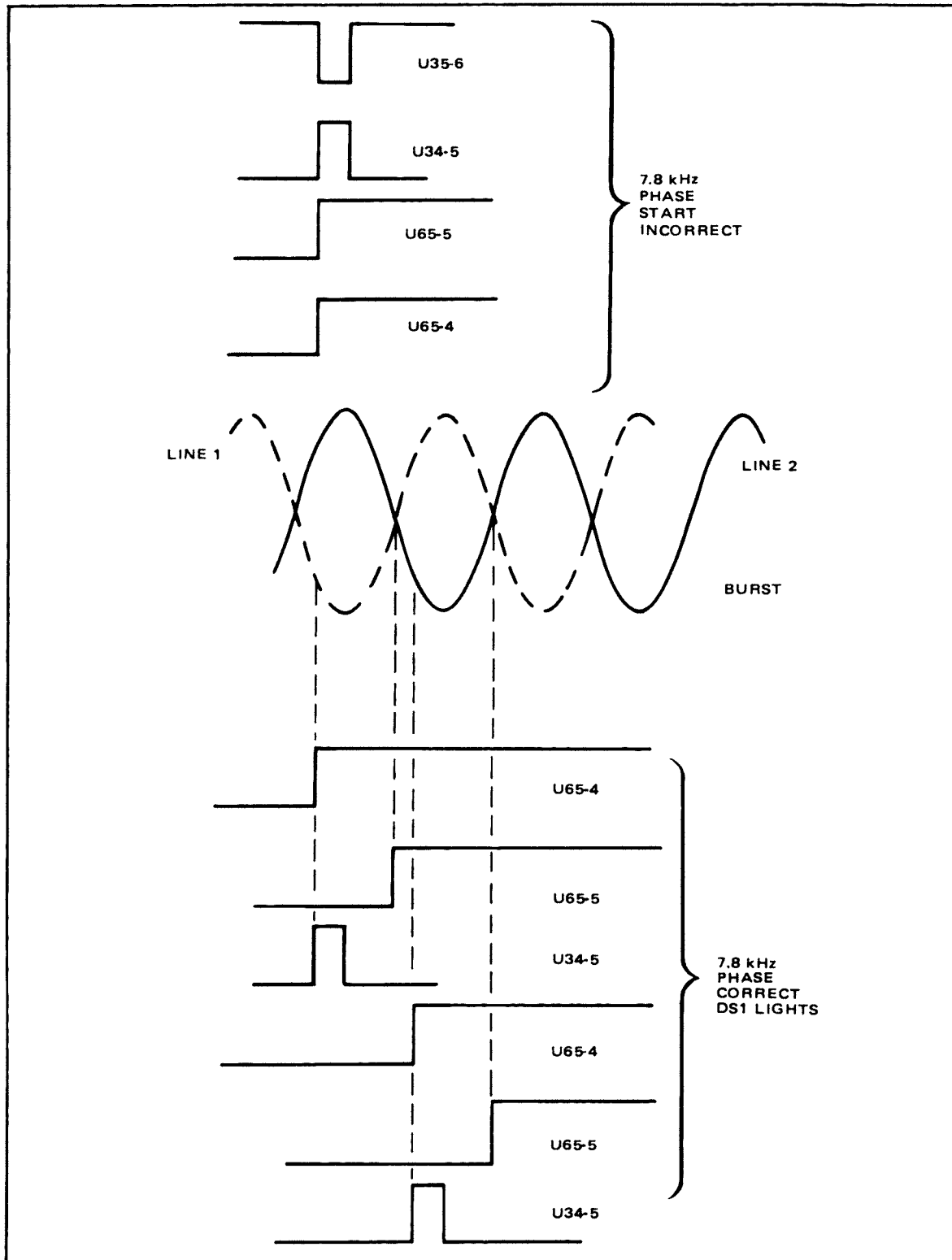


Figure 15-2. Frame 7.8 kHz Phase Correction Circuitry, Timing Diagram

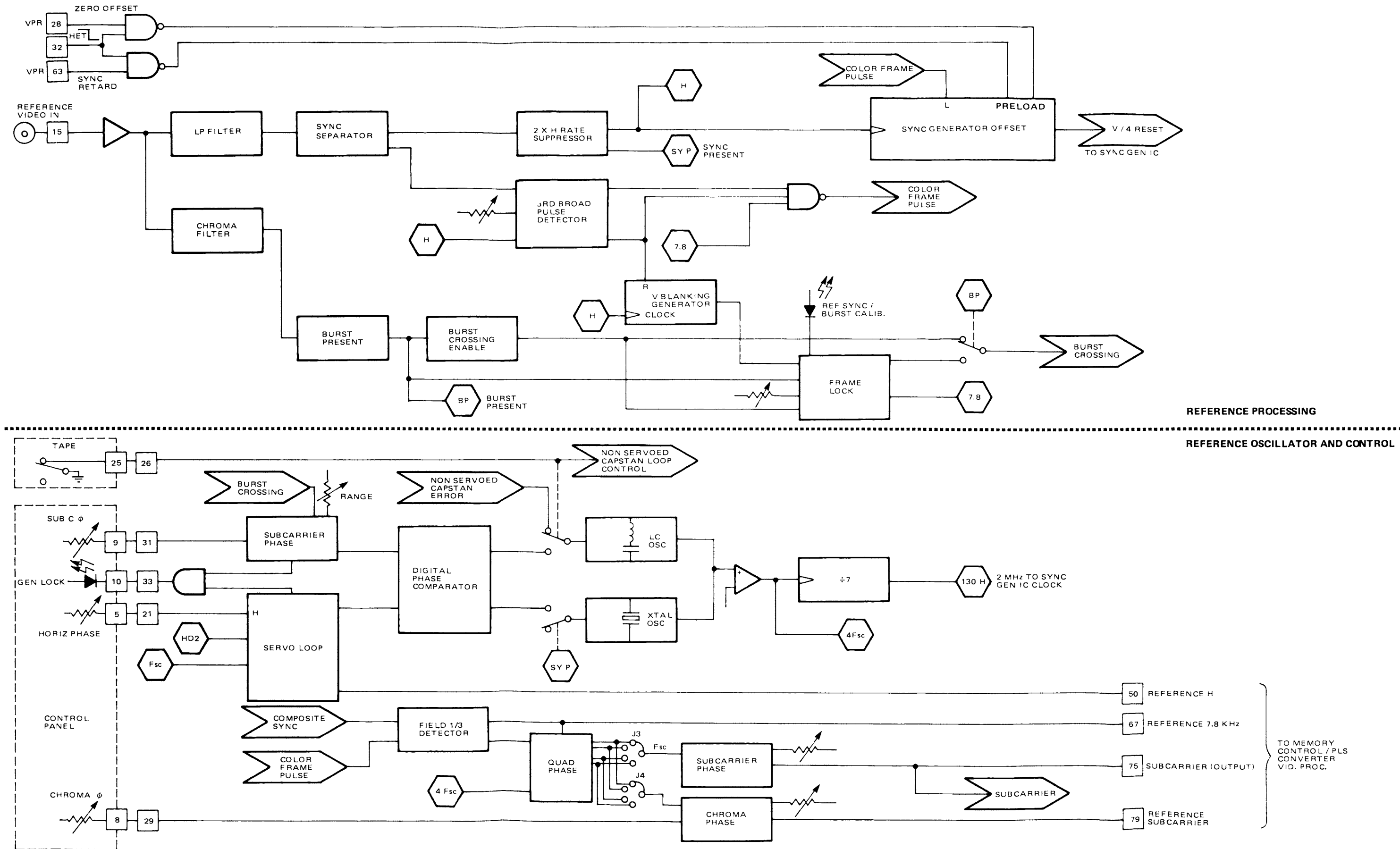
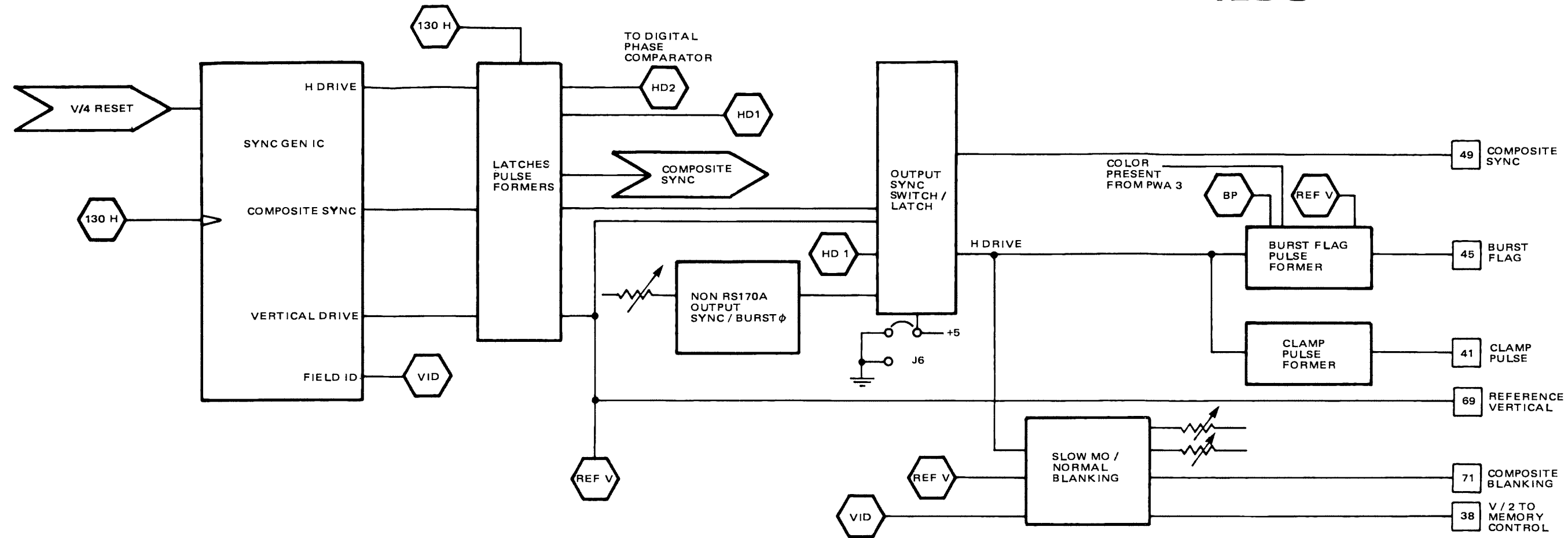


Figure 15-3.
Sync Generator PWA 15 Simplified Block
Diagram (12-line) (Sheet 1 of 2)



OUTPUT SYNC AND BLANKING

ADVANCED REFERENCE

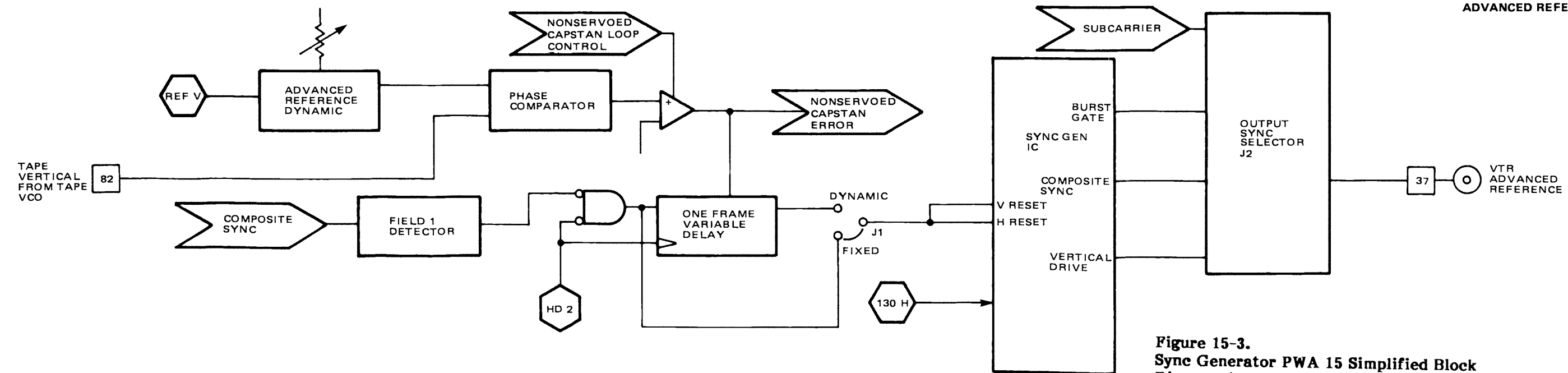


Figure 15-3.
Sync Generator PWA 15 Simplified Block
Diagram (12-line) (Sheet 2 of 2)

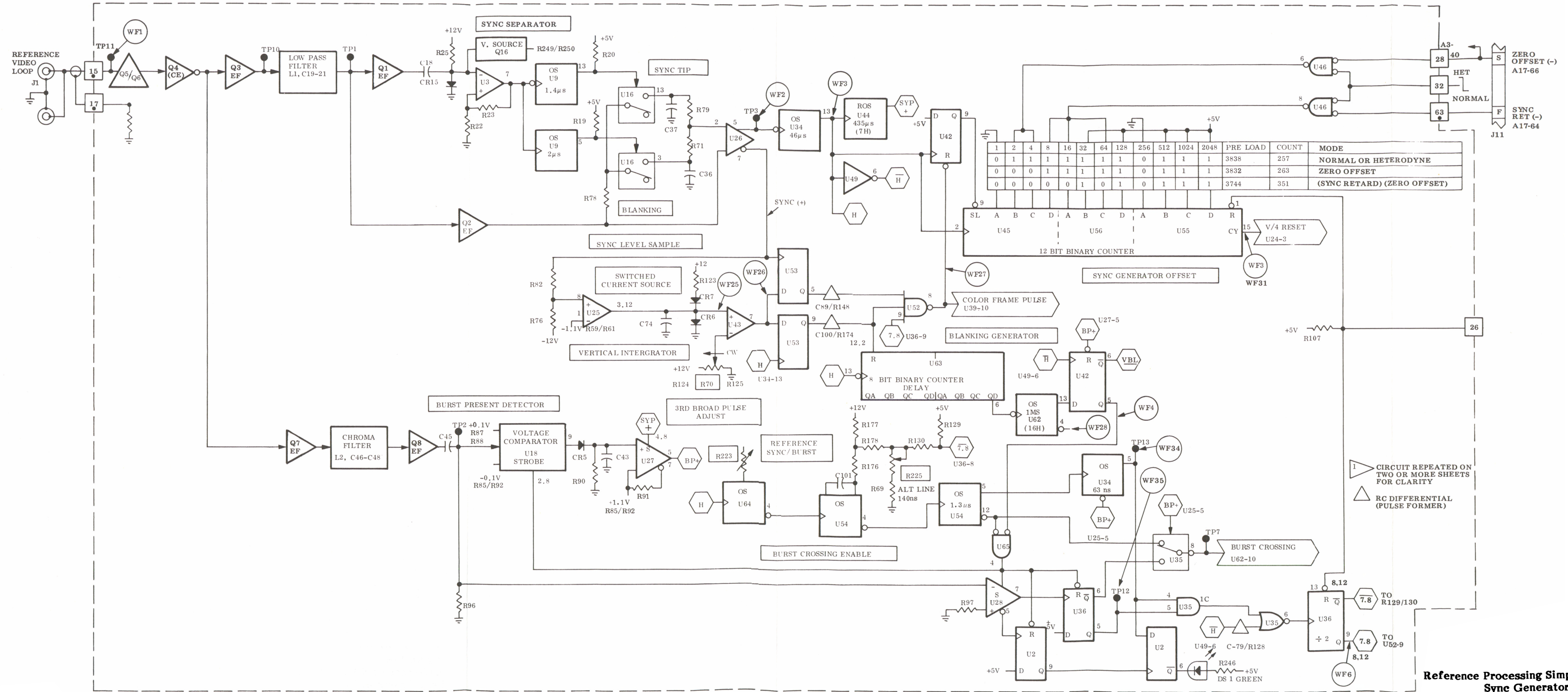


Figure 15-4.
Reference Processing Simplified Schematic,
Sync Generator PWA 15 (12-line)

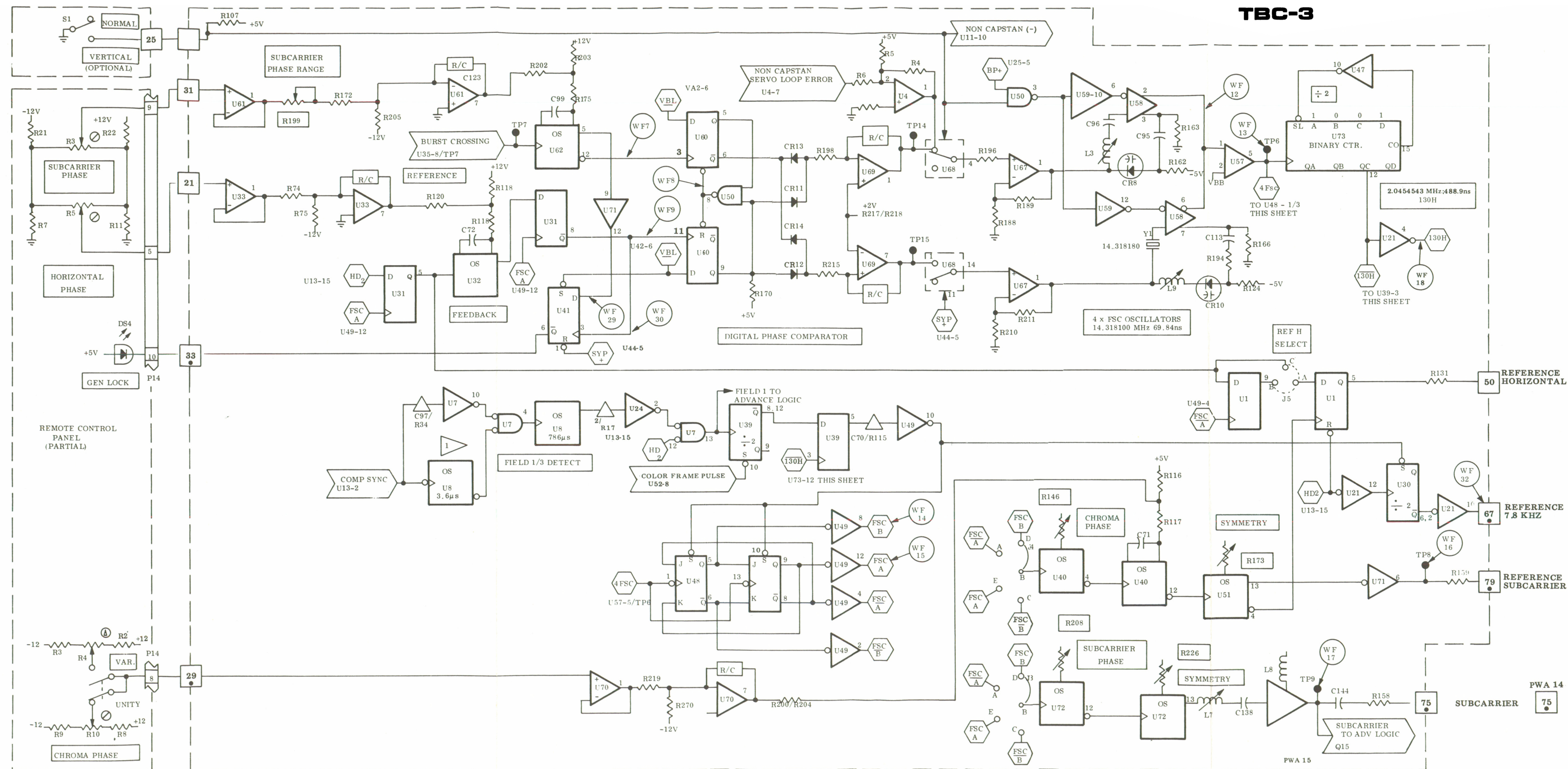


Figure 15-5.
Reference Oscillators Simplified Schematic,
Sync Generator PWA 15, (12-line)

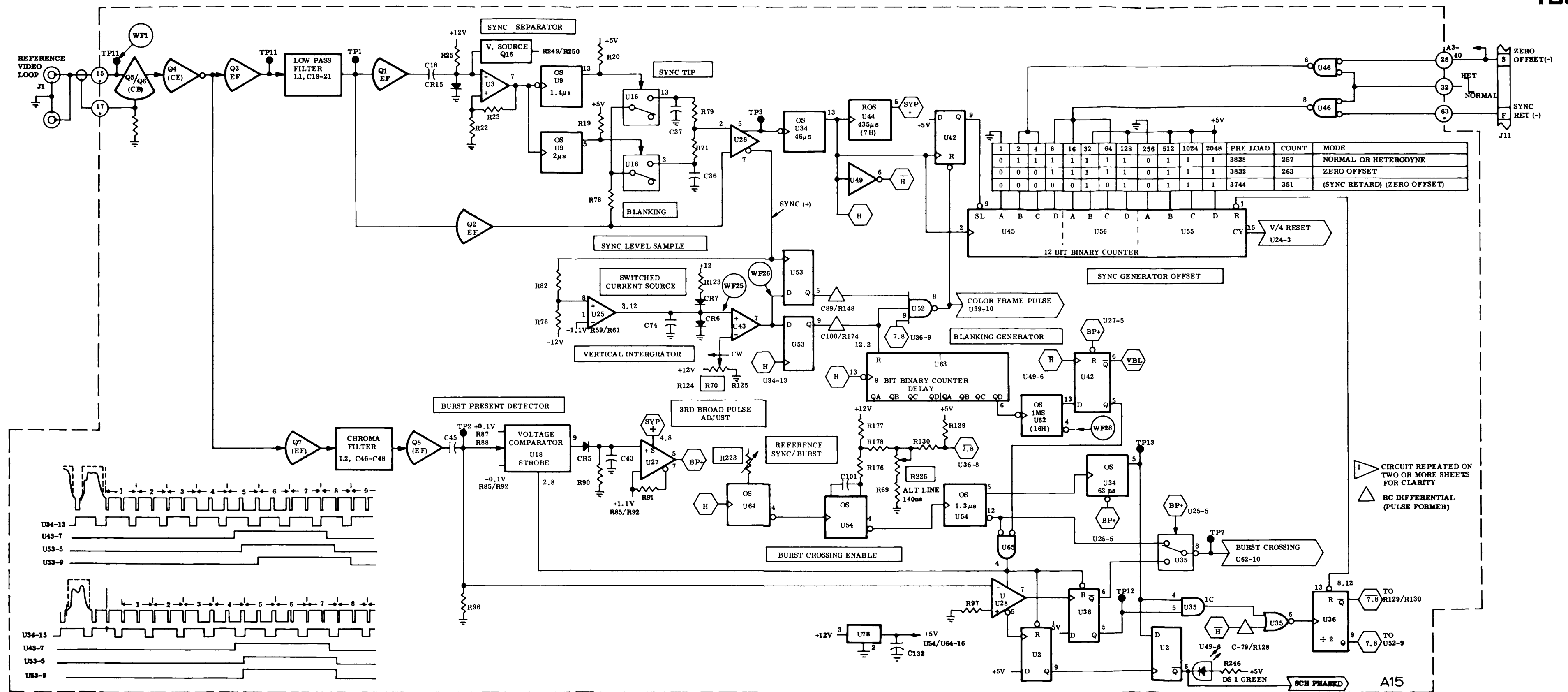


Figure 15-8.
Reference Processing Simplified Schematic,
Sync Generator PWA 15 (16-line)

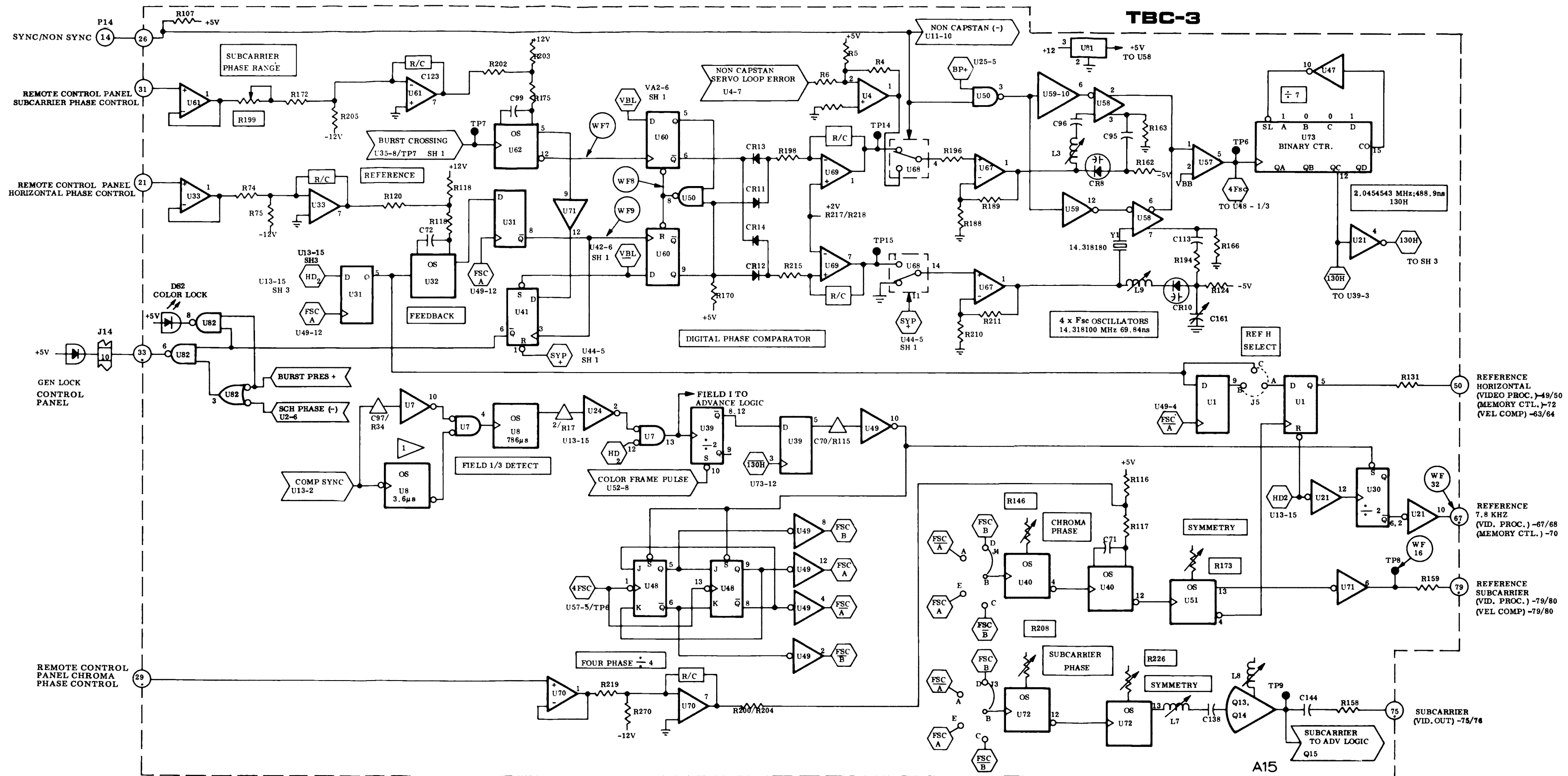


Figure 15-9.
Reference Oscillators Simplified Schematic,
Sync Generator PWA 15 (16-line)

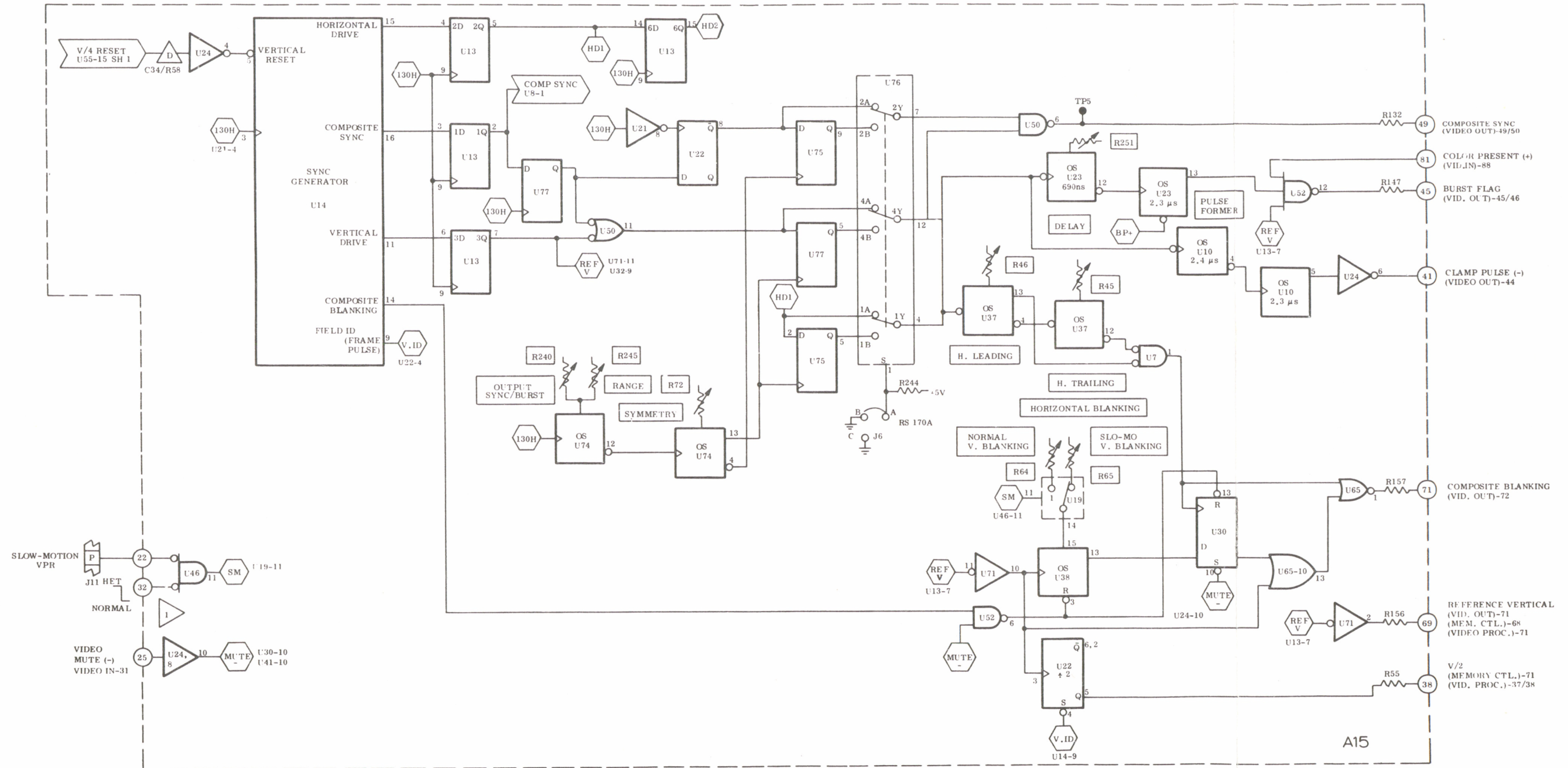


Figure 15-10.
Output Sync Generator Sync and Blanking Simplified
Schematic, Sync Generator PWA 15 (16-line)

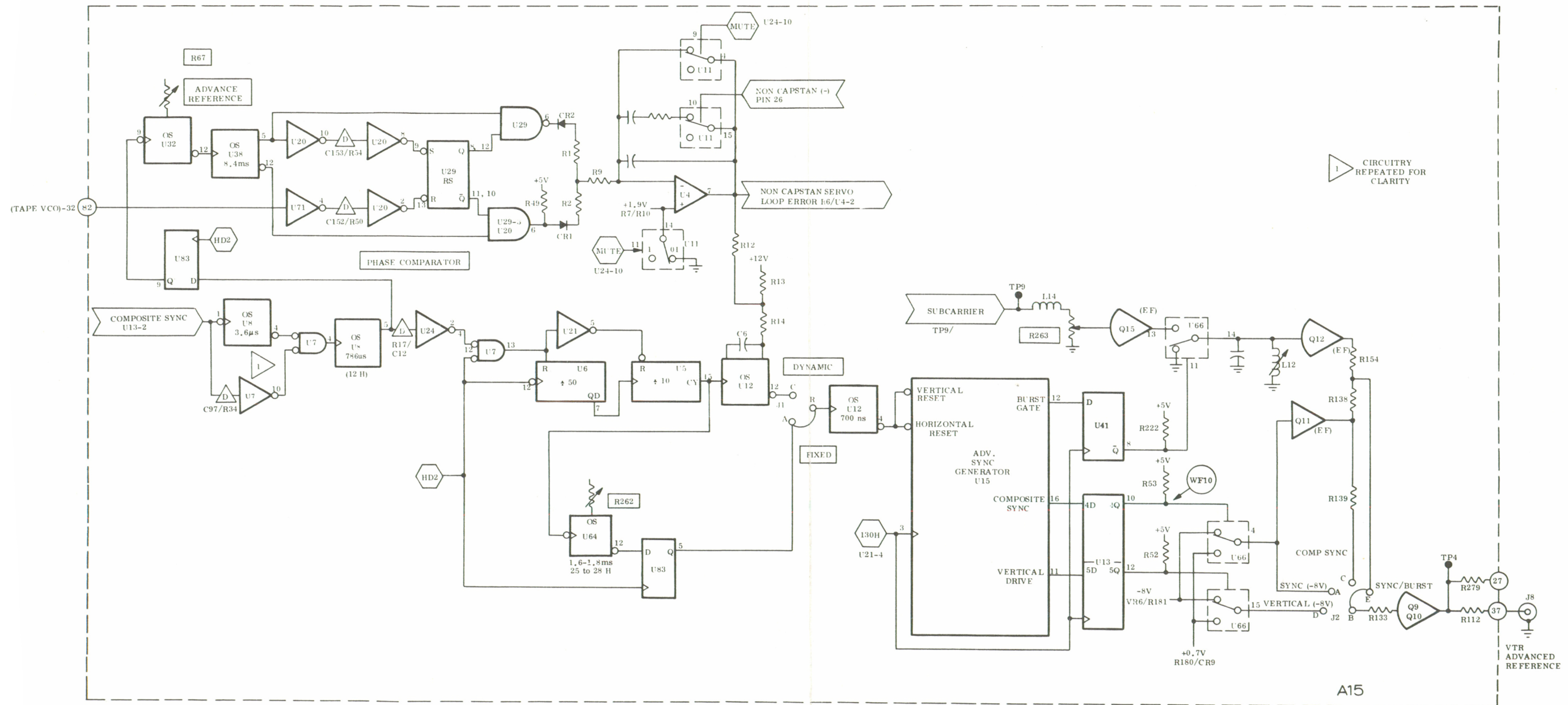
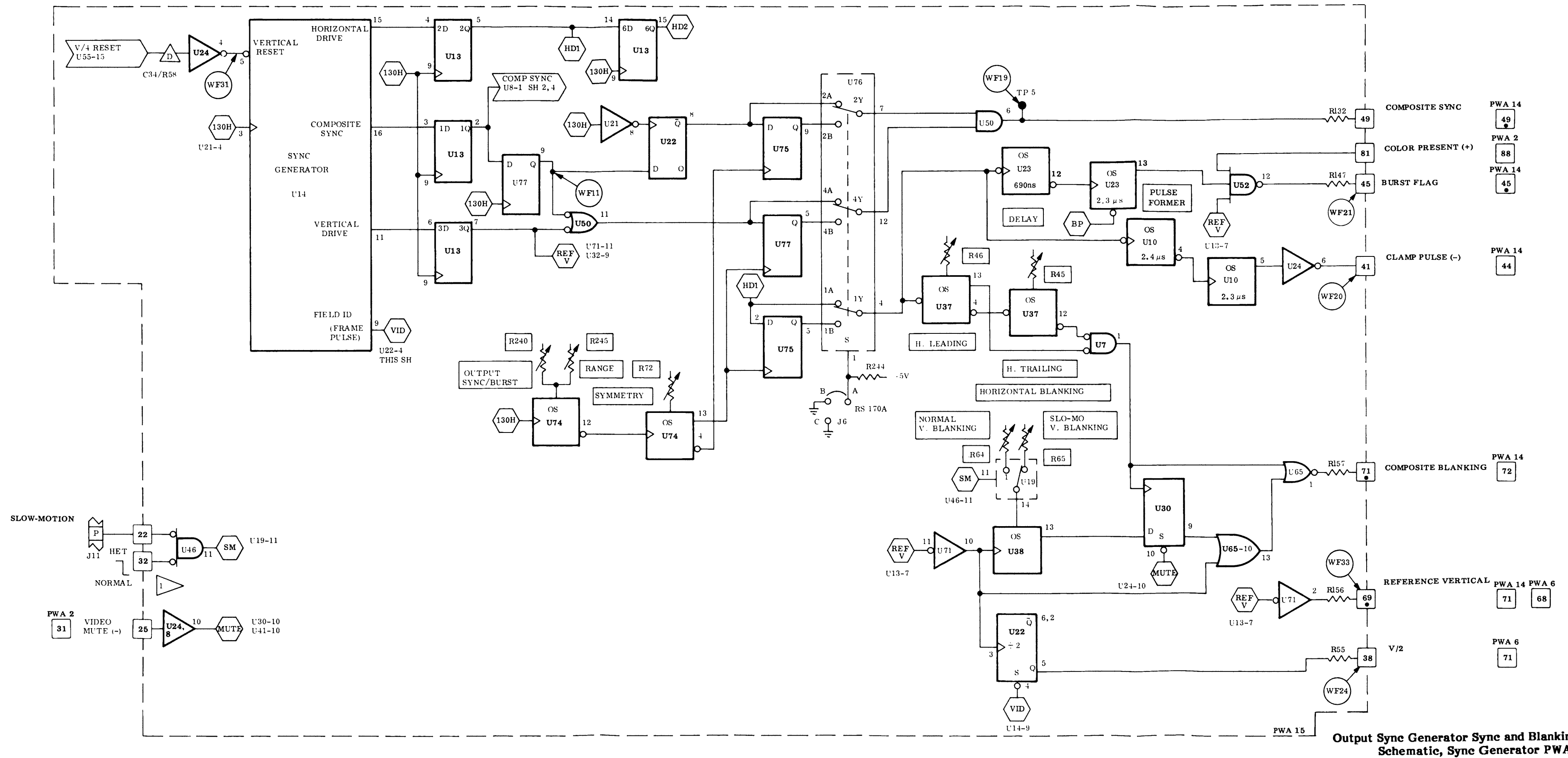


Figure 15-11.
Noncapstan Servo and Advanced Reference Simplified
Schematic, Sync Generator PWA 15 (16-line)



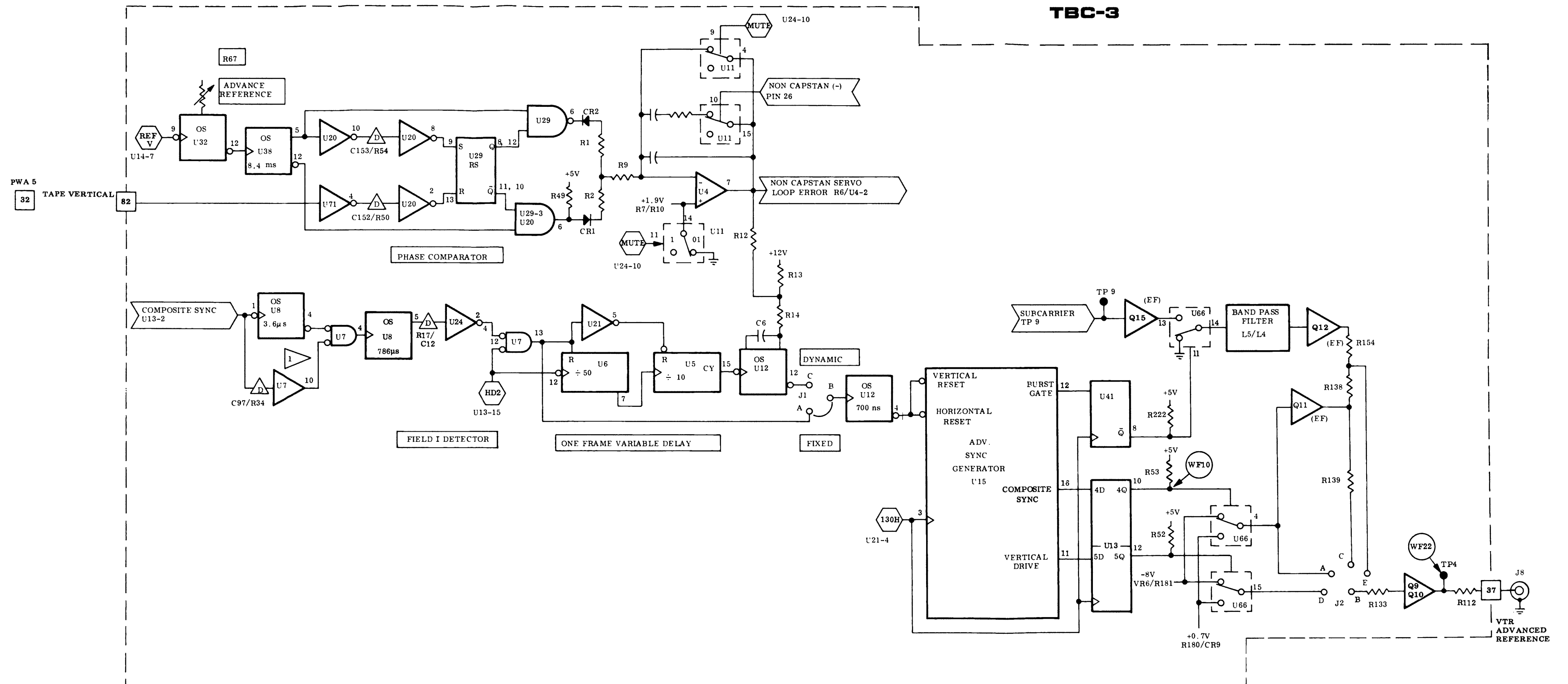


Figure 15-7.
Noncapstan Servo and Advanced Reference Simplified
Schematic, Sync Generator PWA 15 (12-line)

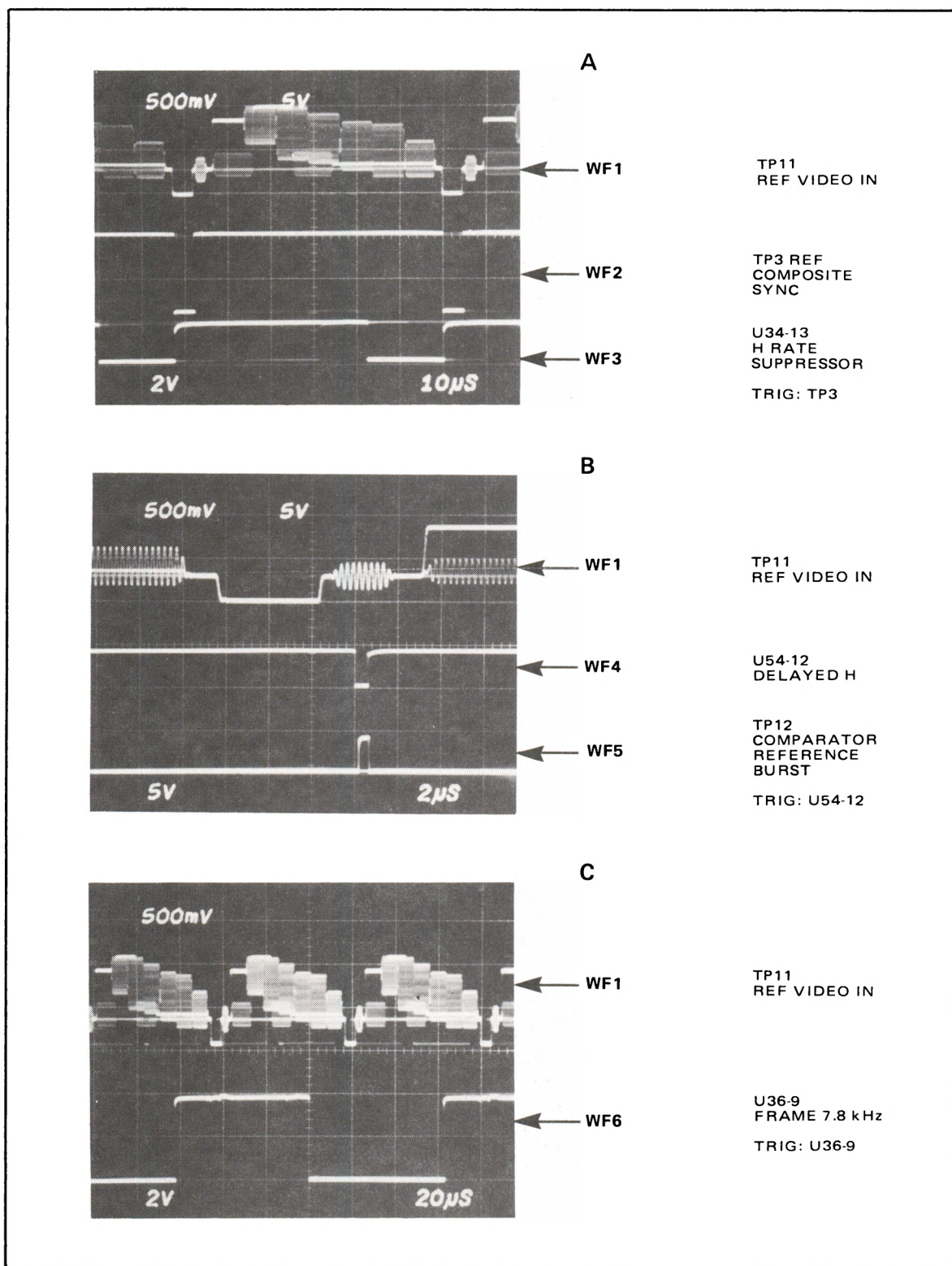


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 1 of 8)

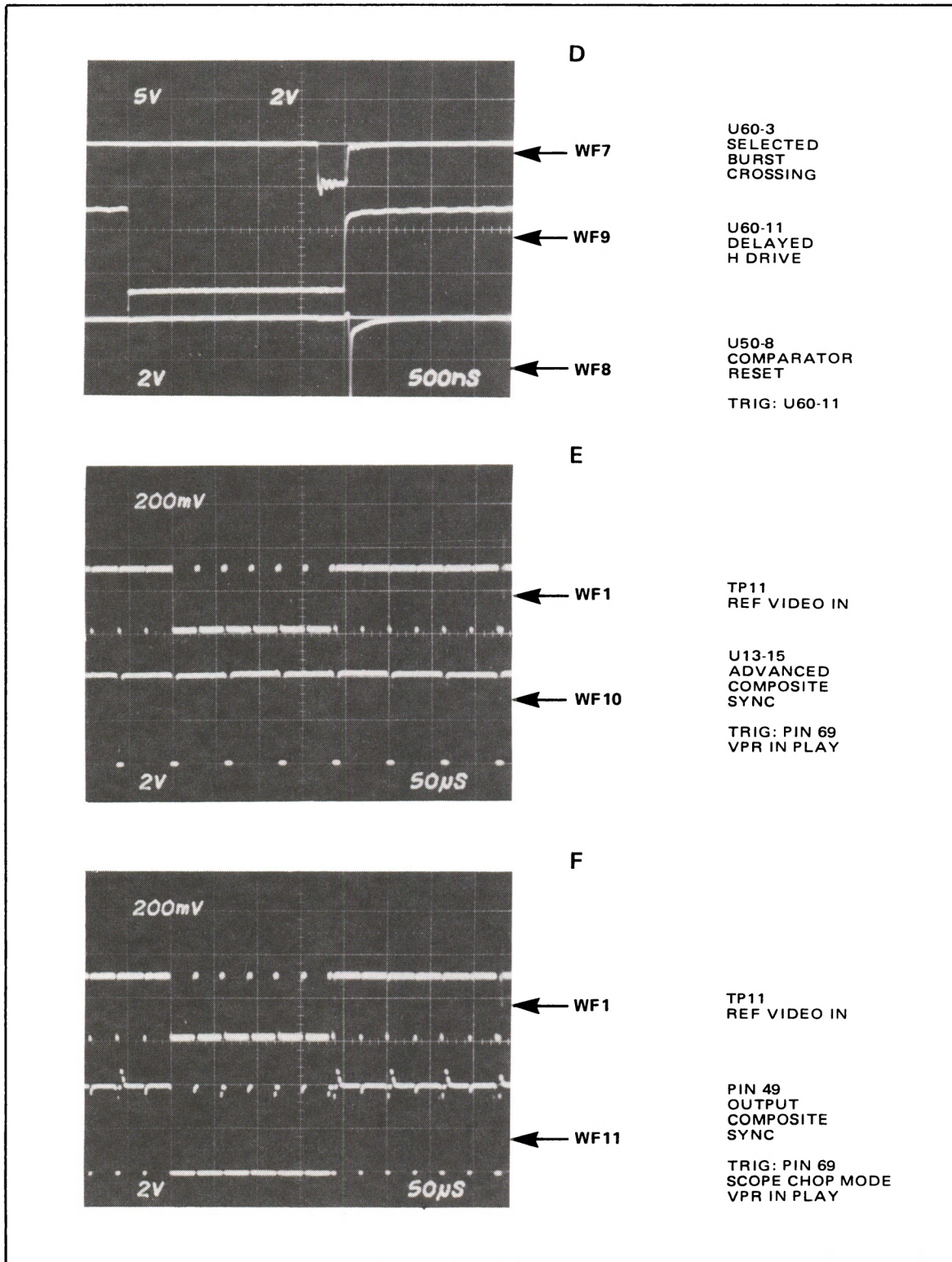


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 2 of 8)

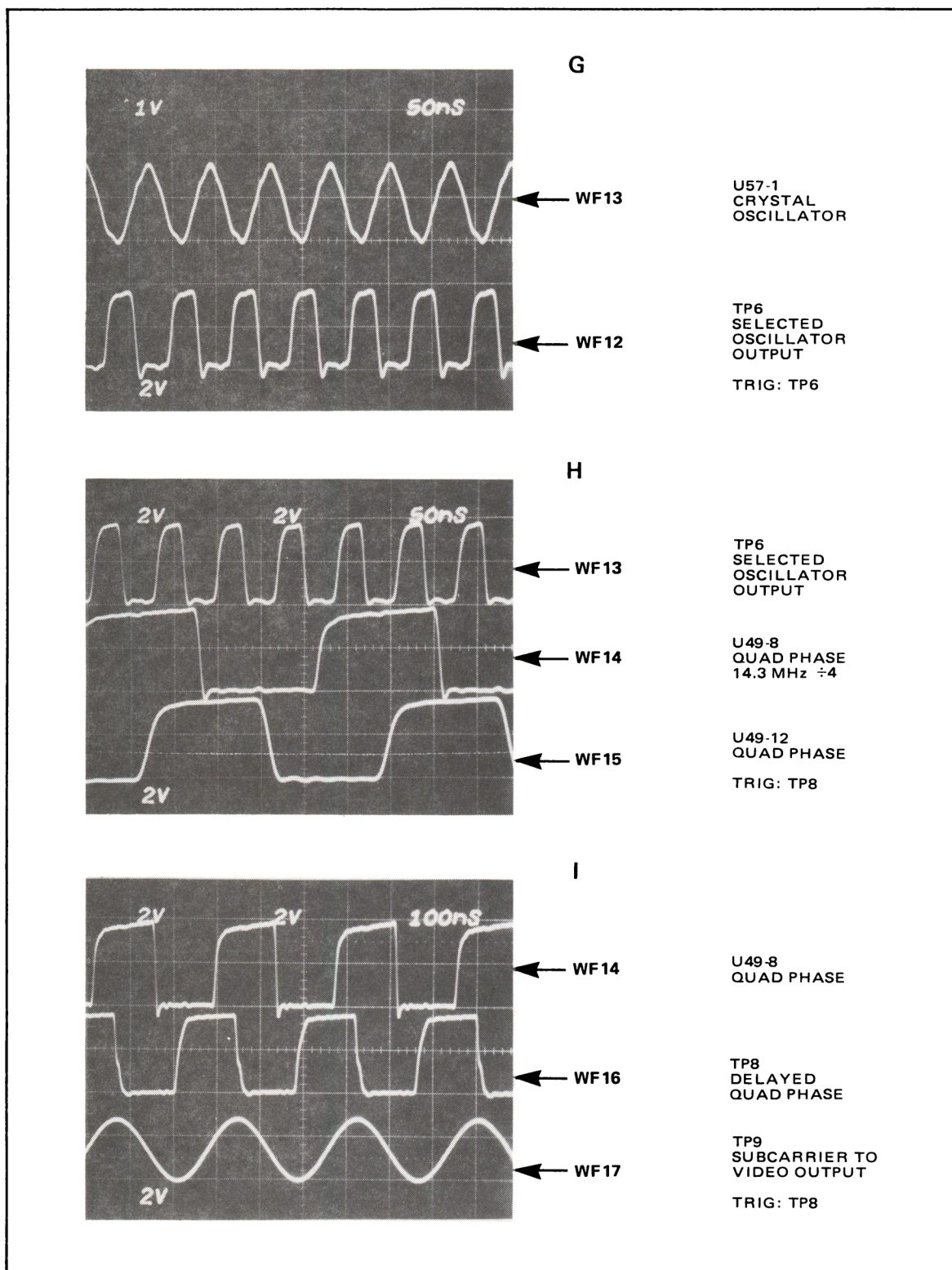


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 3 of 8)

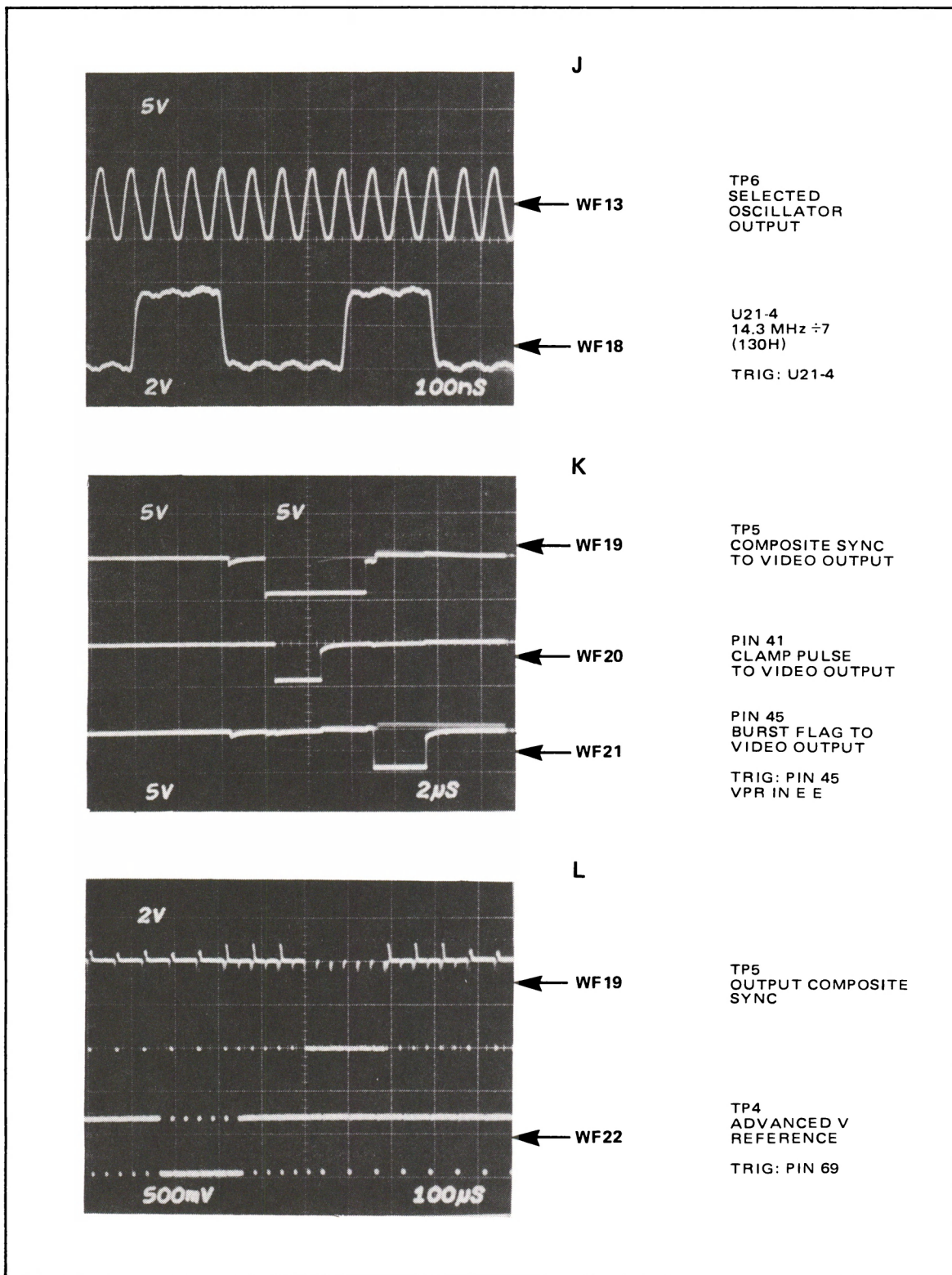


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 4 of 8)

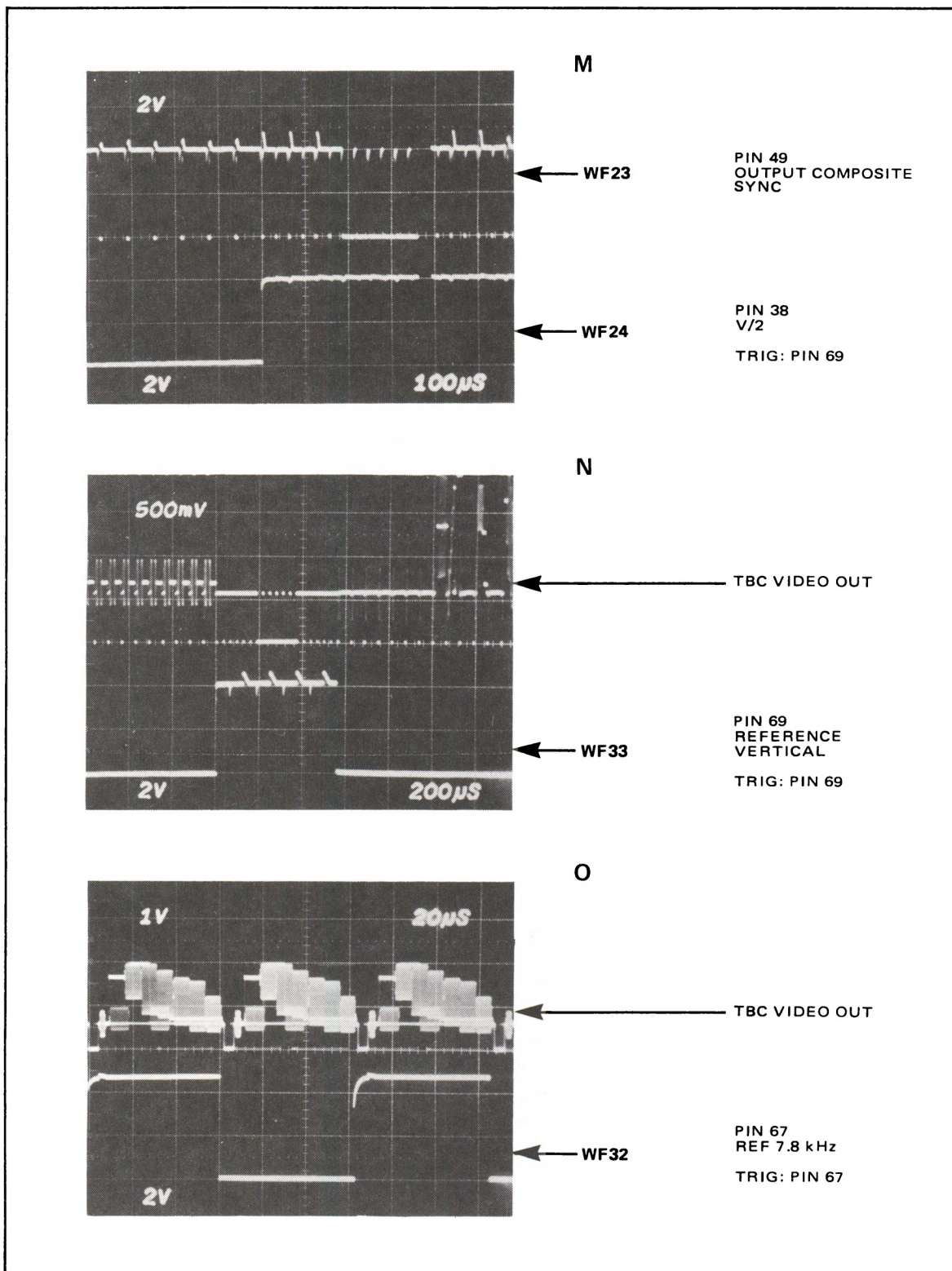


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 5 of 8)

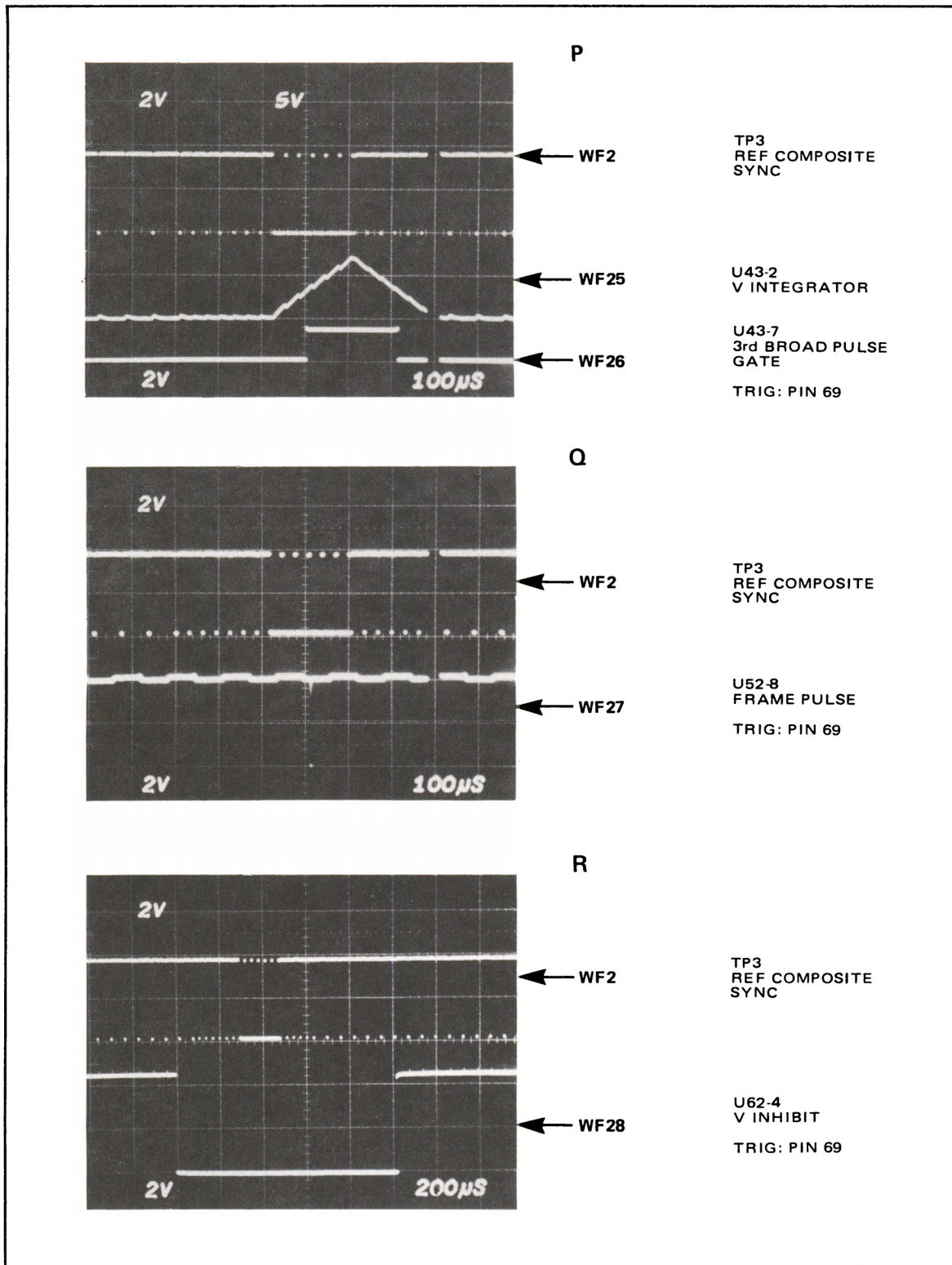


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 6 of 8)

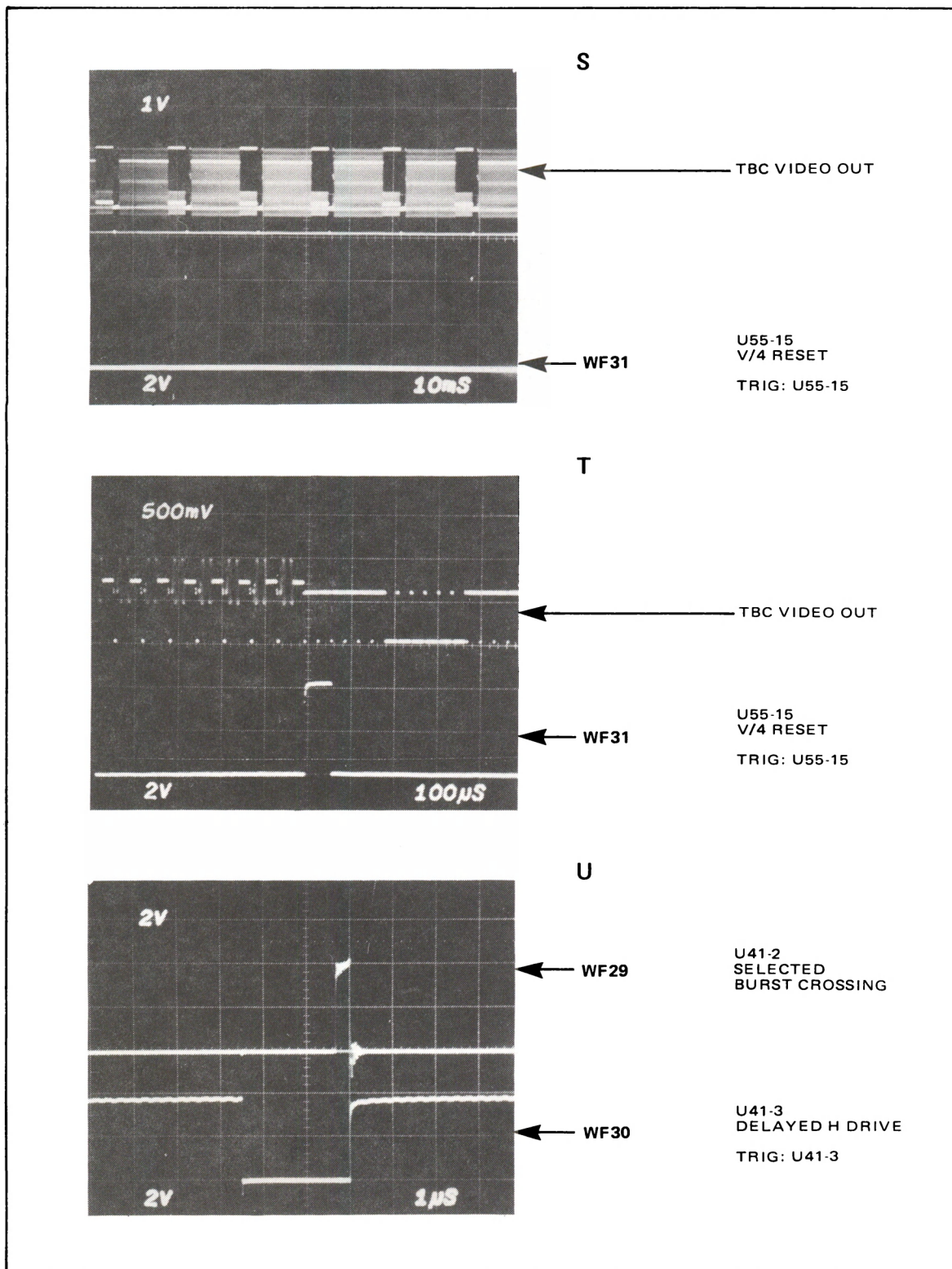


Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 7 of 8)

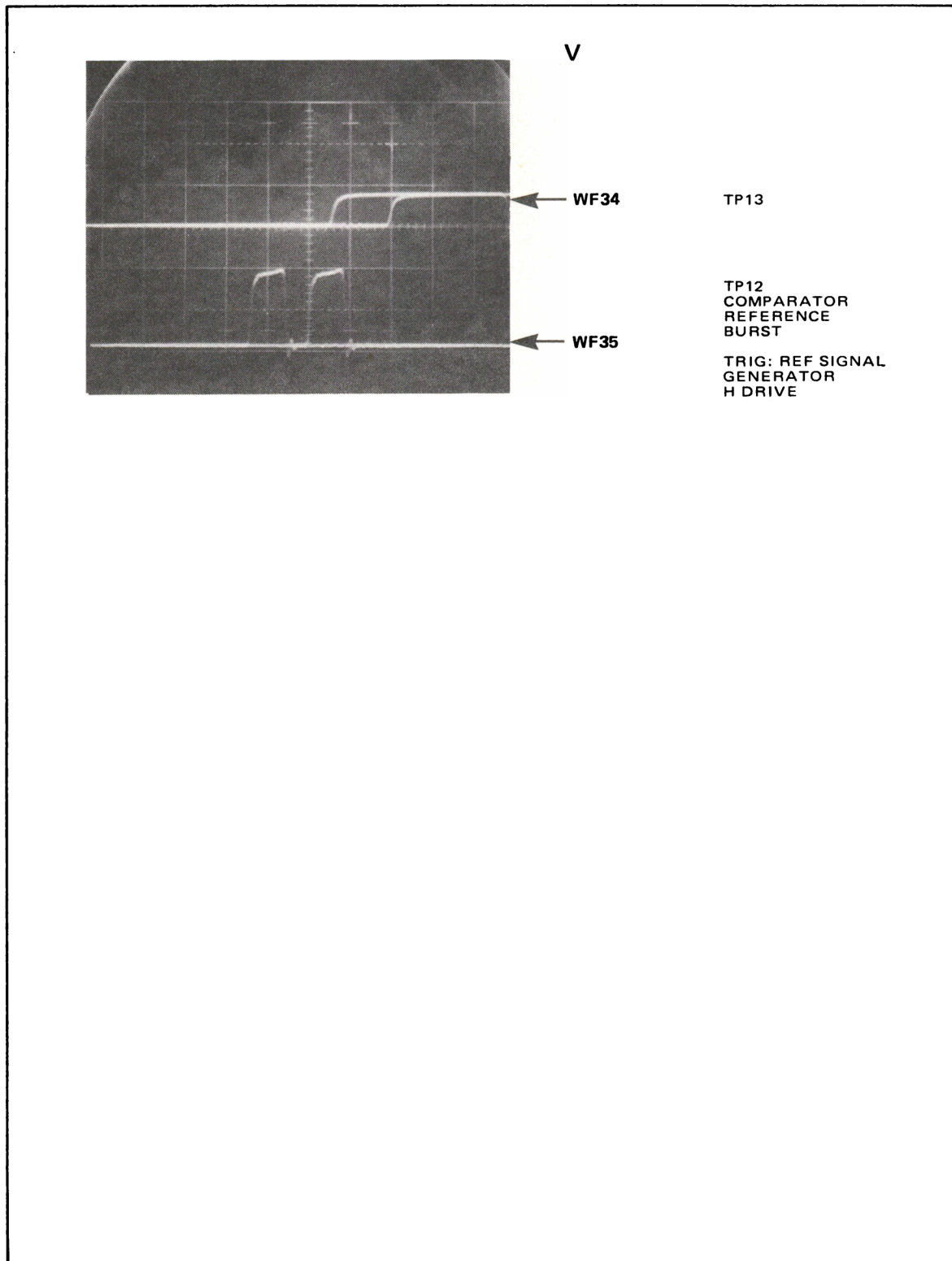


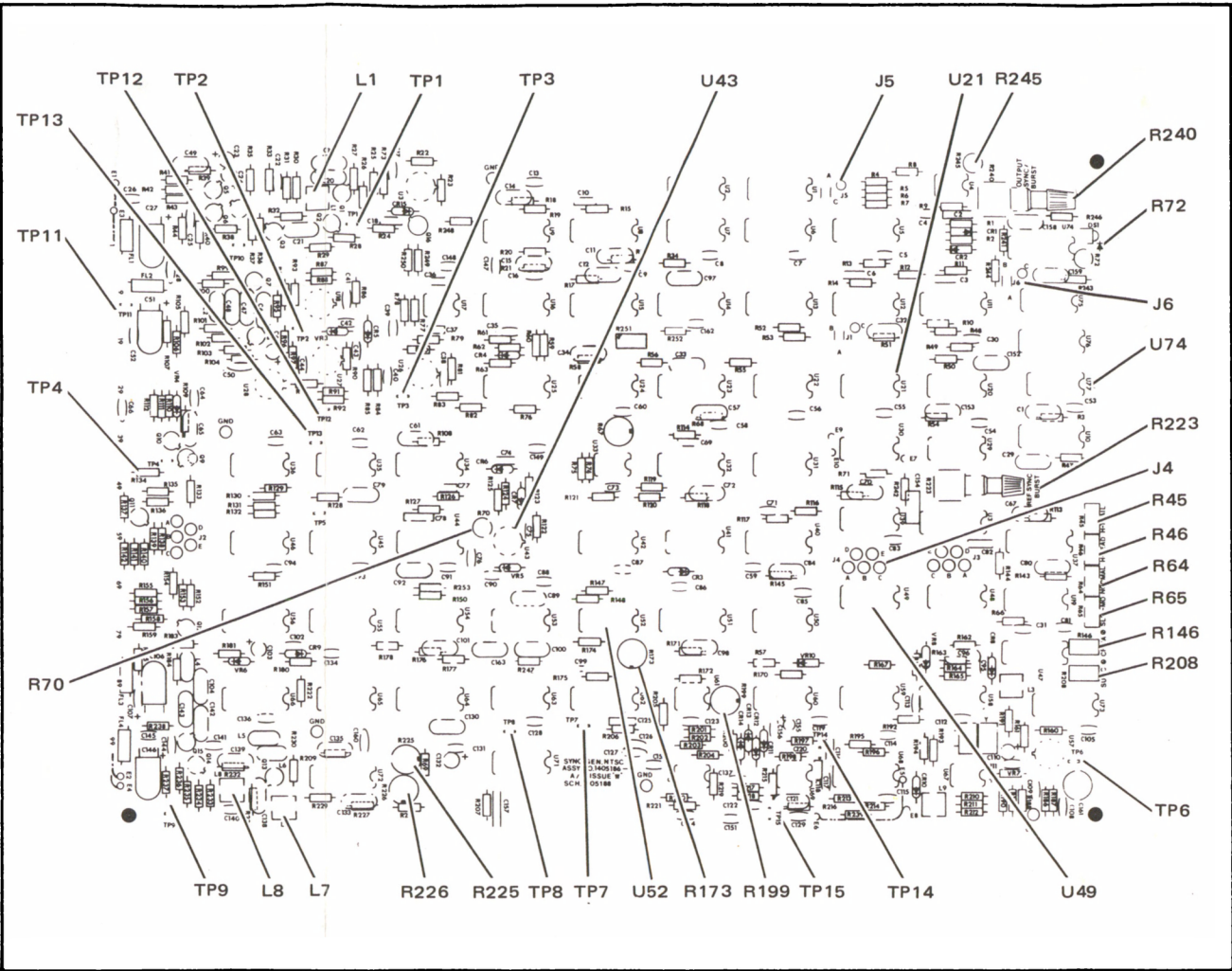
Figure 15-12. Sync Generator PWA 15 Waveforms (Sheet 8 of 8)

PWA 15 Jumpers

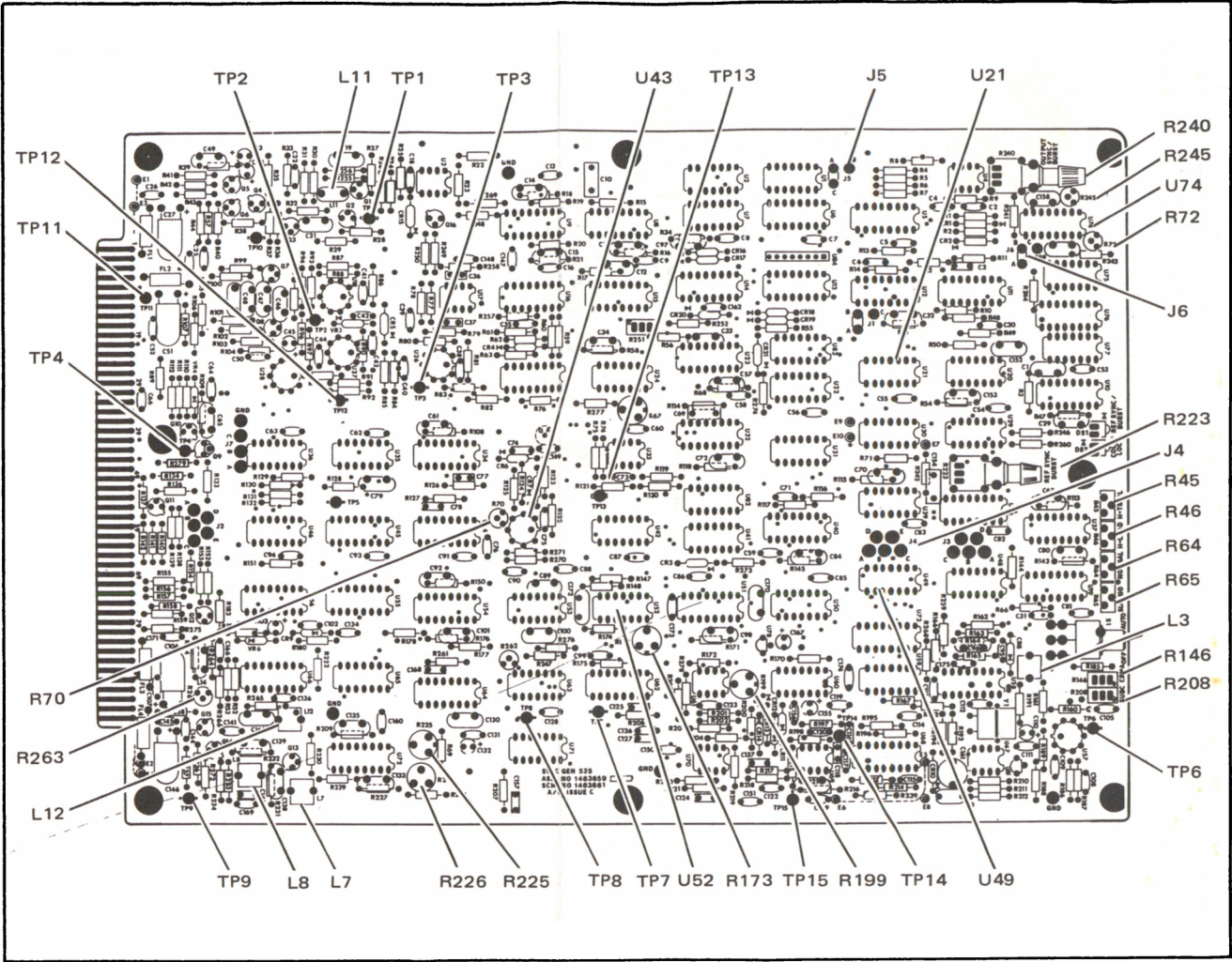
Jumper	Position	Function
J1	A-B	VPR/Heterodyne Select
	B-C	Fixed; VPR-2B/VPR-3
J2	B-C	Dynamic; heterodyne VTR
	A-B	Advanced Reference Select
	B-C	Composite sync (-8V)
	B-D	Composite sync
	B-E	Vertical (-8V)
J3	B-E	Sync and subcarrier (VPR-3)
	A-B	Reference 3.58 MHz
	B-C	Select jumper position as required for correct system operation
	B-D	
	B-E	
J4	B-E	Subcarrier
	A-B	Select jumper position as required for correct system operation
	B-C	
	B-D	
	B-E	
J5	A-B	H-phase select
	B-C	Select jumper position as required for correct system operation
J6	A-B	RS170A Standard Select
	B-C	RS 170A Standard
J7 (16-line sync gen only)	A-B	Non-standard
	B-C	Mode switch lockout
		VPR-3 (normal only)
		VPR-2B (selectable)

PWA 15 Adjustable Components

Component	Function
L1	Video low-pass filter
L3	LC oscillator frequency
L7	Subcarrier filter
L8	Subcarrier filter
L9	Crystal oscillator frequency
L12	Sch phase advance trim (16-line only)
R45	H-sync leading edge
R46	H-syc trailing edge
R64	V-sync normal
R65	V-sync slow motion
R67	Reference vertical delay
R72	Output sync/burst symmetry
R70	3rd broad pulse detector level
R146	Chroma phase
R173	Chroma symmetry
R199	Subcarrier phase offset
R208	Subcarrier phase
R223	Reference sync/burst calibration
R225	7.8-kHz detector
R226	Subcarrier symmetry
R240	Output sync/burst
R245	Output sync/burst range (coarse)
R262	Line advance (16-line only)
R263	Advance sync burst level (16-line only)



PWA 15 Component Locator-12 Line



PWA 15 Component Locator-16 Line

PWA 15 Test Points

Test Point	Name
TP1	Filtered video
TP2	Chroma
TP3	Composite sync
TP4	Advanced reference
TP5	Composite sync out
TP6	14.3 MHz
TP7	Reference burst
TP8	Reference 3.58 Mhz
TP9	Subcarrier
TP10	Amplified video
TP11	Reference video input
TP12	Comparator reference burst
TP13	Delayed reference sync/burst
TP14	LC oscillator error
TP15	Crystal oscillator error

Figure 15-13.
Test Points, Jumpers, Adjustable Components,
Component Locator, Sync Generator PWA 15